MOTOROLA

MC14160B
MC14161B
MC14162B
MC14163B

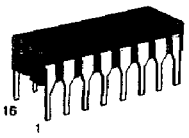
CMOS MSI

SYNCHRONOUS PRESETTABLE 4-BIT COUNTERS

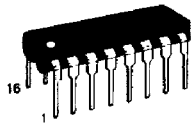
The MC14160B – MC14163B are synchronous programmable counters constructed with complementary MOS P-Channel and N-Channel enhancement mode devices in a single monolithic structure. These counters are functionally equivalent to the 74160–74163 TTL counters.

Two are synchronous programmable BCD counters with asynchronous and synchronous clear inputs respectively (MC14160B, MC14162B). The other two are synchronous programmable 4-bit binary counters with the asynchronous and synchronous clear respectively (MC14161B, MC14163B).

- Internal Look-Ahead for Fast Counting
- Carry Output for N-Bit Cascading
- Synchronously Programmable
- Synchronous Counting
- Load Control Line
- Synchronous or Asynchronous Clear
- Positive Edge Clocked



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648

D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

T_A = −55° to 125°C for all packages.

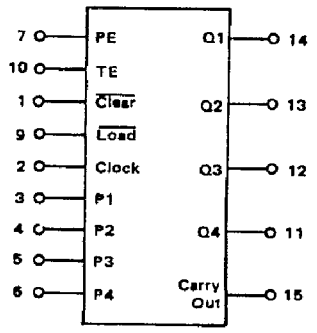
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: −7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: −12 mW/°C From 100°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
Output Voltage V_{in} = V_{DD} or 0	"0" Level	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
V_{in} = 0 or V_{DD}	"1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	"0" Level	V_{IL}	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
(V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	"1" Level	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	Source	I_{OH}	5.0 5.0 10 15	−3.0 −0.64 −1.6 −4.2	— — — —	−2.4 −0.51 −1.3 −3.4	−4.2 −0.88 −2.25 −8.8	— — — —	−1.7 −0.36 −0.9 −2.4	— — — —	mAdc
(V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	Sink	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current		I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V_{in} = 0)		C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)		I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	μAdc
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)		I_T	5.0 10 15	I_T = (0.56 μA/kHz) f + I_{DD} I_T = (1.10 μA/kHz) f + I_{DD} I_T = (1.90 μA/kHz) f + I_{DD}							μAdc

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

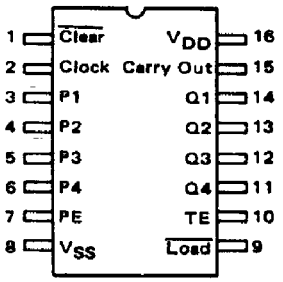
**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

PIN ASSIGNMENT



SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise Time	t_{TLH}					ns
		5.0	—	100	200	
		10	—	50	100	
		15	—	40	80	
Output Fall Time	t_{THL}					ns
		5.0	—	100	200	
		10	—	50	100	
		15	—	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock to Q						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 305 ns		5.0	—	350	700	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 132 ns		10	—	150	300	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 87 ns		15	—	100	200	
Clock to Carry Out						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 395 ns		5.0	—	440	880	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 167 ns		10	—	185	370	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 112 ns		15	—	125	250	
TE to Carry Out						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 225 ns		5.0	—	300	600	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 112 ns		10	—	130	260	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 77 ns		15	—	90	180	
$\overline{\text{Clear}}$ to Q (MC14160B, MC14161B only)						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 110 ns		5.0	—	350	700	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 37 ns		10	—	150	300	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 22 ns		15	—	100	200	
Setup Times						
Data to Clock	t_{su}	5.0	320	160	—	ns
		10	130	65	—	
		15	90	45	—	
$\overline{\text{Load}}$ to Clock		5.0	600	300	—	
		10	260	130	—	
		15	180	90	—	
Enable to Clock (PE or TE)		5.0	420	210	—	
		10	170	85	—	
		15	120	60	—	
$\overline{\text{Clear}}$ to Clock (MC14162B, MC14163B only)		5.0	310	155	—	
		10	110	55	—	
		15	70	35	—	
Hold Times						
Clock to Data	t_h	5.0	−10	−60	—	ns
		10	−5	−25	—	
		15	0	−15	—	
Clock to $\overline{\text{Load}}$		5.0	−40	−195	—	
		10	−10	−80	—	
		15	−5	−50	—	
Clock to PE		5.0	−40	−175	—	
		10	−10	−70	—	
		15	0	−40	—	
Clock to TE		5.0	−150	−280	—	
		10	−30	−130	—	
		15	−20	−80	—	
Clock to $\overline{\text{Clear}}$ (MC14162B, MC14163B only)		5.0	80	40	—	
		10	30	15	—	
		15	−10	−70	—	
$\overline{\text{Clear}}$ Removal Time (MC14160B, MC14161B only)	t_{rem}	5.0	90	30	—	ns
		10	65	20	—	
		15	55	20	—	

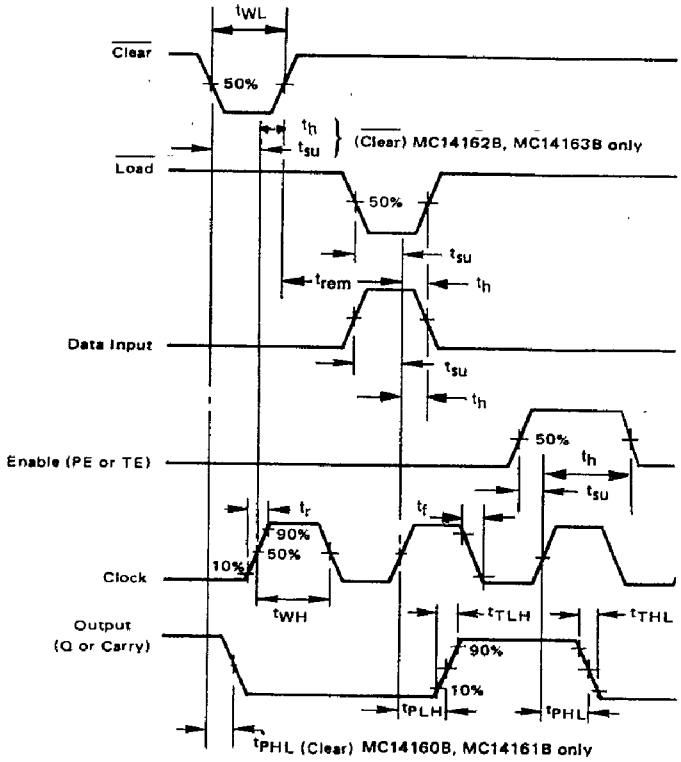
SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C) (Continued)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
$\overline{\text{Clear}}$ Pulse Width, Low (MC14160B, MC14161B only)	t_{WL}	5.0	200	100	—	ns
		10	90	45	—	
		15	60	30	—	
Clock Pulse Width, High	t_{WH}	5.0	250	125	—	ns
		10	100	50	—	
		15	70	35	—	
Clock Rise and Fall Time	t_r, t_f	5	—	—	15	μs
		10	—	—	5	
		15	—	—	4	
Clock Pulse Frequency	f_{cl}	5.0	—	2.0	1.0	MHz
		10	—	5.0	2.5	
		15	—	8.0	4.0	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

SWITCHING WAVEFORMS

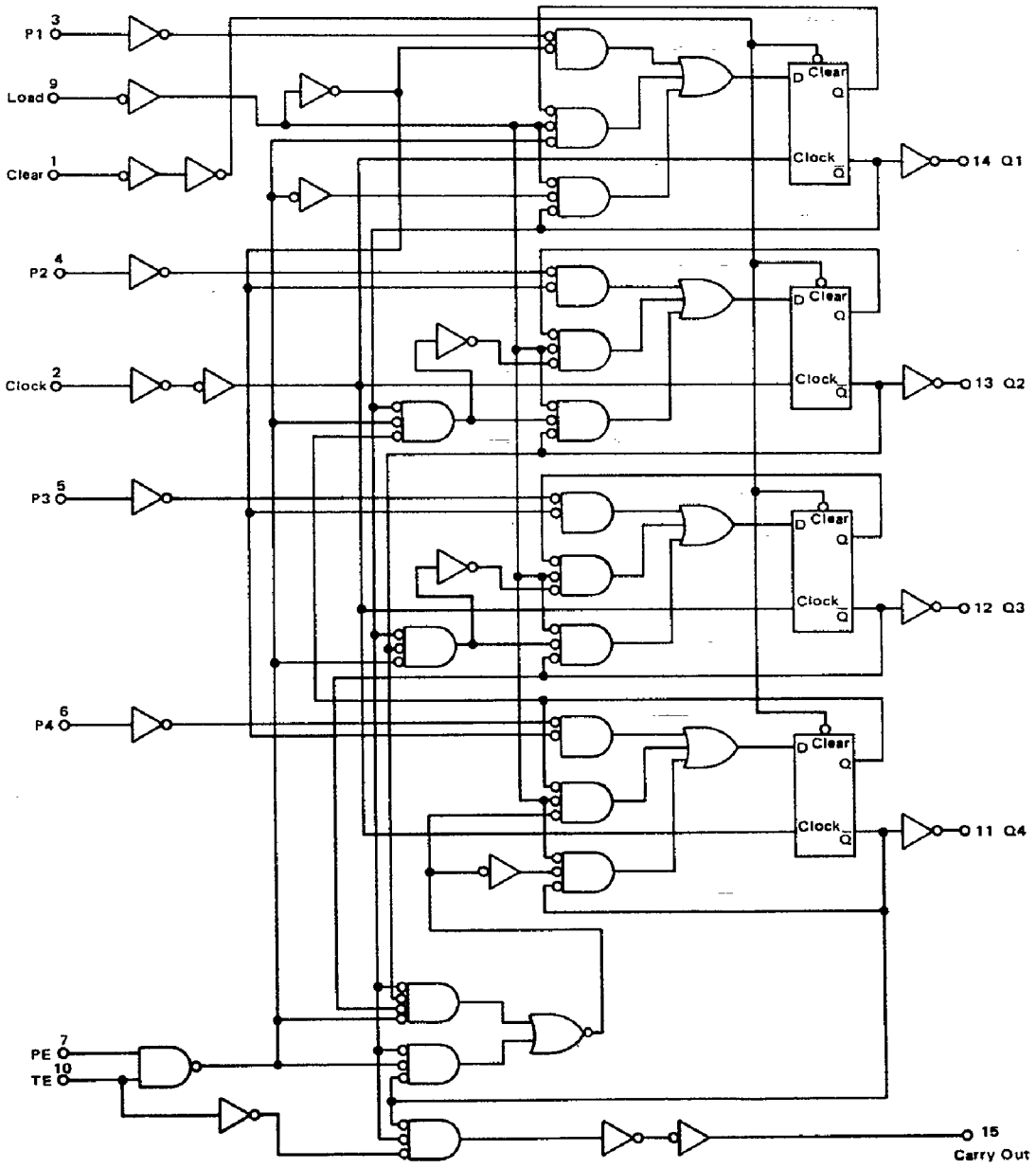


FUNCTIONAL DESCRIPTION

These counters are fully programmable; that is the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. The clear function for the MC14160B, MC14161B is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the clock, load or enable inputs. The clear function for the MC14162B and MC14163B is synchronous and a low level at the clear inputs sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily; decoding the maximum count desired can be acomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count-enable inputs (PE, TE) must be high to count, and enable input TE fed forward to enable the carry output. The carry output thus enabled will produce a positive output pulse with a duration approximately equal to the positive portion of the Q1 output. This positive overflow carry pulse can be used to enable successive cascaded stages.

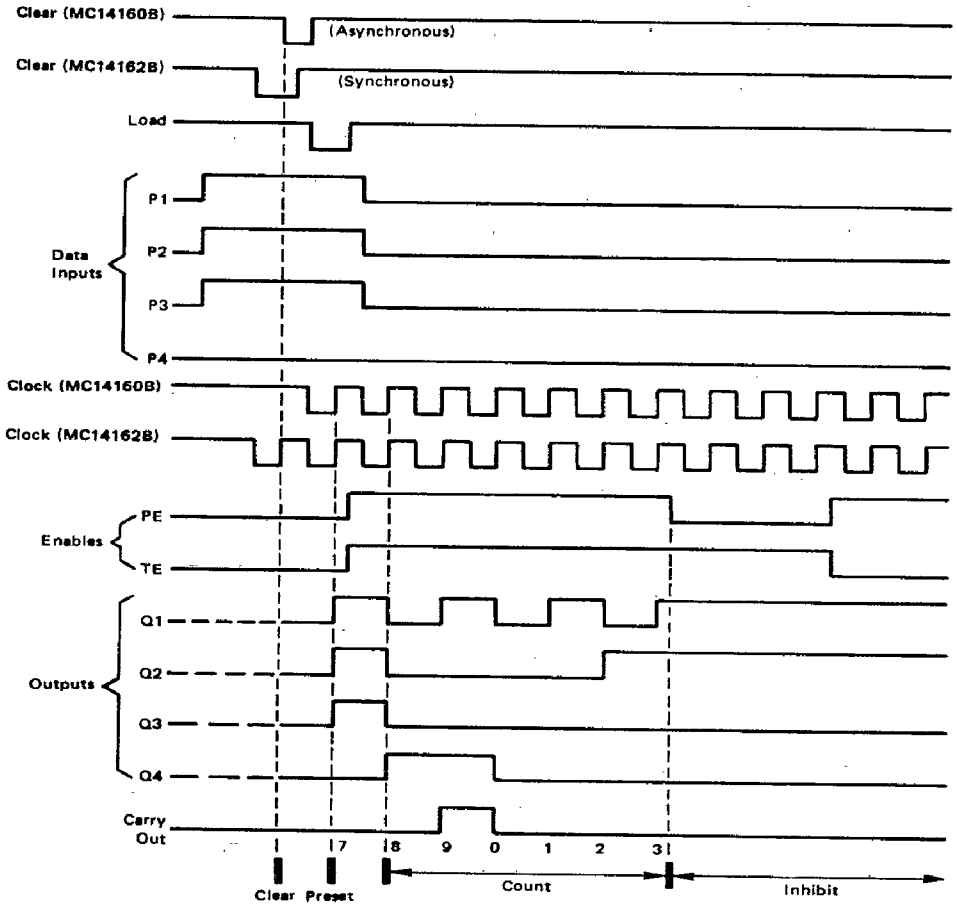
MC14160B, MC14162B LOGIC DIAGRAM
(Clear is synchronous for MC14162B)



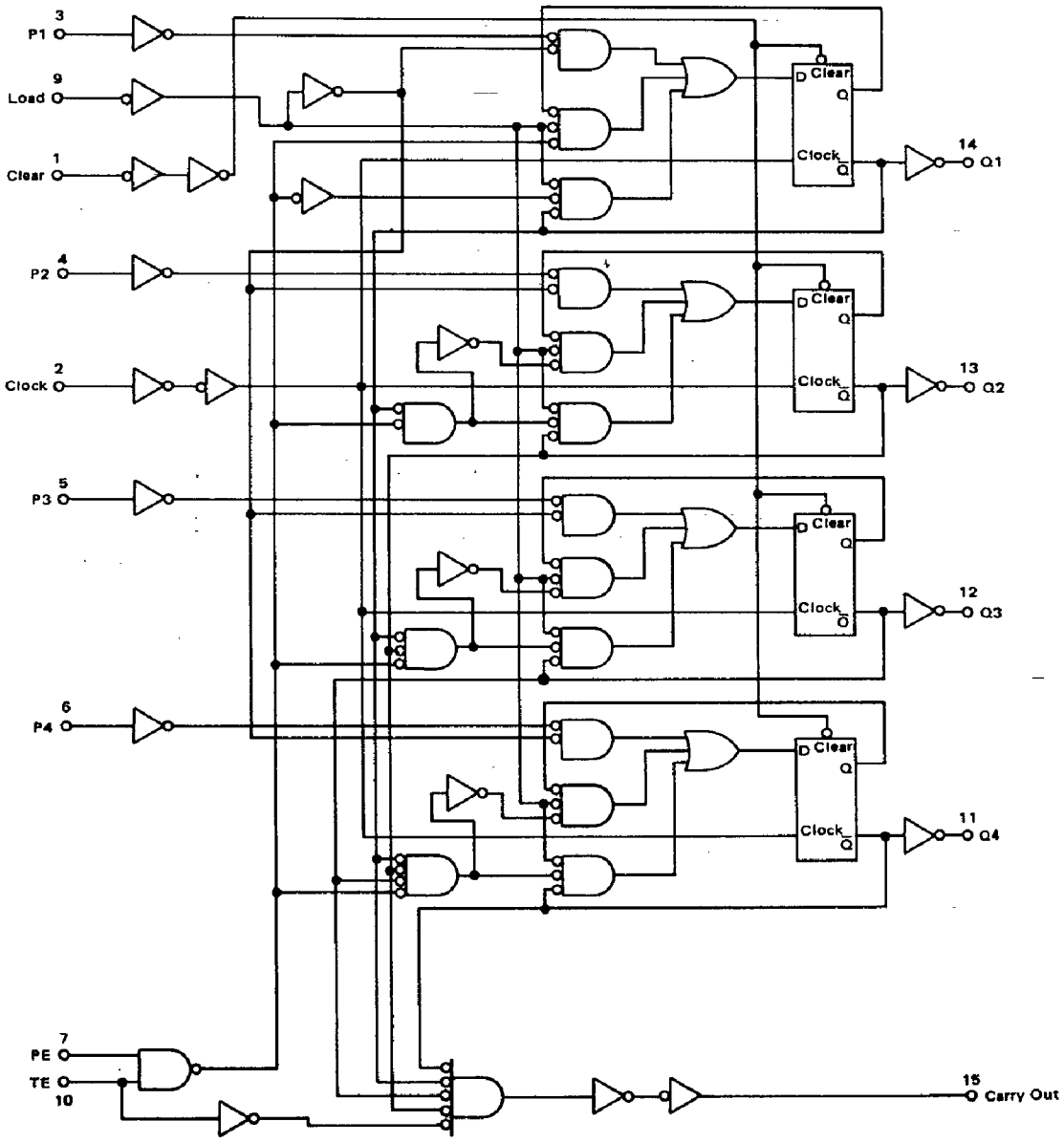
MC14160B, MC14162B TIMING DIAGRAM

Sequence illustrated in waveforms:

1. Clear outputs to zero.
2. Preset to BCD seven.
3. Count to eight, nine, zero, one, two, and three.
4. Inhibit



MC14161B, MC14163B LOGIC DIAGRAM
(Clear is Synchronous for MC14163B)



MC14161B, MC14163B TIMING DIAGRAM

Sequence illustrated in waveforms:

1. Clear outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one, and two.
4. Inhibit