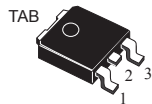
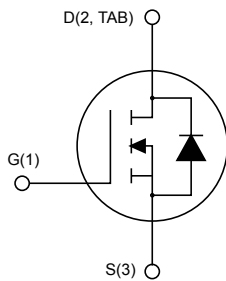


Automotive-grade N-channel 30 V, 38 mΩ typ., 17 A STripFET II Power MOSFET in a DPAK package




DPAK



AM01475v1_noZen

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STD18NF03L	30 V	< 50 mΩ	17 A

- AEC-Q101 qualified 
- Exceptional dv/dt capability
- 100% avalanche tested
- Low gate charge

Applications

- Switching applications

Description

This Power MOSFET has been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.



Product status link

[STD18NF03L](#)

Product summary

Order code	STD18NF03L
Marking	18NF03L
Package	DPAK
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0\text{ V}$)	30	V
V_{GS}	Gate-source voltage	± 16	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	17	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	12	A
$I_{DM}^{(1)}$	Drain current (pulsed)	68	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	30	W
	Derating Factor	0.2	W/ $^\circ\text{C}$
$dv/dt^{(2)}$	Peak diode recovery avalanche energy	7	V/ns
$E_{AS}^{(3)}$	Single pulse avalanche energy	200	mJ
T_{stg}	Storage temperature range	-55 to 175	$^\circ\text{C}$
T_J	Operating junction temperature range		

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 17\text{ A}$, $di/dt \leq 300\text{ A}/\mu\text{s}$, $V_{DD} = V_{(BR)DSS}$, $T_J \leq T_J\text{ max}$.
3. Starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = 8.5\text{ A}$, $V_{DD} = 15\text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	5.0	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-to ambient max	100	$^\circ\text{C}/\text{W}$
T_J	Maximum lead temperature for soldering purpose	275	$^\circ\text{C}$

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified

Table 3. On-/off-states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	30			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = \text{max rating}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = \text{max rating}$, $T_C = 125\text{ °C}$			10	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 16\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	1.0	1.5	2.2	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 8.5\text{ A}$		38	50	m Ω
		$V_{GS} = 5\text{ V}$, $I_D = 8.5\text{ A}$		45	60	

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., $I_D = 8.5\text{ A}$	-	12		S
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	320		pF
C_{oss}	Output capacitance		-	155		pF
C_{riss}	Reverse transfer capacitance		-	28		pF
Q_g	Total gate charge	$V_{DD} = 24\text{ V}$, $I_D = 17\text{ A}$	-	4.8	6.5	nC
Q_{gs}	Gate-source charge	$R_G = 4.7\text{ }\Omega$, $V_{GS} = 5\text{ V}$	-	2.25		nC
Q_{gd}	Gate-drain charge	(see Figure 14. Test circuit for gate charge behavior)	-	1.7		nC

1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%.

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15\text{ V}$, $I_D = 8.5\text{ A}$,	-	11		ns
t_r	Rise time	$R_G = 4.7\text{ }\Omega$, $V_{GS} = 5\text{ V}$	-	100		ns
$t_{d(off)}$	Turn-off delay time	(see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	25		ns
t_f	Fall time		-	22		ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		22	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		88	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 17\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 17\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$,	-	28		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 15\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$	-	18		nC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	1.3		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

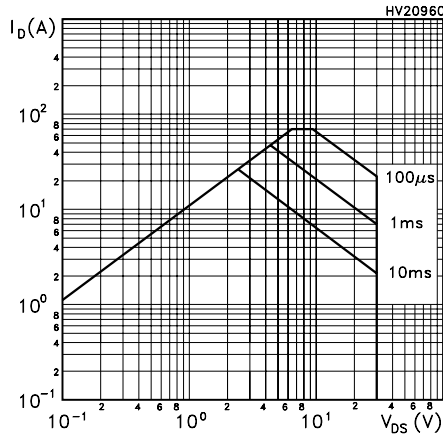


Figure 2. Thermal impedance

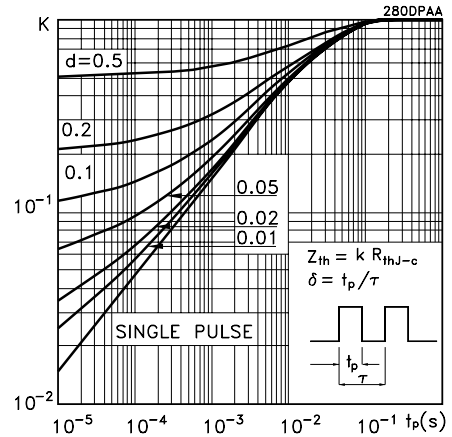


Figure 3. Output characteristics

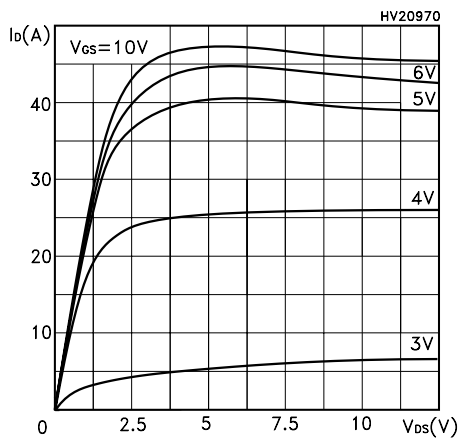


Figure 4. Transfer characteristics

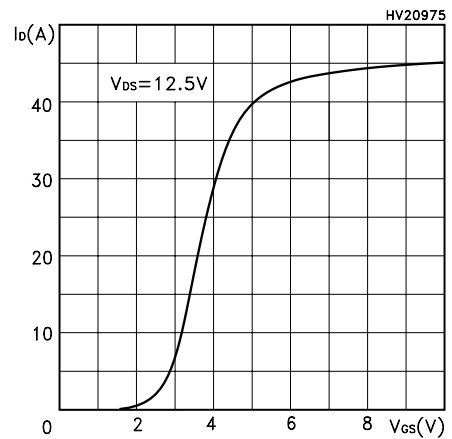


Figure 5. Transconductance

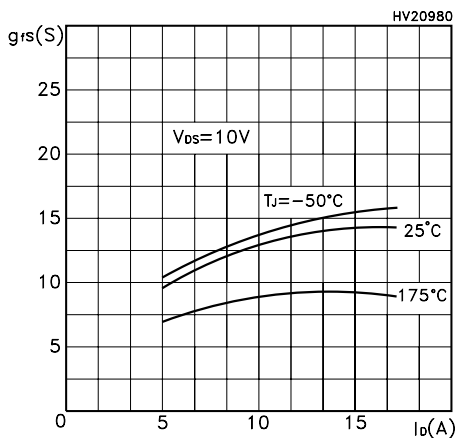


Figure 6. Static drain-source on resistance

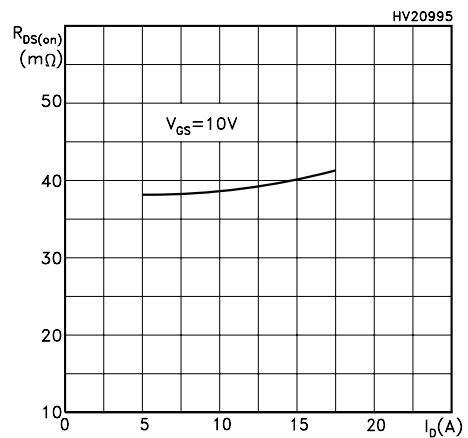


Figure 7. Gate charge vs. gate-source voltage

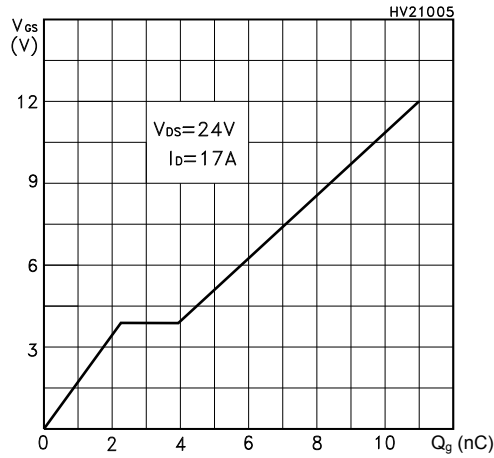


Figure 8. Capacitance variations

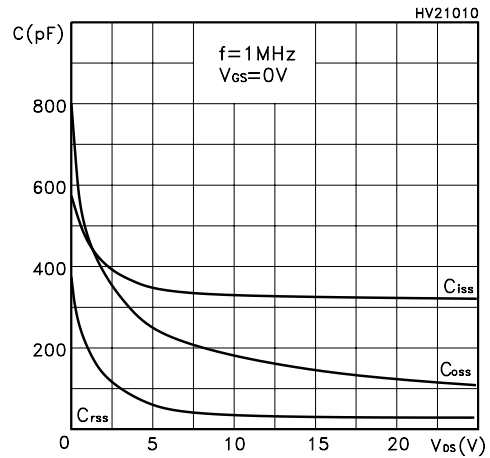


Figure 9. Normalized gate threshold voltage vs temperature

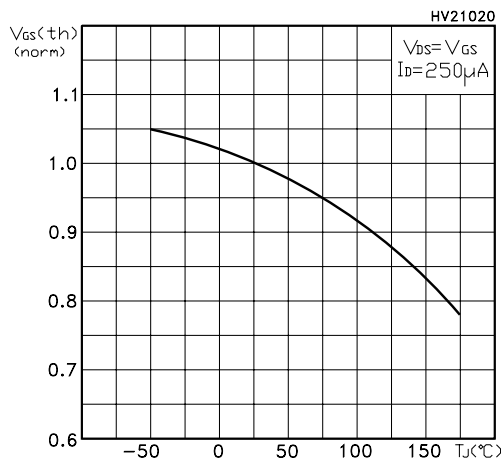


Figure 10. Normalized on resistance vs temperature

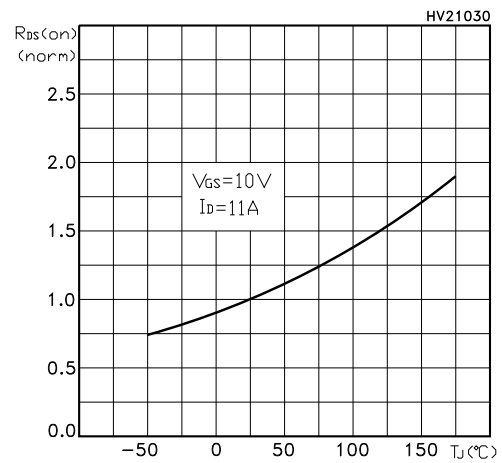


Figure 11. Source-drain diode forward characteristics

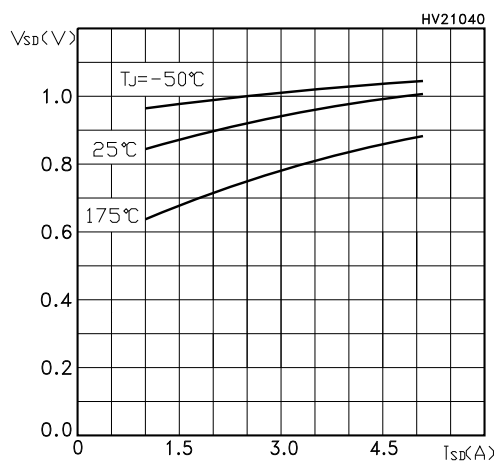
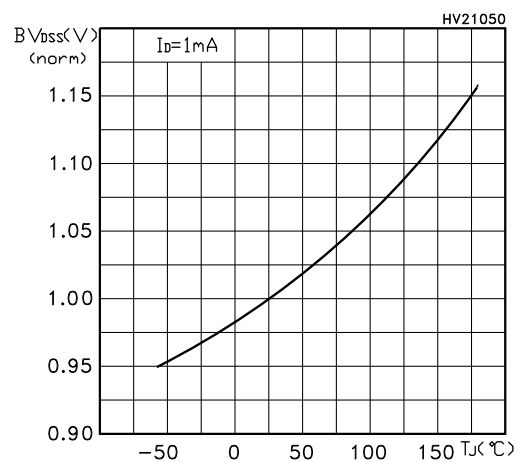
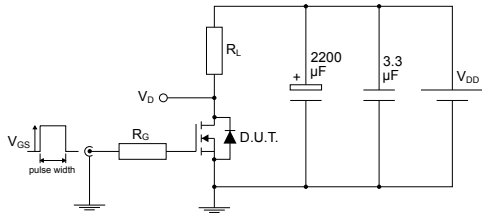


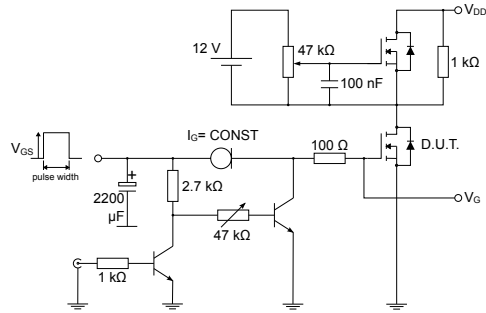
Figure 12. Normalized breakdown voltage vs temperature



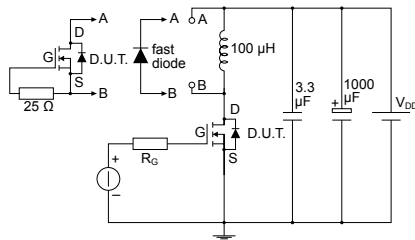
3 Test circuits

Figure 13. Test circuit for resistive load switching times


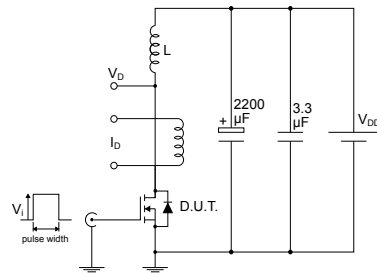
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Figure 14. Test circuit for gate charge behavior


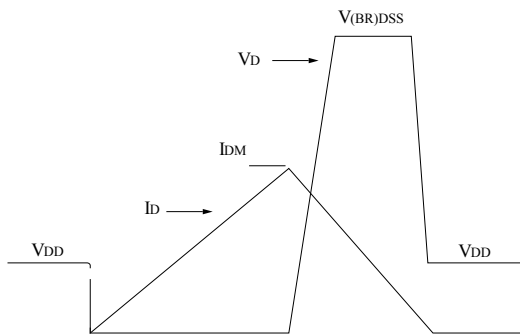
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Figure 15. Test circuit for inductive load switching and diode recovery times


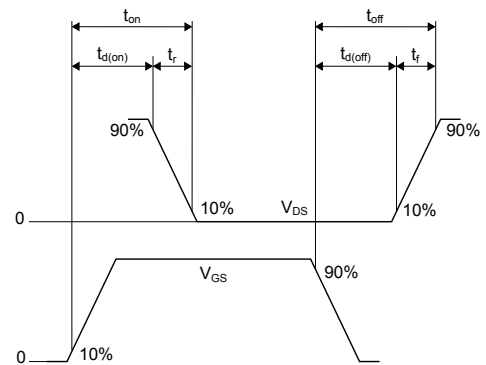
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Figure 16. Unclamped inductive load test circuit


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Figure 17. Unclamped inductive waveform


AM01472v1

Figure 18. Switching time waveform


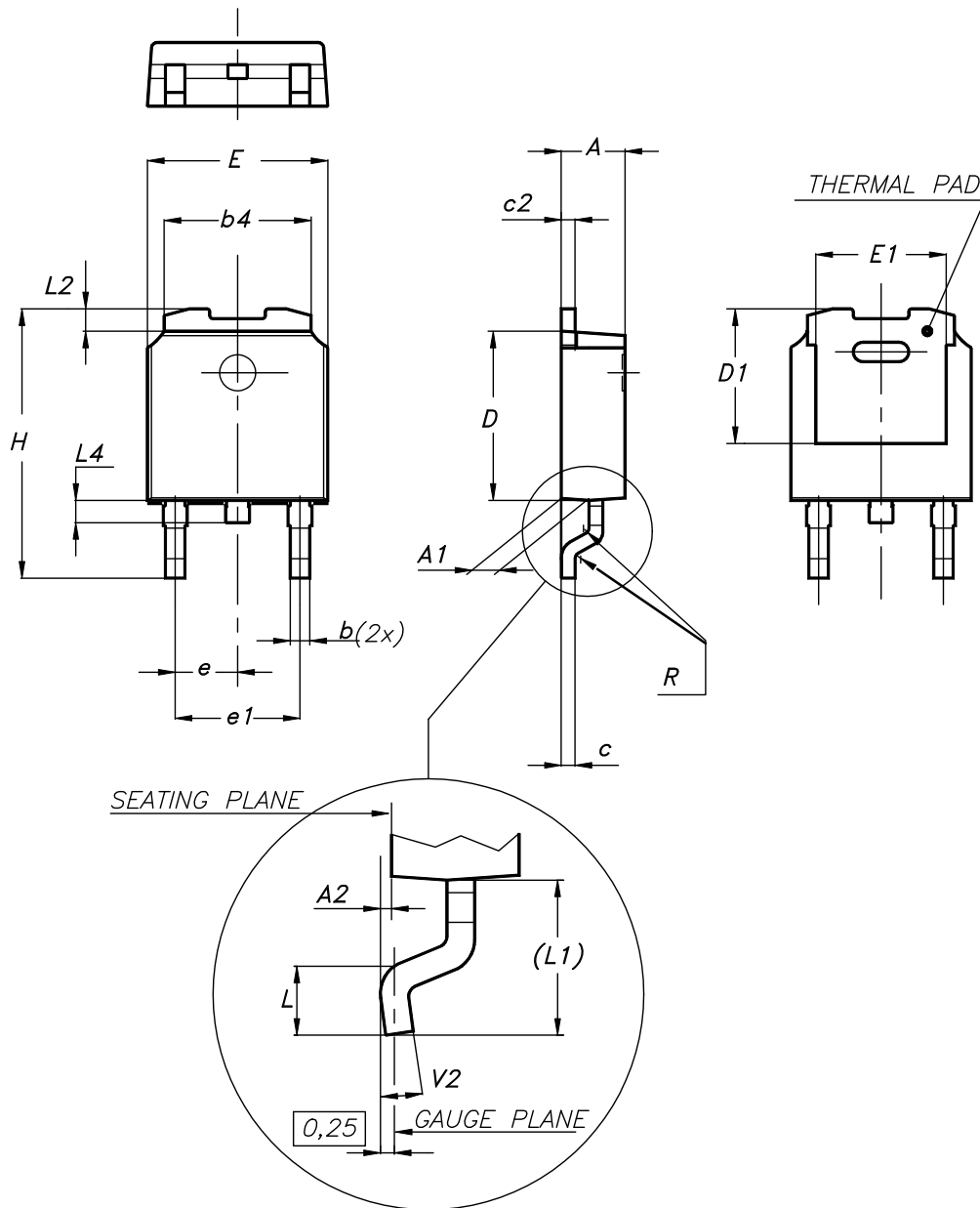
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 DPAK (TO-252) type A package information

Figure 19. DPAK (TO-252) type A package outline

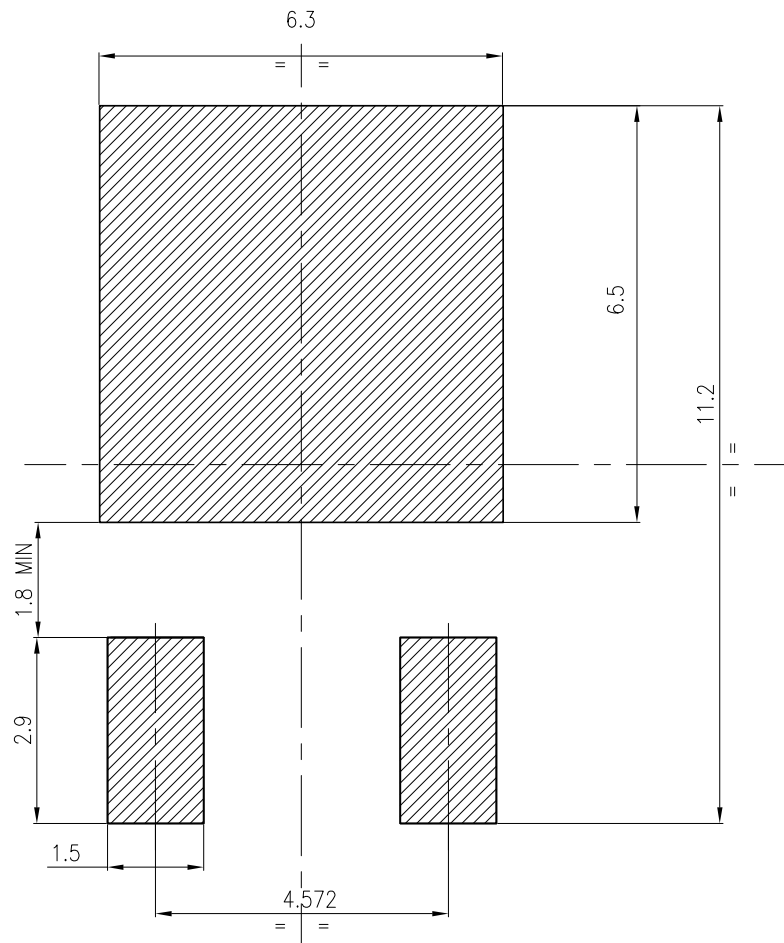


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Table 7. DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

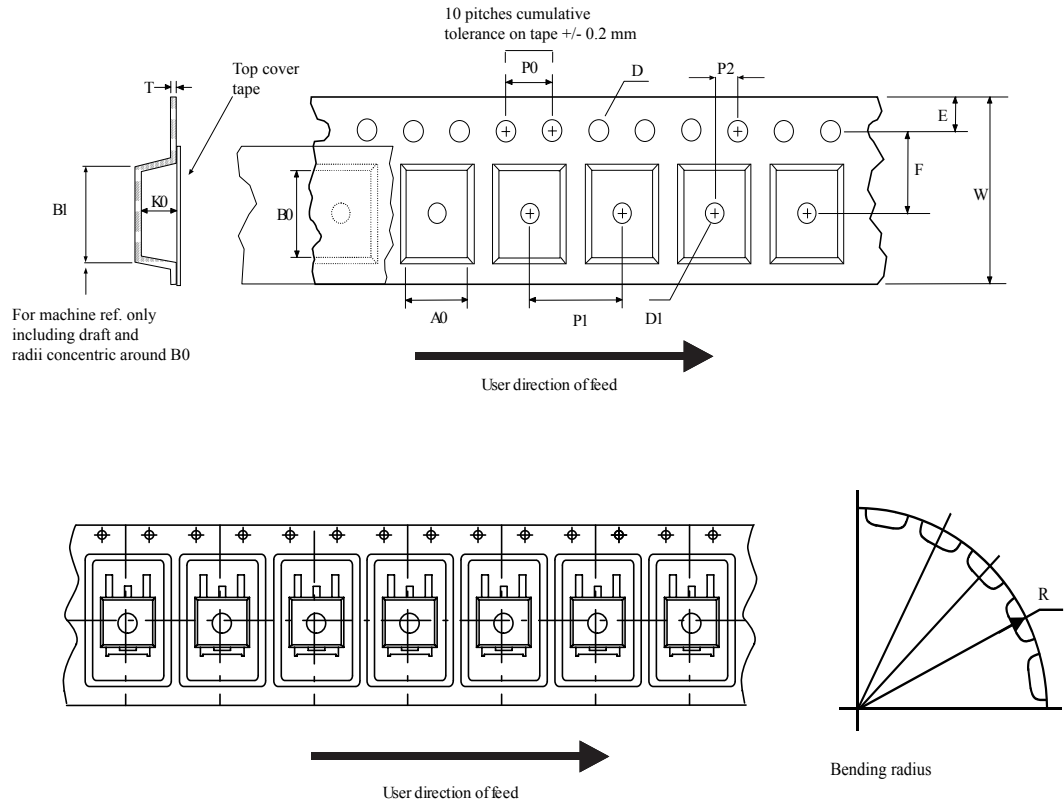
Figure 20. DPAK (TO-252) type A recommended footprint (dimensions are in mm)



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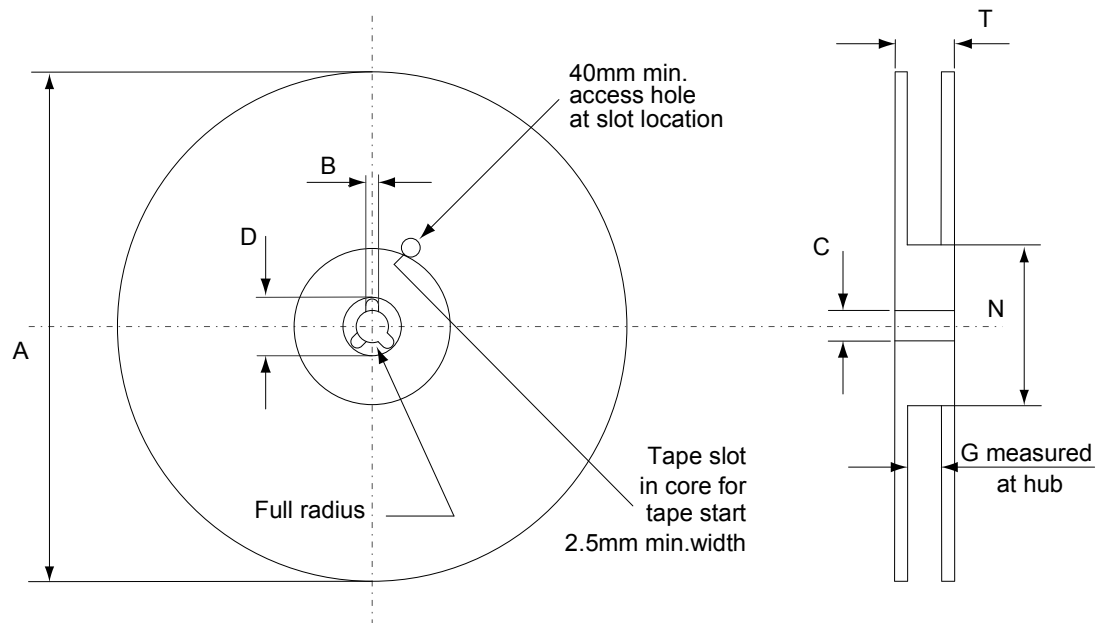
4.2 DPAK (TO-252) packing information

Figure 21. DPAK (TO-252) tape outline



AM08852v1

Figure 22. DPAK (TO-252) reel outline



AM06038v1

Table 8. DPAK (TO-252) tape and reel mechanical data

Dim.	Tape		Dim.	Reel	
	mm			mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1		Base qty.	2500
P1	7.9	8.1		Bulk qty.	2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Revision history

Table 9. Document revision history

Date	Version	Changes
27-Jul-2007	1	First release.
29-Apr-2020	2	Updated Title, Internal schematic , Features and Device summary in cover page. Minor text changes.

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