Integrated Device Technology, Inc.

HIGH-PERFORMANCE CMOS BUS INTERFACE LATCHES

IDT54/74FCT841A/B/C
IDT54/74FCT843A/B/C
IDT54/74FCT844A/B/C
IDT54/74FCT845A/B/C

T-52-09

FEATURES:

- Equivalent to AMD's Am29841-46 bipolar registers in pinout/function, speed and output drive over full temperature and voltage supply extremes
- IDT54/74FCT841A/843A/844A/845A equivalent to FAST™ speed
- **IDT54/74FCT841B/843B/844B/845B 25% faster than FAST**
- **IDT54/74FCT841C/843C/844C/845C 40% faster than FAST**
- Buffered common latch enable, clear and preset inputs
- I_{OL} = 48mA (commercial) and 32mA (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 series (5µA max.)
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

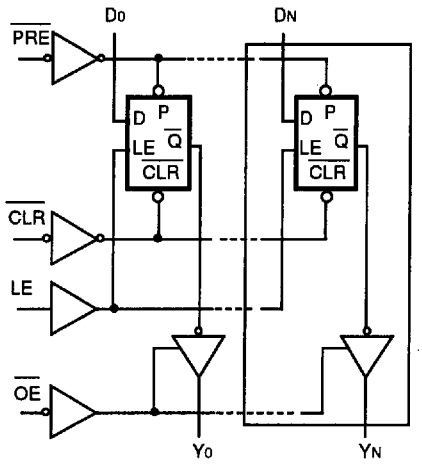
The IDT54/74FCT800 series is built using advanced CEMOS™, a dual metal CMOS technology.

The IDT54/74FCT840 series bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The IDT54/74FCT841 is a buffered, 10-bit wide version of the popular '373 function. The IDT54/74FCT843 and IDT54/74FCT844 are 9-bit wide buffered latches with Preset ($\overline{PRE}$) and Clear ($\overline{CLR}$)—ideal for parity bus interfacing in high-performance systems. The IDT54/74FCT845 is an 8-bit buffered latch with all the '843/4 controls, plus multiple enables ($\overline{OE_1}$, $\overline{OE_2}$, $\overline{OE_3}$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA and RD/$\overline{WR}$. It is ideal for use as an output port requiring high IOL/IOH.

All of the IDT54/74FCT800 high-performance interface family are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high-impedance state.

FUNCTIONAL BLOCK DIAGRAM

IDT54/74FCT841/843/845



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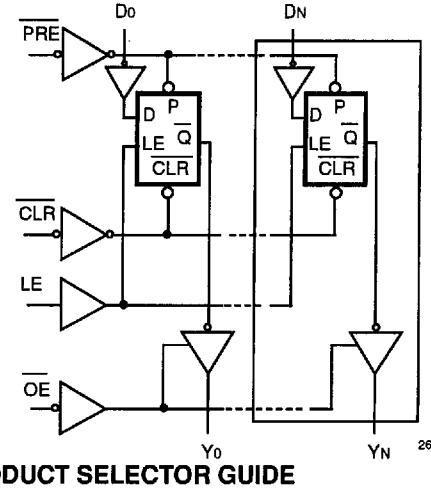
IDT54/74FCT844



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PRODUCT SELECTOR GUIDE

	Device		
	10-Bit	**9-Bit**	**8-Bit**
Non-Inverting	IDT54/74FCT841 A/B/C	IDT54/74FCT843 A/B/C	IDT54/74FCT845 A/B/C
Inverting		IDT54/74FCT844 A/B/C	

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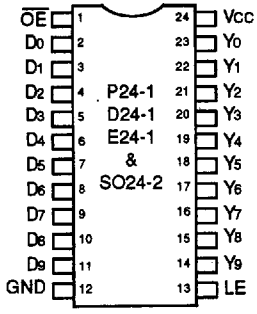
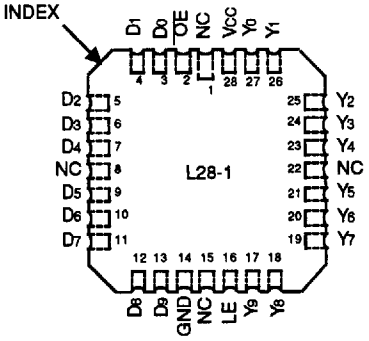
CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN CONFIGURATIONS

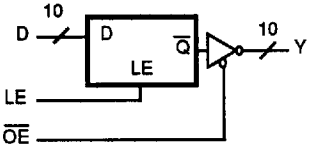
IDT54/74FCT841 10-BIT LATCH



DIP/CERPACK/SOIC
TOP VIEW



LCC
TOP VIEW



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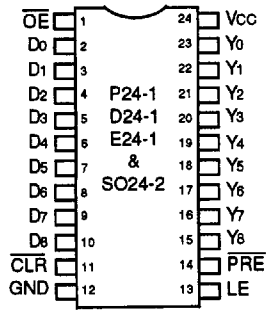
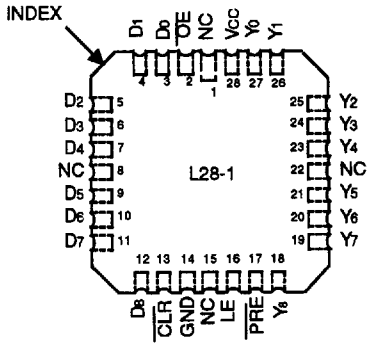
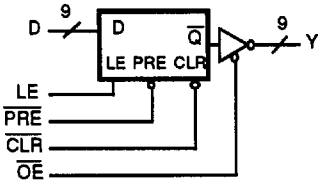
IDT54/74FCT843/844 9-BIT LATCHES



DIP/CERPACK/SOIC
TOP VIEW



LCC
TOP VIEW



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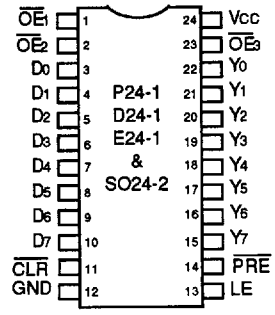
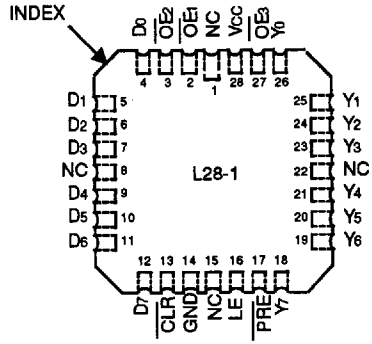
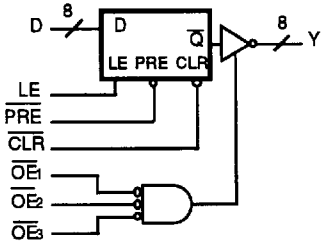
IDT54/74FCT845 8-BIT LATCH



DIP/CERPACK/SOIC
TOP VIEW



LCC
TOP VIEW



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PIN DESCRIPTION

Name	I/O	Description
IDT54/74FCT841/843/845 (Non-Inverting)		
$\overline{CLR}$	I	When $\overline{CLR}$ is low, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch.
D_I	I	The latch data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
Y_I	O	The 3-state latch outputs.
$\overline{OE}$	I	The output enable control. When $\overline{OE}$ is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs (Y_I) are in the high-impedance (off) state.
$\overline{PRE}$	I	Preset line. When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. Preset overrides $\overline{CLR}$
IDT54/74FCT844 (Inverting)		
$\overline{CLR}$	I	When $\overline{CLR}$ is low, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch.
D_I	I	The latch inverting data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
Y_I	O	The 3-state latch outputs.
$\overline{OE}$	I	The output enable control. When $\overline{OE}$ is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs (Y_I) are in the high-impedance (off) state.
$\overline{PRE}$	I	Preset line. When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. Preset overrides $\overline{CLR}$

2607 tbl 02

FUNCTION TABLE[1]
IDT54/74FCT841/843/845

Inputs					Internal	Outputs	
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D_I	Q_I	Y_I	Function
H	H	H	X	X	X	Z	High Z
H	H	H	H	L	L	Z	High Z
H	H	H	H	H	H	Z	High Z
H	H	H	L	X	NC	Z	Latched (High Z)
H	H	L	H	L	L	L	Transparent
H	H	L	H	H	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (High Z)
H	L	H	L	X	H	Z	Latched (High Z)

NOTE: 2607 tbl 03
1. H = HIGH, L = LOW, X = Don't Care, NC = No Change, Z = High Impedance

FUNCTION TABLE[1]
IDT54/74FCT844

Inputs					Inter-nal	Out-puts	
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D_I	Q_I	Y_I	Function
H	H	H	X	X	X	Z	High Z
H	H	H	H	H	L	Z	High Z
H	H	H	H	L	H	Z	High Z
H	H	H	L	X	NC	Z	Latched (High Z)
H	H	L	H	H	L	L	Transparent
H	H	L	H	L	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (High Z)
H	L	H	L	X	H	Z	Latched (High Z)

NOTE: 2607 tbl 04
1. H = HIGH, L = LOW, X = Don't Care, NC = No Change, Z = High Impedance

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE: 2607 tbl 05

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter (1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2607 tbl 06

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5(4)	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	–5(4)	
			V_I = GND	—	—	–5	
I_{OZH}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	10	µA
			V_O = 2.7V	—	—	10(4)	
I_{OZL}			V_O = 0.5V	—	—	–10(4)	
			V_O = GND	—	—	–10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		–75	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
			I_{OH} = –15mA MIL.	2.4	4.3	—	
			I_{OH} = –24mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}(4)	
			I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

NOTES: 2607 tbl 07

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

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POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND LE = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.0	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.2	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	5.2	14.5[5]	

2607 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter		Conditions[1]	FCT841A/843A-844A/845A				FCT841B/843B-844B/845B				FCT841C/843C-844C/845C				Unit
				Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
				Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
(FCT841, 843, 845) tPLH tPHL	Propagation Delay DI to YI (LE = HIGH)		CL = 50pF RL = 500Ω	1.5	9.0	1.5	10.0	1.5	6.5	1.5	7.5	1.5	5.5	1.5	6.3	ns
			CL = 300pF[4] RL = 500Ω	1.5	13.0	1.5	15.0	1.5	13.0	1.5	15.0	1.5	13.0	1.5	15.0	
(FCT844) tPLH tPHL	Propagation Delay DI to YI (LE = HIGH)		CL = 50pF RL = 500Ω	1.5	10.0	1.5	12.0	1.5	8.0	1.5	9.0	1.5	7.0	1.5	8.0	ns
			CL = 300pF[4] RL = 500Ω	1.5	13.0	1.5	15.0	1.5	13.0	1.5	15.0	1.5	13.0	1.5	15.0	
tPLH tPHL	Propagation Delay LE to YI		CL = 50pF RL = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	10.5	1.5	6.4	1.5	6.8	ns
			CL = 300pF[4] RL = 500Ω	1.5	16.0	1.5	20.0	1.5	15.5	1.5	18.0	1.5	15.0	1.5	16.0	
tPLH	Propagation Delay, $\overline{PRE}$ to YI		CL = 50pF RL = 500Ω	1.5	12.0	1.5	14.0	1.5	8.0	1.5	10.0	1.5	7.0	1.5	9.0	ns
tPHL				1.5	14.0	1.5	17.0	1.5	10.0	1.5	13.0	1.5	9.0	1.5	12.0	
tPHL	Propagation Delay, $\overline{CLR}$ to YI			1.5	13.0	1.5	14.0	1.5	10.0	1.5	11.0	1.5	9.0	1.5	10.0	ns
tPLH				1.5	14.0	1.5	17.0	1.5	10.0	1.5	10.0	1.5	9.0	1.5	9.0	
tPZH tPZL	Output Enable Time $\overline{OE}$ to YI		CL = 50pF RL = 500Ω	1.5	11.5	1.5	13.0	1.5	8.0	1.5	8.5	1.5	6.5	1.5	7.3	ns
			CL = 300pF[4] RL = 500Ω	1.5	23.0	1.5	25.0	1.5	14.0	1.5	15.0	1.5	12.0	1.5	13.0	
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to YI		CL = 5pF[4] RL = 500Ω	1.5	7.0	1.5	9.0	1.5	6.0	1.5	6.5	1.5	5.7	1.5	6.0	ns
			CL = 50pF RL = 500Ω	1.5	8.0	1.5	10.0	1.5	7.0	1.5	7.5	1.5	6.0	1.5	6.3	
tSU	Data to LE Set-up Time		CL = 50pF RL = 500Ω	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	ns
tH	Data to LE Hold Time			2.5	—	3.0	—	2.5	—	2.5	—	2.5	—	2.5	—	ns
tW	LE Pulse Width[3]	HIGH		4.0	—	5.0	—	4.0	—	4.0	—	4.0	—	4.0	—	ns
tW	$\overline{PRE}$ Pulse Width[3]	LOW		5.0	—	7.0	—	4.0	—	4.0	—	4.0	—	4.0	—	ns
tW	$\overline{CLR}$ Pulse Width[3]	LOW		4.0	—	5.0	—	4.0	—	4.0	—	4.0	—	4.0	—	ns
tREM	Recovery Time $\overline{PRE}$ to LE			4.0	—	4.0	—	4.0	—	4.0	—	4.0	—	4.0	—	ns
tREM	Recovery Time $\overline{CLR}$ to LE			3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns

2607 tbl 09

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed but not tested.
4. These conditions are guaranteed but not tested.

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