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April 1st, 2010 Renesas Electronics Corporation

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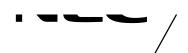
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DATA SHEET



MOS FIELD EFFECT TRANSISTOR NP50P06KDG

SWITCHING **P-CHANNEL POWER MOSFET**

DESCRIPTION

The NP50P06KDG is P-channel MOS Field Effect Transistor designed for high current switching applications.

ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE	
NP50P06KDG-E1-AY Note		Tara 000 alasal	TO-263 (MP-25ZK)	
NP50P06KDG-E2-AY Note	Pure Sn (Tin)	Tape 800 p/reel		

Note Pb-free (This product does not contain Pb in external electrode.)

FEATURES

• Super low on-state resistance

 $R_{DS(on)1} = 17 \text{ m}\Omega \text{ MAX.} (V_{GS} = -10 \text{ V}, I_{D} = -25 \text{ A})$

 $R_{DS(on)2} = 23 \text{ m}\Omega \text{ MAX.} \text{ (Vgs} = -4.5 \text{ V, Ip} = -25 \text{ A)}$

Low input capacitance

Ciss = 5000 pF TYP.

(TO-263)



ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (V _{GS} = 0 V)	Voss	-60	V
Gate to Source Voltage (VDS = 0 V)	Vgss	∓20	V
Drain Current (DC) (Tc = 25°C)	ID(DC)	∓50	Α
Drain Current (pulse) Note1	D(pulse)	∓150	Α
Total Power Dissipation (Tc = 25°C)	P _{T1}	90	W
Total Power Dissipation (T _A = 25°C)	P _{T2}	1.8	W
Channel Temperature	Tch	175	°C
Storage Temperature	Tstg	-55 to +175	°C
Single Avalanche Current Note2	las	32	Α
Single Avalanche Energy Note2	Eas	106	mJ

Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1%

2. Starting T_{ch} = 25°C, V_{DD} = -30 V, R_G = 25 Ω , V_{GS} = -20 \rightarrow 0 V

THERMAL RESISTANCE

Channel to Case Thermal Resistance °C/W $R_{th(ch-C)}$ 1.67 Channel to Ambient Thermal Resistance °C/W Rth(ch-A) 83.3

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ELECTRICAL CHARACTERISTICS (TA = 25°C)

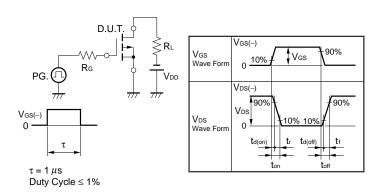
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V _{DS} = -60 V, V _{GS} = 0 V			-10	μΑ
Gate Leakage Current	Igss	V _{GS} = ∓20 V, V _{DS} = 0 V			∓100	nA
Gate to Source Threshold Voltage	V _{GS(th)}	V _{DS} = -10 V, I _D = -1 mA	-1.0	-1.6	-2.5	V
Forward Transfer Admittance Note	y _{fs}	V _{DS} = -10 V, I _D = -25 A	15	30		S
Drain to Source On-state Resistance Note	R _{DS(on)1}	V _{GS} = -10 V, I _D = -25 A		13.5	17	mΩ
	R _{DS(on)2}	V _{GS} = -4.5 V, I _D = -25 A		15.4	23	mΩ
Input Capacitance	Ciss	V _{DS} = -10 V,		5000		pF
Output Capacitance	Coss	V _{GS} = 0 V,		600		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		300		pF
Turn-on Delay Time	t _{d(on)}	$V_{DD} = -30 \text{ V}, I_D = -25 \text{ A},$		20		ns
Rise Time	tr	V _{GS} = -10 V,		45		ns
Turn-off Delay Time	t _{d(off)}	R _G = 0 Ω		405		ns
Fall Time	tr			270		ns
Total Gate Charge	Q _G	V _{DD} = -48 V,		95		nC
Gate to Source Charge	Q _{GS}	V _{GS} = -10 V,		10		nC
Gate to Drain Charge	Q _{GD}	I _D = -50 A		26		nC
Body Diode Forward Voltage Note	V _{F(S-D)}	I _F = -50 A, V _{GS} = 0 V		0.97	1.5	V
Reverse Recovery Time	trr	I _F = -50 A, V _{GS} = 0 V,		50		ns
Reverse Recovery Charge	Qrr	di/dt = -100 A/μs		70		nC

Note Pulsed test PW \leq 350 μ s, Duty Cycle \leq 2%

TEST CIRCUIT 1 AVALANCHE CAPABILITY

$V_{GS} = -20 \rightarrow 0 \text{ V}$ V_{DD} V_{DD}

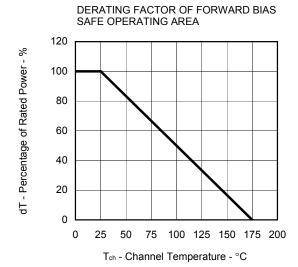
TEST CIRCUIT 2 SWITCHING TIME



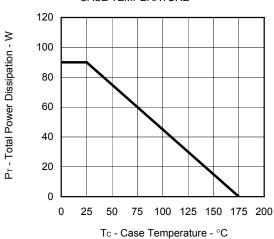
TEST CIRCUIT 3 GATE CHARGE

$$\begin{array}{c|c} D.U.T. & \\ \hline \\ IG = -2 \text{ mA} \\ \hline \\ PG. & \\ \hline \\ \end{array}$$

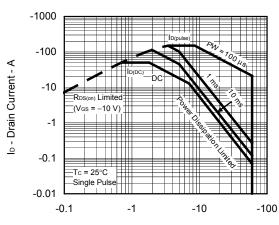
TYPICAL CHARACTERISTICS (TA = 25°C)



TOTAL POWER DISSIPATION vs. CASE TEMPERATURE

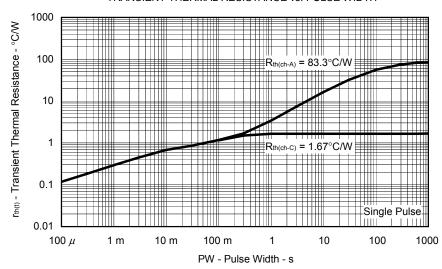


FORWARD BIAS SAFE OPERATING AREA

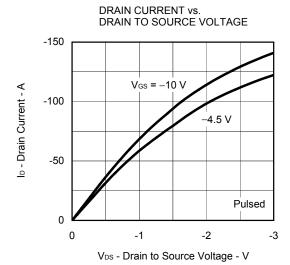


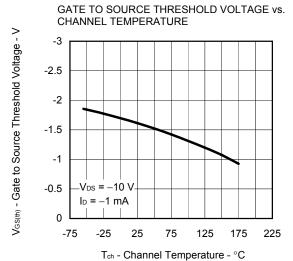
$V_{\text{\scriptsize DS}}$ - Drain to Source Voltage - V

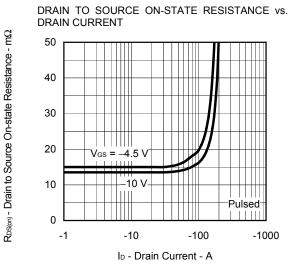
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



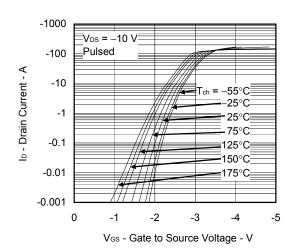
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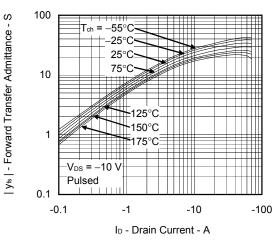




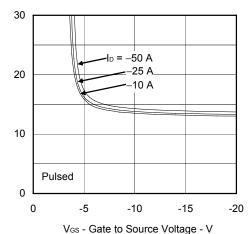
FORWARD TRANSFER CHARACTERISTICS



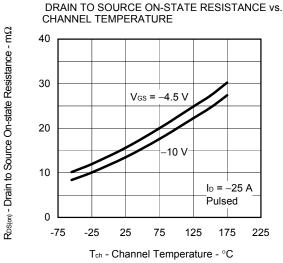
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

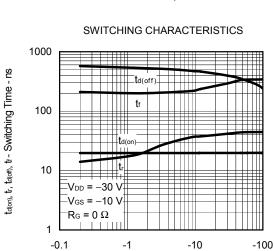


DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

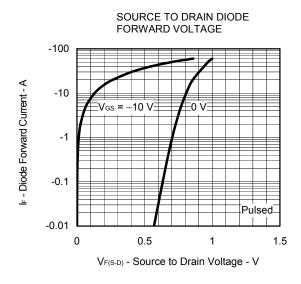


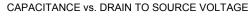
RDS(on) - Drain to Source On-state Resistance - mΩ

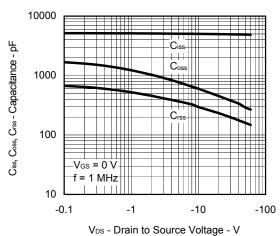




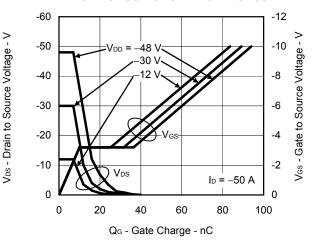
ID - Drain Current - A

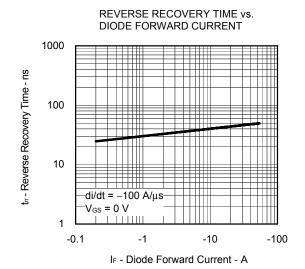






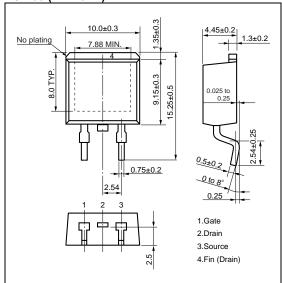
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



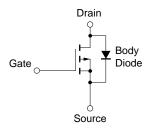


PACKAGE DRAWING (Unit: mm)

TO-263 (MP-25ZK)



EQUIVALENT CIRCUIT



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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NP50P06KDG

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