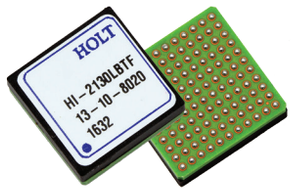
HOLT INTEGRATED CIRCUITS INC.

April 2021

HI-2130

Single Package MIL-STD-1553 / MIL-STD-1760 3.3V BC / MT / RT with Integrated Transformers



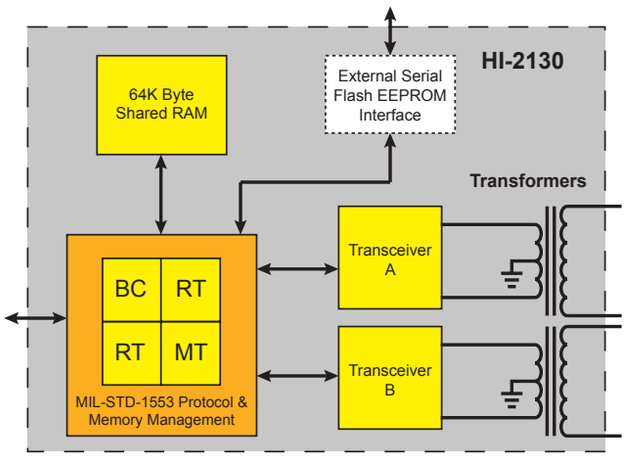
GENERAL DESCRIPTION

The HI-2130 provides a 3.3V fully integrated interface between a host processor and a MIL-STD-1553 / MIL-STD-1760 bus. It combines the functionality of Holt's HI-6130 16-bit parallel bus interface and HI-6131 SPI devices, integrating MIL-STD-1553 protocol logic, dual transceivers and dual transformers in a single compact 15 x 15 x 4.4 mm package; the smallest 1553 terminal solution with integrated magnetics in a single package. Both RoHS compliant and Sn/Pb configurations are available, giving customers a solution for tin-lead assemblies while avoiding expensive re-balling.

The device includes the entire signal I/O set of HI-6130 and HI-6131, with the addition of a new input signal for selecting parallel bus or SPI host interface. Two pairs of transformer output signals connect directly to the MIL-STD-1553 Bus A and Bus B stubs.

The part is available in Industrial -40°C to +85°C, or Extended, -55°C to +125°C temperature ranges.

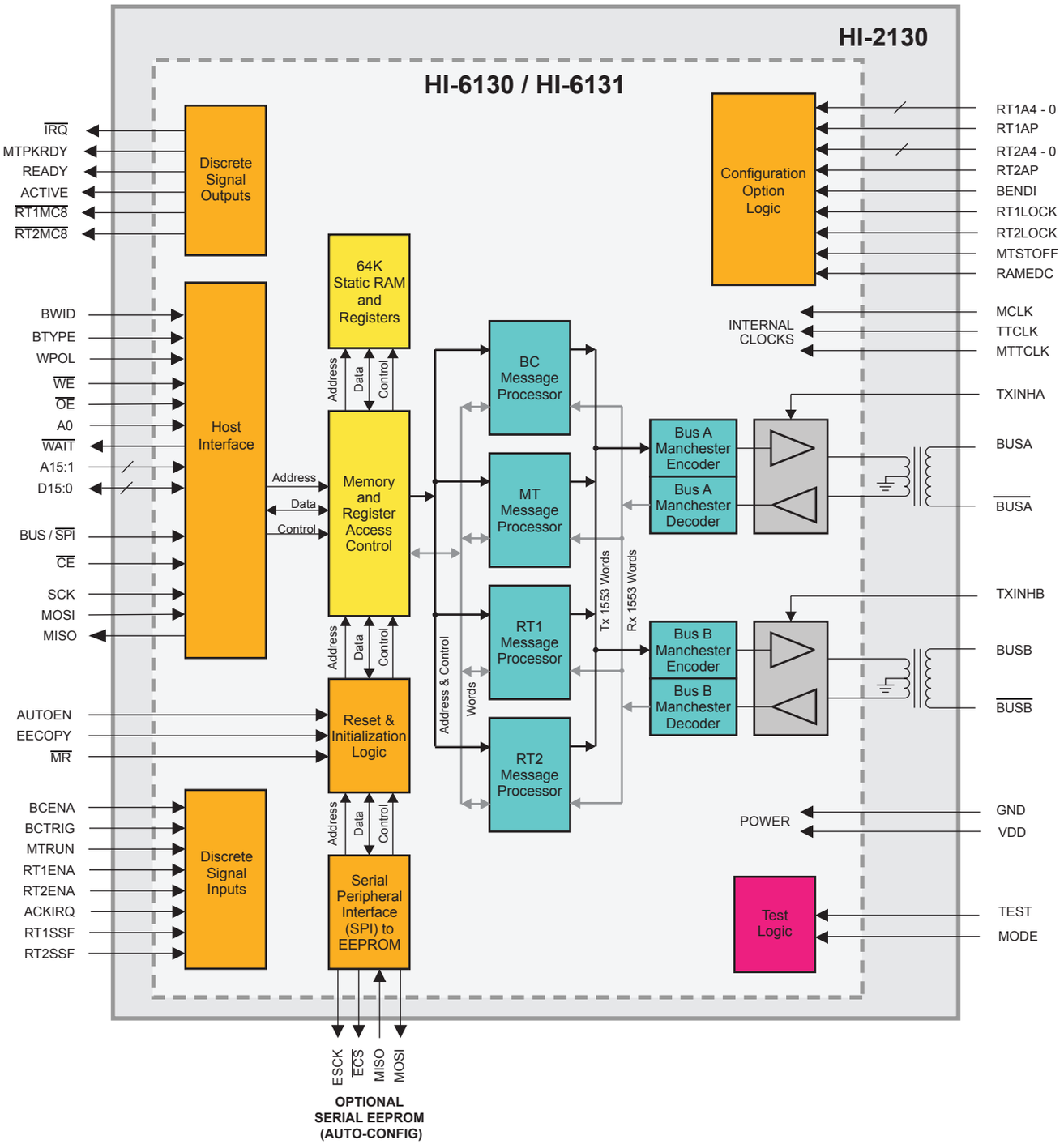
Refer to the HI-6130 datasheet for full functional description and operation.



FEATURES

- Combined functionality of HI-6130 and HI-6131 in a single package with integrated transformers
- Smallest footprint MIL-STD-1553 solution available (includes transformers)
- Low profile package solution suitable for PMC and XMC applications
- Extended temperature range, -55ºC to +125ºC
- Hermetically sealed die option (MSL 1) available
- Less expensive than traditional multi-chip modules
- DO-254 certifiable
- Concurrent multi-terminal operation (BC, MT, 1 or 2 independent RTs)
- Two host interface options in one package: 16-bit parallel bus or 4-wire SPI
- 64K bytes on-chip RAM with error detection/ correction option
- Autonomous terminal operation requires minimal host intervention
- Shared MIL-STD-1553 bus interface reduces circuit complexity and circuit board area.
- Fully programmable Bus Controller with 28 op code instruction set
- Simple Monitor Terminal (SMT) Mode records commands and data separately, with 16-bit or 48-bit time tagging
- IRIG Monitor Terminal (IMT) Mode supports IRIG-106 Chapter 10 packet format. Complete IRIG-106 data packets including full packet headers and trailers can be generated
- Independent time-tag counters for all terminals with 32-bit option for Bus Controller and 48-bit option for Monitor Terminal
- 64-Word Interrupt Log Buffer queues the most recent 32 interrupts. Hardware-assisted interrupt decoding quickly identifies interrupt sources
- Built-in self-test for protocol logic, digital signal paths and internal RAM
- Optional self-initialization at reset uses external serial EEPROM
- Two temperature ranges: -40°C to +85°C, or -55°C to +125°C

BLOCK DIAGRAM



PIN DIAGRAM

Top View

	11	10	9	8	7	6	5	4	3	2	1	
L	RAM EDC	DATA 14	DATA 11	DATA 9	DATA 4	RT1 SSF	MTPKT RDY	RT1 MC8	nIRQ	B TYPE	BENDI	L
K	nCE	DATA 12	DATA 10	AUTO EN	DATA 6	VDD	AC-TIVE	ACK IRQ	DATA 2	WPOL	nBUS A	K
J	MODE	BC TRIG	DATA 13	TX INHA	DATA 7	DATA 5	READY	TEST	DATA 0	DATA 1	nBUS A	J
H	MISO	DATA 15	MOSI	TX INHB	DATA 8	DATA 3	RT2 MC8	MTST OFF	RT1 LOCK	DNC	BUS A	H
G	nWAIT	SCLK	nOE	VDD	GND	VDD	GND	VDD	BC ENA	DNC	BUS A	G
F	nWE	BUS nSPI	MCLK	GND	VDD	GND	VDD	GND	VDD	DNC	DNC	F
E	RT1 A2	RT1 A0	RT1 A1	VDD	GND	VDD	GND	VDD	RT2 ENA	DNC	BUS B	E
D	nMR	RT1 A3	RT1 A4	ADDR 8	nECS	ADDR 10	RT2 LOCK	RT2 A0	RT2 A1	DNC	BUS B	D
C	ADDR 0	RT1 ENA	ADDR 2	E MOSI	GND	EE COPY	MT RUN	RT2 A2	RT2 A3	ADDR 14	nBUS B	C
B	ADDR 1	ADDR 3	ADDR 4	ADDR 6	TT CLK	VDD	ESCK	RT2 SSF	ADDR 13	ADDR 15	nBUS B	B
A	ADDR 5	RT1 AP	E MISO	ADDR 7	MTT CLK	ADDR 9	ADDR 11	RT2 AP	RT2 A4	ADDR 12	BWID	A
	11	10	9	8	7	6	5	4	3	2	1	

See HI-6130 datasheet for a full Pin Description.

Notes:

a. DNC: Do Not Connect.

b. All balls denoted VDD **must** be connected to 3.3V DC power.

c. All balls denoted GND **must** be connected to circuit ground.

d. BUS/nSPI (F10) selects 16-bit wide parallel bus or SPI operation (see Section “Selection of Host Interface” on page 4).

e. nCE: The chip enable signal is shared between 16-bit parallel and SPI host interfaces (SPI $\overline{\text{Slave Select}}$).

OPERATION

Refer to the HI-6130 datasheet for detailed operation and register description.

Selection of Host Interface

The host interface is selected using the SPI/$\overline{\text{BUS}}$ pin.

- BUS/$\overline{\text{SPI}}$ pin set to logic “1”: Selects 16-bit parallel bus host interface
- BUS/$\overline{\text{SPI}}$ pin reset to logic “0”: Selects SPI host interface

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Supply voltage (V_{DD})	-0.3 V to +5.0 V
Logic input voltage range	-0.3 V to +3.6 V
Receiver differential voltage	10 Vp-p
Solder Temperature (reflow)	245°C
Junction Temperature	175°C
Storage Temperature	-65°C to +150°C

Recommended Operating Conditions

Operating Supply voltage (V_{DD})	3.3 VDC ± 5%
Operating Temperature Range	
Industrial Extended	-40°C to +85°C -55°C to +125°C

NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

DC Electrical Characteristics

V_{DD} = 3.3V, GND = 0V, T_A = Operating Temperature Range (unless otherwise stated)

Parameters	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Operating Voltage	V_{DD}		3.15	3.3	3.45	V
Power Supply Current See Note 1 on next page	I_{CC1}	Not Transmitting	-	40	50	mA
	I_{CC2}	Continuous supply current while one bus transmits @ 100% duty cycle, 78Ω resistive load	-	720	760	mA
Power Dissipation See Note 2 on next page	PD_1	Not Transmitting	-	132	172	mW
	PD_2	Transmit one bus @ 100% duty cycle, 78Ω resistive load	-	0.85	1.04	W
Input Voltage (High)	V_{IH}	Digital Inputs	70%	-	-	V_{DD}
Input Voltage (Low)	V_{IL}	Digital Inputs	-	-	30%	V_{DD}
Input Current (High): inputs with pull-down.	I_{IH}	Digital Inputs (each digital input pulled high)	-	-	100	µA
Input Current (High): inputs with pull-up.	I_{IH}	Digital Inputs (each digital input pulled high)	+1	-	-	µA

Parameters		Symbol	Test Conditions	Limits			Unit
				Min	Typ	Max	
Input Current (Low) inputs with pull-up.		I_{IL}	Digital Inputs (each digital input pulled low)	-	-	-100	µA
Input Current (Low) inputs with pull-down.		I_{IL}	Digital Inputs (each digital input pulled low)	-1	-	-	µA
Output Voltage (High)		V_{OH}	I_{OUT} = -1.0mA, Digital outputs	90%	-	-	V_{DD}
Output Voltage (Low)		V_{OL}	I_{OUT} = 1.0mA, Digital outputs	-	-	10%	V_{DD}
RECEIVER (Measured at Point "AD" in Figure 7 unless otherwise specified)							
Input Resistance		R_{IN}	Differential	20	-	-	kΩ
Input Capacitance		C_{IN}	Differential	-	-	5	pF
Common Mode Rejection Ratio		CMRR		40	-	-	dB
Input Level		V_{IN}	Differential	-	-	9	Vp-p
Input Common Mode Voltage		V_{ICM}		-5	-	+5	V-pk
Threshold Voltage (Direct-Coupled)	Detect	V_{THD}	1 MHz Sine Wave (Measured at Point "AD" in Figure 7)	1.15	-	20.0	Vp-p
	No Detect	V_{THND}		-	-	0.28	Vp-p
Threshold Voltage (Transformer-Coupled)	Detect	V_{THD}	1 MHz Sine Wave (Measured at Point "AT" in Figure 8)	0.86	-	14.0	Vp-p
	No Detect	V_{THND}		-	-	0.2	Vp-p
TRANSMITTER (Measured at Point "AD" in Figure 7 unless otherwise specified)							
Output Voltage	Direct Coupled	V_{OUT}	35Ω Load	6.6	-	9.0	Vp-p
	Transformer Coupled	V_{OUT}	70Ω Load (Measured at Point "AT" in Figure 8)	20.0	-	27.0	Vp-p
Output Noise		V_{ON}	Differential, inhibited	-	-	10.0	mVp-p
Output Dynamic Offset Voltage	Direct Coupled	V_{DYN}	35Ω Load	-90	-	90	mV
	Transformer Coupled	V_{DYN}	70Ω Load (Measured at Point "AT" in Figure 8)	-250	-	250	mV
Output Resistance		R_{OUT}	Differential, not transmitting	10	-	-	kΩ
Output Capacitance		C_{OUT}	1 MHz sine wave	-	-	15	pF

Note 1: In actual use, the highest practical transmit duty cycle is 96%, occurring when a Remote Terminal responds to a series of 32 data word transmit commands (RT to BC) repeating with minimum intermessage gap of 4µs (2µs dead time) and typical RT response delay of 5µs.

Note 2: While one bus continuously transmits, the power delivered by the 3.3V power supply is 3.3V × 720mA typical = 2.4W. Of this, 850mW is dissipated in the device, the remainder in the load.

AC Electrical Characteristics — SPI Host Interface Timing

V_{DD} = 3.3V, GND = 0V, T_A = Operating Temperature Range (unless otherwise stated)

Parameters	Symbol	Limits			Units
		Min	Typ	Max	
HI-6131 INTERFACE TIMING (SPI Host Bus Interface)					
SCK clock Period	t_{CYC}	50	-	-	ns
$\overline{CE}$ set-up time to first SCK rising edge	t_{CES}	25	-	-	ns
$\overline{CE}$ hold time after last SCK rising edge	t_{CEH}	25	-	-	ns
$\overline{CE}$ inactive between SPI instructions	t_{CPH}	100	-	-	ns
SPI SI Data set-up time to SCK rising edge	t_{DS}	10	-	-	ns
SPI SI Data hold time after SCK rising edge	t_{DH}	10	-	-	ns
SO valid after SCK falling edge	t_{DV}	-	-	20	ns
SO high-impedance after $\overline{CE}$ inactive	t_{CHZ}	-	-	75	ns

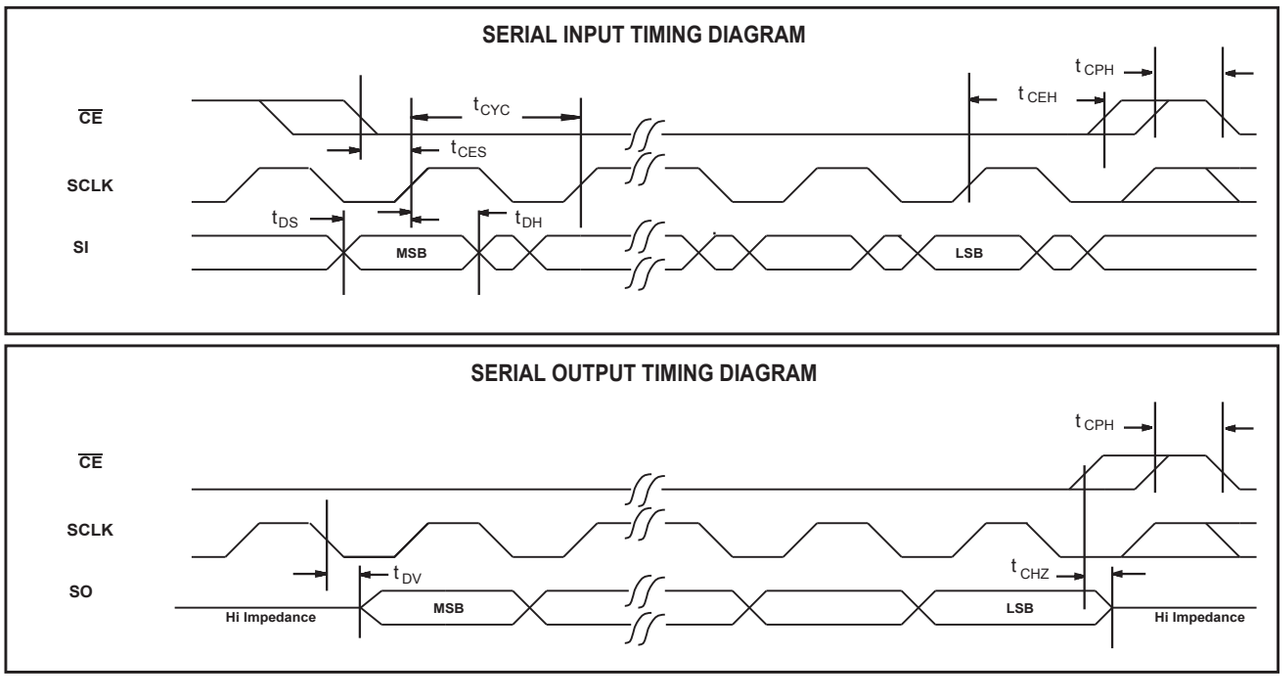


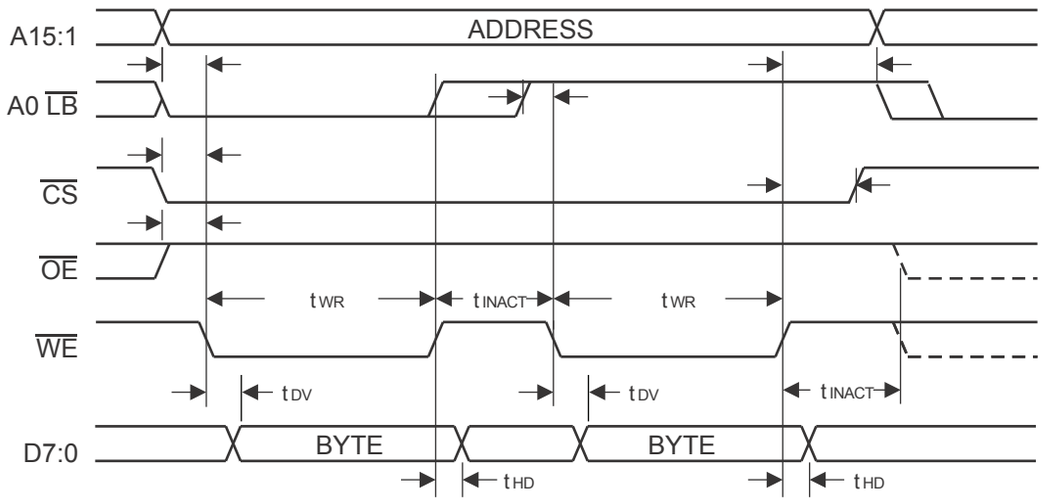
Figure 1. HI-2130 Host Bus Interface Timing Diagram

AC Electrical Characteristics — 16-Bit Parallel Bus Host Interface Timing

Parameters	Symbol	Limits			Units
		Min	Typ	Max	
WRITE TIMING					
Write strobe	t_{WR}	55	-	-	ns
Write inactive time	t_{INACT}	25	-	-	ns
Write data available	t_{DV}	-	-	20	ns
Write cycle, $t_{WR} + t_{INACT}$	-	80	-	-	ns
READ TIMING					
Wait assertion time	t_{WAS}	-	-	20	ns
Wait time	t_{W}	-	-	110	ns
Read strobe, sequential address, 8-bit bus mode	t_{SR8}	55	-	-	ns
Read strobe, sequential address, 16-bit bus mode	t_{SR16}	55	-	-	ns
Read strobe, non-sequential address	t_{NSR}	130	-	-	ns
Read inactive time	t_{INACT}	25	-	-	ns
Read access time1	t_{RA1}	-	-	130	ns
Read access time2	t_{RA2}	-	-	55	ns
Read cycles in 8-bit bus mode (see note below)					
Read cycle, sequential address, 16-bit word, 8-bit bus mode, $t_{SR8} + t_{INACT} + t_{SR8} + t_{INACT}$	-	160	-	-	ns
Read cycle, non-sequential address, 8-bit bus mode, $t_{WAS} + t_{W} + t_{INACT} + t_{SR8}$	-	-	-	210	ns
Read cycles in 16-bit bus mode (see note below)					
Read cycle, sequential address, 16-bit bus mode, $t_{SR16} + t_{INACT}$	-	80	-	-	ns
Read cycle, non-sequential address, 16-bit bus mode, $t_{WAS} + t_{W}$	-	-	-	130	ns

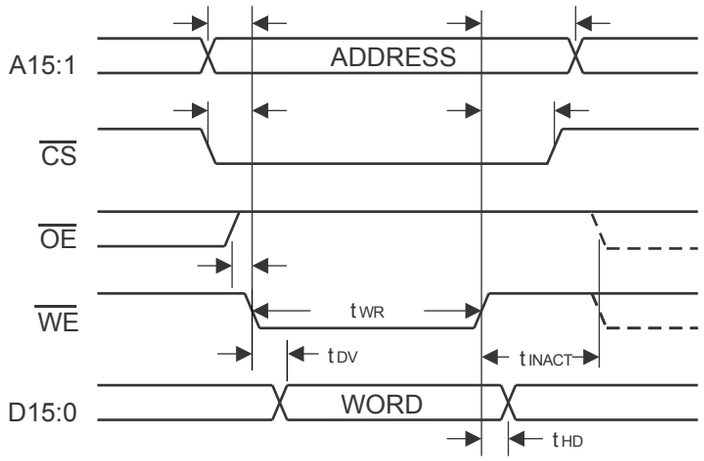
NOTE: When reading a series of sequential addresses, the read cycle for the first word (or byte) location is always longer because the HI-6130 asserts the WAIT output. As long as sequential addresses are then read, automatic prefetch speeds up read access for following words (or bytes) since these occur without WAIT assertion.

HOST WRITE IN DUAL-BYTE MODE (8-BIT BUS WIDTH)
using BTYPE = 1 (“Intel Style” - $\overline{OE}$ Output Enable and $\overline{WE}$ Write Enable)
showing 2 bytes written for a single 16-bit word



All timing intervals equal 0 ns MIN unless otherwise indicated.
The WAIT output is inactive during write access

HOST WRITE IN WORD MODE (16-BIT BUS WIDTH)
using BTYPE = 1 (“Intel Style” - $\overline{OE}$ Output Enable and $\overline{WE}$ Write Enable)
showing a one-word write cycle. Successive writes to sequential addresses have same timing.



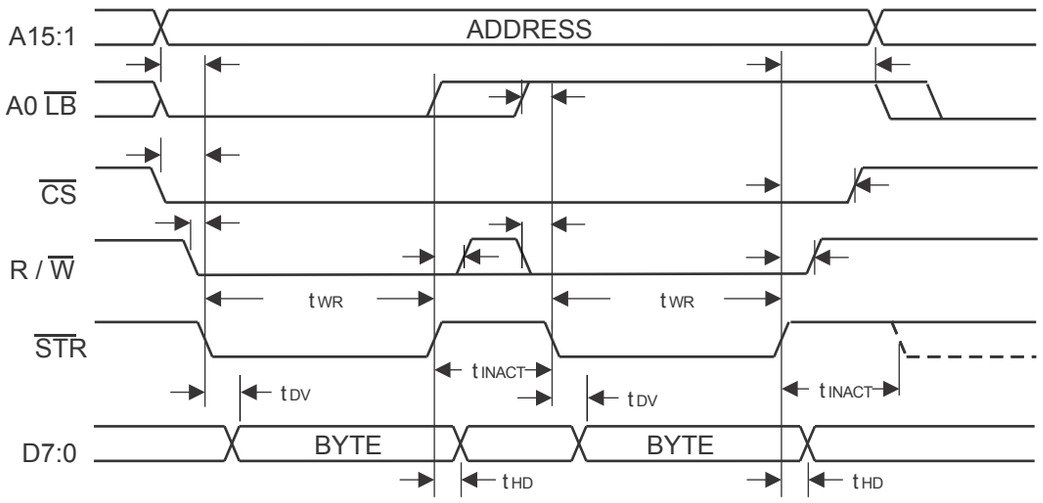
All timing intervals equal 0 ns MIN unless otherwise indicated.
The WAIT output is inactive during write access

Figure 2. Register and RAM Write Operations for BTYPE = 1

HOST WRITE IN DUAL-BYTE MODE (8-BIT BUS WIDTH)

using BTYPE = 0 (”Motorola Style” - Single Read/Write Strobe $\overline{STR}$ and R/$\overline{W}$ Direction Select)

showing 2 bytes written for a single 16-bit word

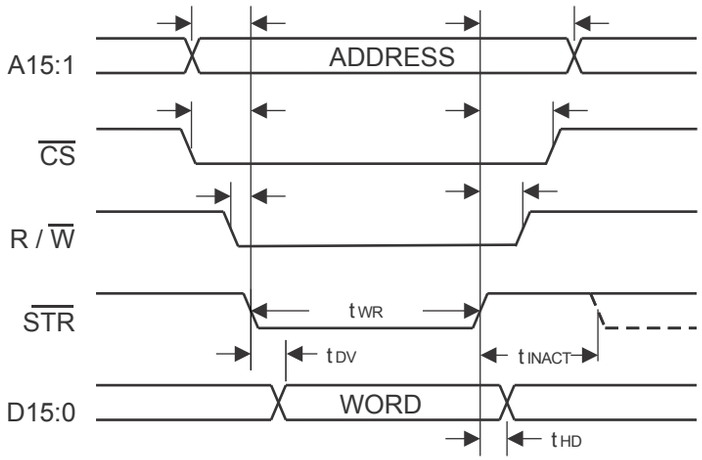


All timing intervals equal 0 ns MIN unless otherwise indicated.
The WAIT output is inactive during write access

HOST WRITE IN WORD MODE (16-BIT BUS WIDTH)

using BTYPE = 0 (”Motorola Style” - Single Read/Write Strobe $\overline{STR}$ and R/$\overline{W}$ Direction Select)

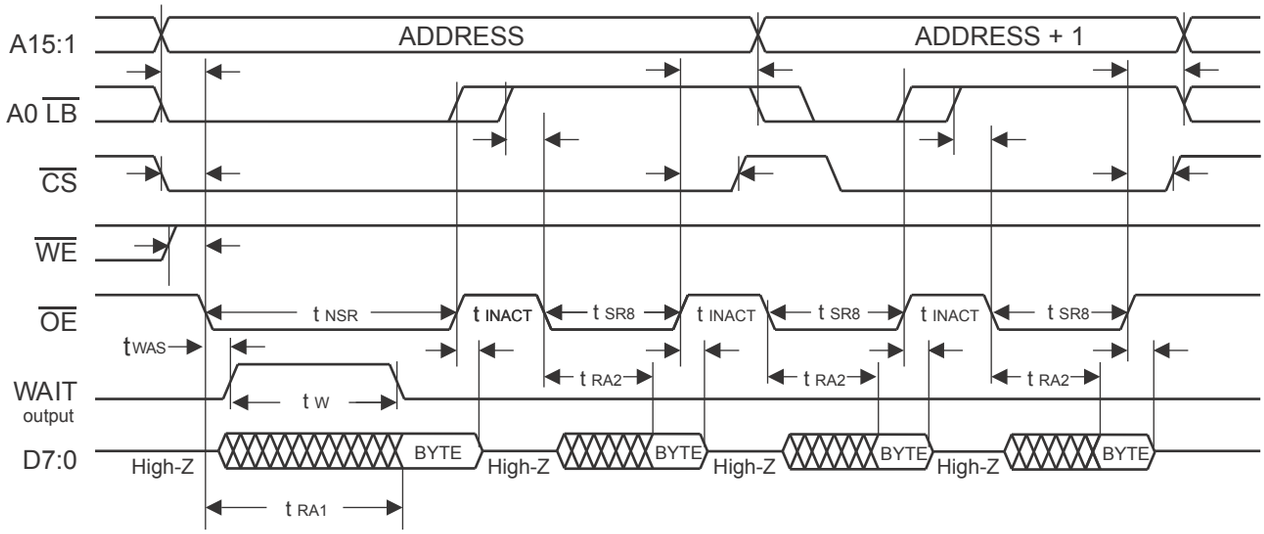
showing a one-word write cycle. Successive writes to sequential addresses have same timing.



All timing intervals equal 0 ns MIN unless otherwise indicated.
The WAIT output is inactive during write access

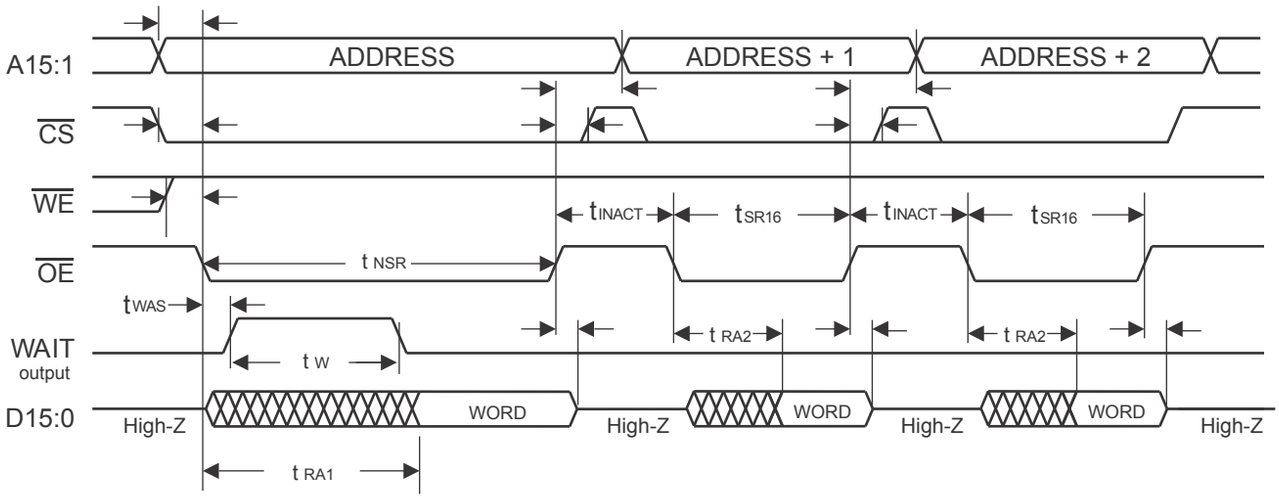
Figure 3. Register and RAM Write Operations for BTYPE = 0

HOST READ IN DUAL-BYTE MODE (8-BIT BUS WIDTH)
using BTYPE = 1 (”Intel Style” - $\overline{OE}$ Output Enable and $\overline{WE}$ Write Enable)
showing two successive 16-bit words (4 bytes) read from sequential addresses



All timing intervals equal 0 ns MIN unless otherwise indicated.

HOST READ IN WORD MODE (16-BIT BUS WIDTH)
using BTYPE = 1 (”Intel Style” - $\overline{OE}$ Output Enable and $\overline{WE}$ Write Enable)
showing a three word read access from sequential addresses

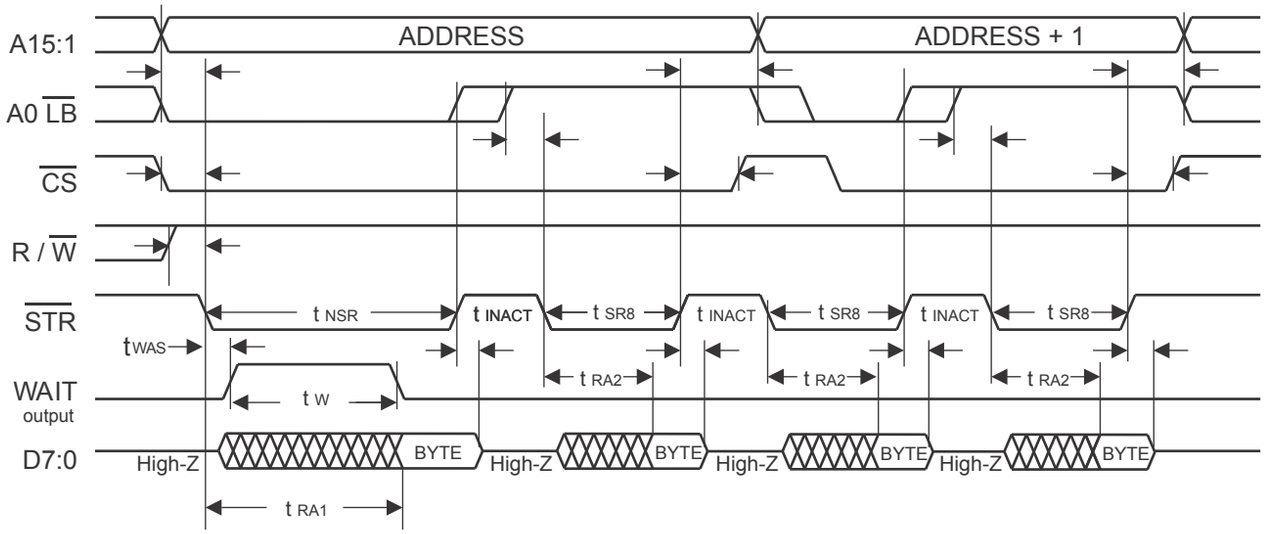


All timing intervals equal 0 ns MIN unless otherwise indicated.

After first byte or word is read, prefetch allows faster access times for successive reads, as long as read addresses are sequential.

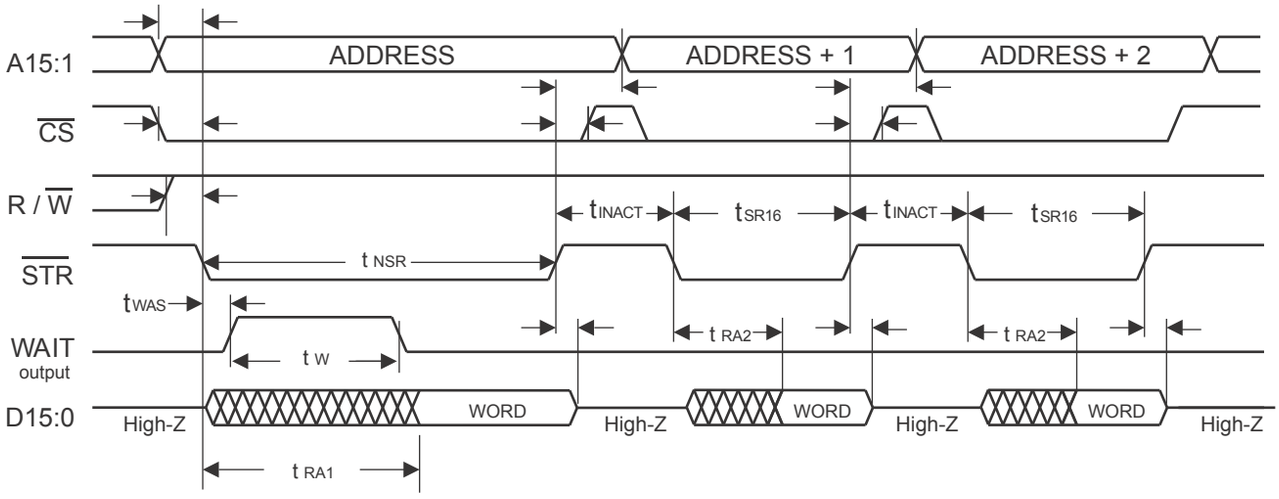
Figure 4. Register and RAM Read Operations for BTYPE = 1

HOST READ IN DUAL-BYTE MODE (8-BIT BUS WIDTH)
using BTYPE = 0 (”Motorola Style” - Single Read/Write Strobe $\overline{STR}$ and R/$\overline{W}$ Direction Select)
showing two successive 16-bit words (4 bytes) read from sequential addresses



All timing intervals equal 0 ns MIN unless otherwise indicated.

HOST READ IN WORD MODE (16-BIT BUS WIDTH)
using BTYPE = 0 (”Motorola Style” - Single Read/Write Strobe $\overline{STR}$ and R/$\overline{W}$ Direction Select)
showing a three word read access from sequential addresses



All timing intervals equal 0 ns MIN unless otherwise indicated.

After first byte or word is read, prefetch allows faster access times for successive reads, as long as read addresses are sequential.

Figure 5. Register and RAM Read Operations for BTYPE = 0

MIL-STD-1553 BUS INTERFACE

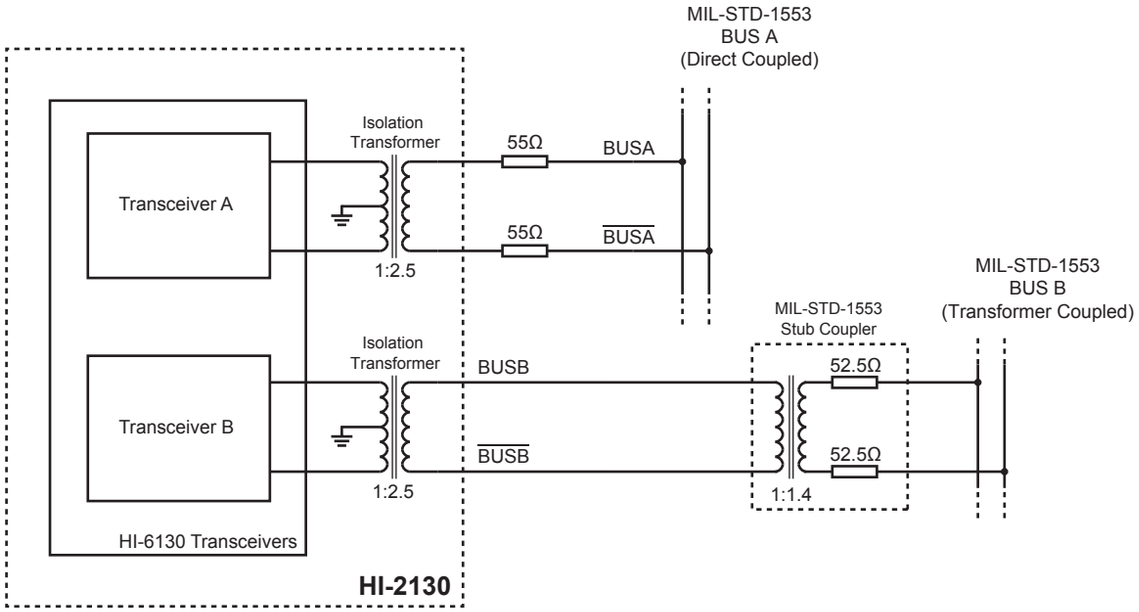


Figure 6. Bus Connection Example using HI-2130

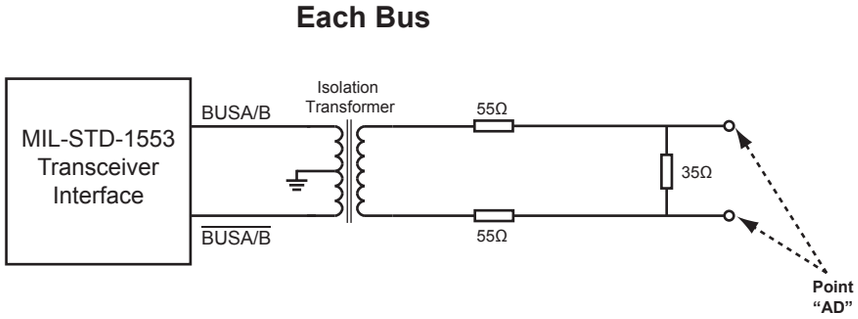


Figure 7. MIL-STD-1553 Direct Coupled Test Circuit Example

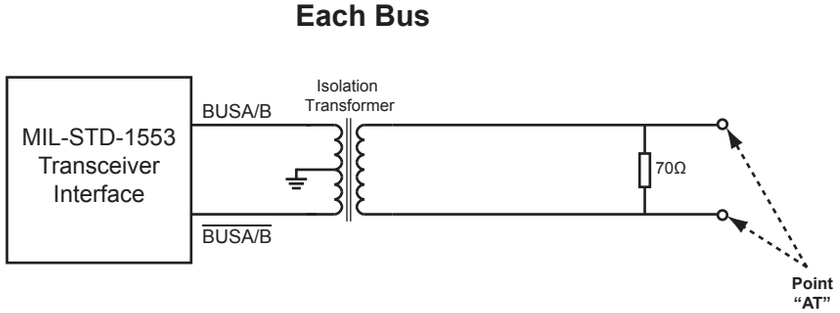
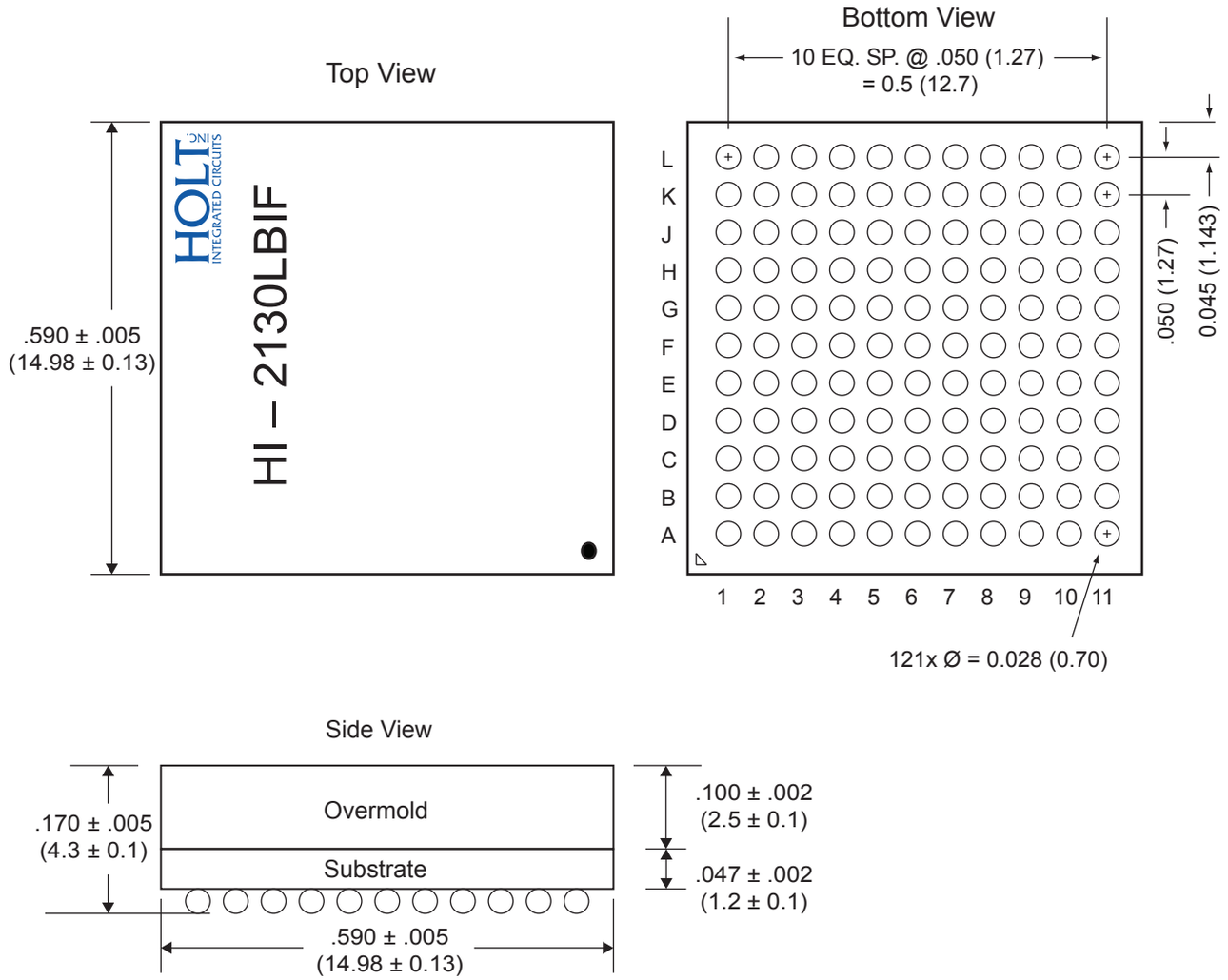


Figure 8. MIL-STD-1553 Transformer Coupled Test Circuit Example

PACKAGE DIMENSIONS

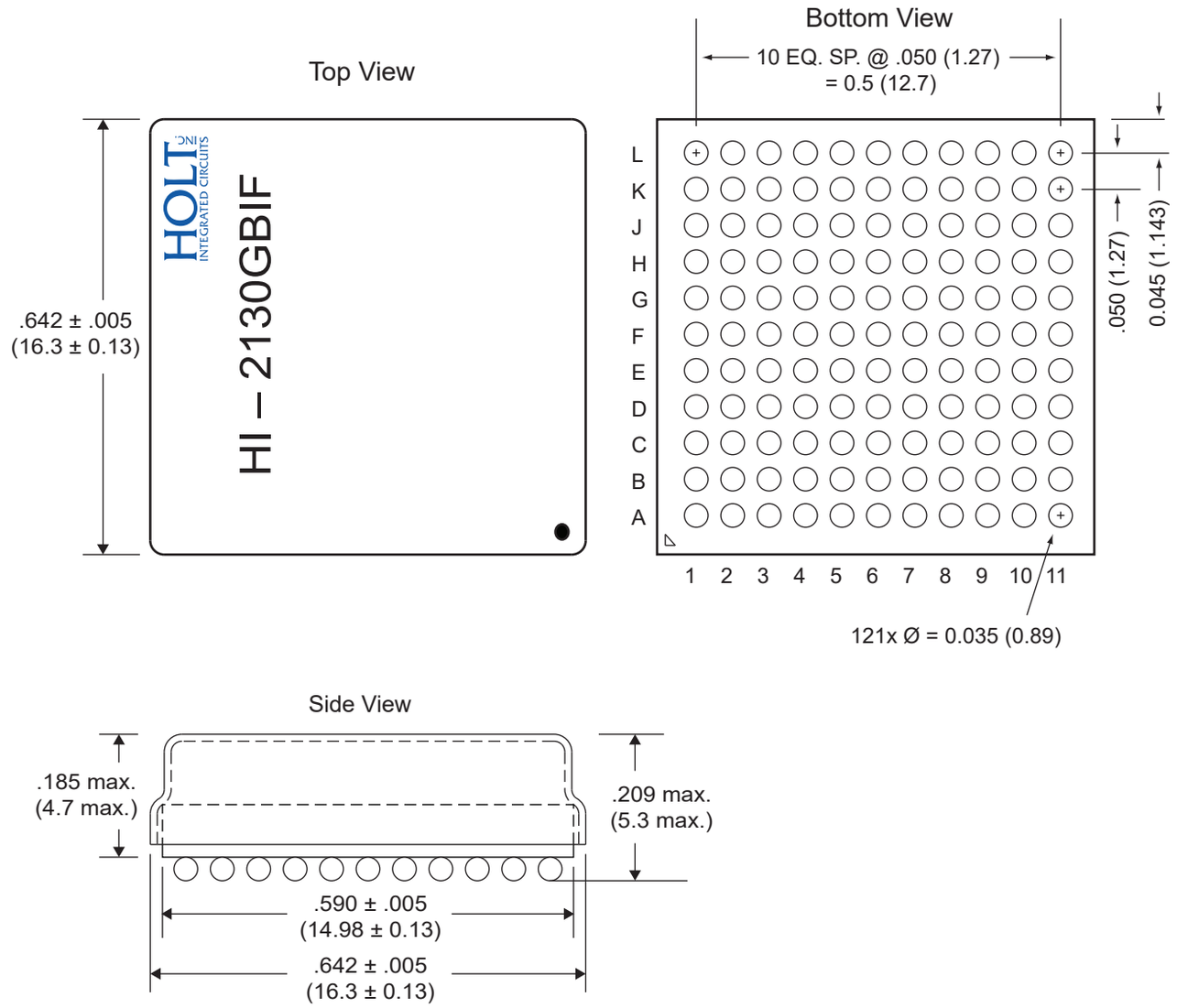
Ball Grid Array

inches (millimeters)
Package Type: 121BGA3



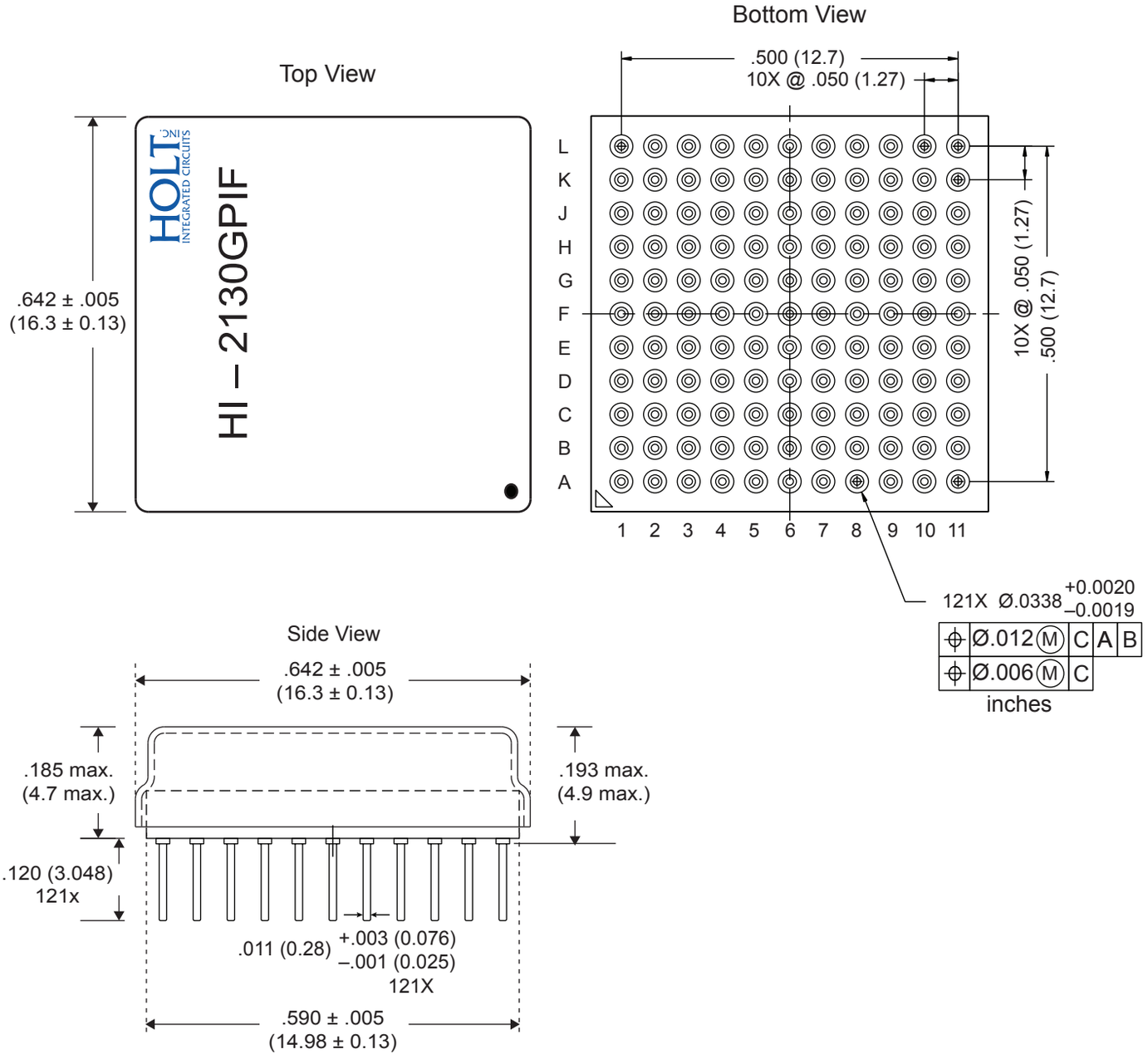
Ball Grid Array

inches (millimeters)
Package Type: 121BGA2



Pin Grid Array

inches (millimeters)
Package Type: 121PGA2



ORDERING INFORMATION

HI - 2130 LB x x **Lowest profile (4.4 mm), Overmold Option**

PART NUMBER	LEAD FINISH
Blank	Leaded Balls (Sn63Pb37)
F	Pb-free, RoHS compliant, SAC305 Solder Balls (Sn96.5/Ag3/Cu0.5)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C to +85°C	I	No
T	-55°C to +125°C	T	No

PART NUMBER	PACKAGE DESCRIPTION
LB	121 BALL GRID ARRAY - BGA (121BGA3)

HI - 2130 Gx x F **Hermetic, Metal Lid Option**

PART NUMBER	LEAD FINISH
F	Pb-free, RoHS compliant, SAC305 Solder Balls (Sn96.5/Ag3/Cu0.5)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C to +85°C	I	No
T	-55°C to +125°C	T	No
M[1]	-55°C to +125°C	M	Yes

Note 1: M-Grade available for GB package option only

PART NUMBER	PACKAGE DESCRIPTION
GP	121 PIN GRID ARRAY - PGA (121PGA2), (Pb-free, RoHS compliant)
GB	121 BALL GRID ARRAY - BGA (121BGA2), non-collapsing solder balls

REVISION HISTORY

Revision	Date	Description of Change
DS2130, Rev. New	09/14/12	Initial Release.
Rev. A	11/14/12	Corrected typos in pin diagram. Updated package drawings for new thickness. Updated Ordering Information table.
Rev. B	01/22/13	Remove LGA package option.
Rev. C	07/28/14	Remove leaded BGA option.
Rev. D	03/18/15	Replace “CB” and “CP” package options with low profile “GB” and “GP” package options.
Rev. E	05/28/15	Remove dimensions from front page package drawing.
Rev. F	11/18/15	Correct typo for $\overline{OE}$ pin.
Rev. G	05/17/16	Update BGA and PGA package dimensions. Total BGA package height is reduced to 5.1 ± 0.1mm.
Rev. H	10/24/16	Add new lower profile BGA package (LB).
Rev. J	11/02/17	Add Electrical Characteristics Table.
Rev. K	07/02/18	Update “AC Electrical Characteristics — 16-Bit Parallel Bus Host Interface Timing” parameter table and 8-bit bus width read examples to reflect two 16-bit word reads. Update Test Circuit Examples, Figure 7 and Figure 8. Update ball metallurgy in “Ordering Information”.
Rev. L	03/19/19	Correct Figure reference typos in “DC Electrical Characteristics” table. Update timing diagrams in Figure 2, Figure 3, Figure 4 and Figure 5. Waveforms shown incorrectly. Timing values in AC Electrical Characteristics did not change. Add additional timing parameters t_{DV}, T_{RA1} and T_{RA2} to “AC Electrical Characteristics — 16-Bit Parallel Bus Host Interface Timing”. Add “M-Grade” burn-in option to “GB” package.
Rev. M	07/31/19	Change maximum reflow temperature from 260°C to 245°C in “Absolute Maximum Ratings”.
Rev. N	01/10/2020	Show position of “dot” for pin A1 on top of package.
Rev. P	04/27/2020	Change thickness dimensions on ‘GB’ and ‘GP’ packages to show maximum values. Fix typos in package labels.
Rev. Q	04/13/2021	Update maximum height of metal lid BGA package (121BGA2) from 5.2 mm max. to 5.3 mm max.