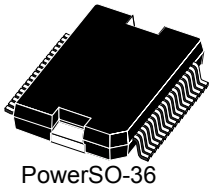
VN808CM-E, VN808CM-32-E

Datasheet

Octal channel high-side driver



PowerSO-36

Features

- CMOS compatible input
- Junction overtemperature protection
- Case overtemperature protection for thermal independence of the channels
- Current limitation
- Shorted load protection
- Undervoltage shutdown
- Protection against loss of ground
- Very low standby current
- Compliance to 61000-4-4 IEC test up to 4 kV

Description

The VN808CM-E and VN808CM-32-E are monolithic devices designed with STMicroelectronics VIPower M0-3 technology, intended to drive any kind of load with one side connected to ground. It can be driven by using a 3.3 V logic supply.

Active current limitation combined with thermal shutdown and automatic restart protect the device against overload. In overload conditions, the channel turns OFF and ON again automatically to maintain the junction temperature between T_{JSD} and T_R. If this condition causes the case temperature to trigger T_{CSD}, then overloaded channels are turned OFF and can be turned back ON only when the case temperature decreases down to T_{CR}.

. Non- overloaded channels continue to operate normally. The device automatically turns OFF in case of ground pin disconnection. This device is especially suitable for industrial applications conforming to IEC 61131.

Product status link
VN808CM-E
VN808CM-32-E

Product label

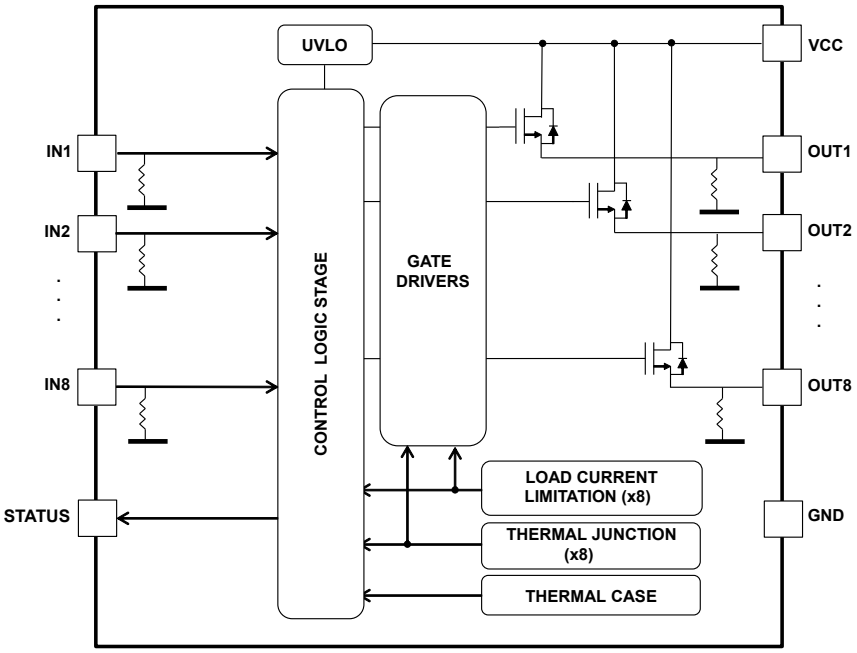
SUSTAINABLE TECHNOLOGY

Type	$R_{DS(on)}$ (1)	I_{OUT}	V_{CC}
VN808CM-E	160 mΩ	0.7 A	45 V
VN808CM-32-E	160 mΩ	1 A	45 V

1. *Per channel*

1 Overview

Figure 1. **Internal schematic**



2 Maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Max.	Unit
V_{CC}	DC Supply Voltage	45	V
$-I_{GND}$	DC Ground Reverse Current	250	mA
	TRAN ground reverse current (pulse duration < 1 ms)	6	A
I_{OUT}	DC Output Current	Internally limited	A
$-I_{OUT}$	Reverse DC Output Current	2	A
I_{IN}	DC Input Current	±10	mA
V_{IN}	Input Voltage Range	5.5	V
V_{ESD}	Electrostatic discharge (R = 1.5K Ω; C = 100pF)	2000	V
P_{TOT}	Power dissipation at Tc = 25°C	96	W
EAS	Single pulse Avalanche Energy per channel, all channels driven simultaneously (T_{AMB} = 125 °C, I_{OUT} = 0.6 A per channel)	1.15	J
T_J	Junction Operating Temperature	Internally limited	°C
T_c	Case Operating Temperature	Internally limited	°C
T_{STG}	Storage Temperature	-40 to 150	°C

Table 2. Thermal data

Symbol	Parameter	Max. value	Unit
$R_{th(JC)}$	Thermal resistance junction-case	1.3	°C/W
$R_{th(JA)}$	Thermal resistance junction-ambient	50	°C/W

1. *When mounted on FR4 printed circuit board with 0.5 cm2 of copper area (at least 35 µm thick) connected to all TAB pins.*

3 Electrical characteristics

10.5 V < V_{CC} < 32 V; -40 °C < T_J < 125 °C; unless otherwise specified.

Table 3. Power section

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{USD}	V_{CC} under-voltage turn-off threshold		7		10.5	V
R_{ON}	On-state resistance	I_{OUT} = 0.5A; T_J = 25°C			160	mΩ
		I_{OUT} = 0.5A; T_J = 125°C			280	mΩ
I_S	Supply current	OFF-state V_{CC} = 24 V; T_{CASE} = 25 °C			150	µA
		ON-state (all channels ON) V_{CC} = 24 V; T_{CASE} = 100 °C			12	mA
I_{LGND}	Output current at turn-off	V_{CC} = V_{GND} = 24 V; V_{STAT} = V_{IN} = 5 V; V_{OUT} = 0 V			1	mA
$I_{L(OFF)}$	OFF-state output current	V_{IN} = V_{OUT} = 0 V	0		5	µA
$V_{OUT(OFF)}$	OFF-state output voltage	V_{IN} = 0 V; I_{OUT} = 0 A			3	V
$t_{d(VCCON)}$	Power-on delay time from VCC rising edge	(see Figure 5)		1		ms

Table 4. Switching (V_{CC} = 24 V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
t_{ON}	Turn-ON time	R_L = 48 Ω from 80% V_{OUT} (see Figure 4)		50	100	µs
t_{OFF}	Turn-OFF time	R_L = 48 Ω to 10% V_{OUT} (see Figure 4)		75	150	µs
$dV_{OUT}/dt_{(ON)}$	Turn-ON voltage slope	R_L = 48 Ω from V_{OUT} = 2.4 V to V_{OUT} = 19.2 V (see Figure 4)		0.7		V/µs
$dV_{OUT}/dt_{(OFF)}$	Turn-OFF voltage slope	R_L = 48 Ω from V_{OUT} = 21.6 V to V_{OUT} = 2.4 V (see Figure 4)		1.5		V/µs

Table 5. Input pins

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{INL}	Input low level				1.25	V
I_{INL}	Low level input current	V_{IN} = 1.25 V	1			µA
V_{INH}	Input high level		2.25			V
I_{INH}	High level input current	V_{IN} = 2.25 V			10	µA
$V_{IN(HYST)}$	Input hysteresis voltage		0.25			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	6.0	6.8	8.0	V
		I_{IN} = -1 mA		-0.7		

Table 6. Protections

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
T_{CSD}	Case shut-down temperature		125	130	135	°C
T_{CR}	Case reset temperature		110			°C
T_{CHYST}	Case thermal hysteresis		7	15		°C
T_{JSD}	Junction shutdown temperature		150	175	200	°C
T_R	Junction reset temperature		135			°C
T_{HYST}	Junction thermal hysteresis		7	15		°C
I_{PEAK}	Maximum DC output current before limitation	V_{CC} = 24 V; R_{LOAD} = 10 mΩ	1.1		2.6	A
I_{LIM}	DC short-circuit current limitation per channel	V_{CC} = 24 V; R_{LOAD} = 10 mΩ	0.7(1) 1(2)		1.7	A
V_{DEMAG}	Turn-OFF output clamp voltage	I_{OUT} = 0.5A; L= 6 mH	V_{CC}-57	V_{CC}-52	V_{CC}-47	V

1. *VN808CM-E*
2. *VN808CM-32-E*

Table 7. Status pin

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{HSTAT}	STATUS pin high level current	V_{CC} = 18 to 32 V; R_{STAT} = 1 kΩ (Fault condition)	2	3	4	mA
I_{LSTAT}	STATUS pin leakage current	Normal operation; V_{CC} = 32 V			0.1	µA
V_{CLSTAT}	STATUS pin clamp voltage	I_{STAT} = 1 mA	6.0	6.8	8.0	V
		I_{STAT} = -1 mA		-0.7		

4 Pin connections

Figure 2. **Connection diagram (top view)**

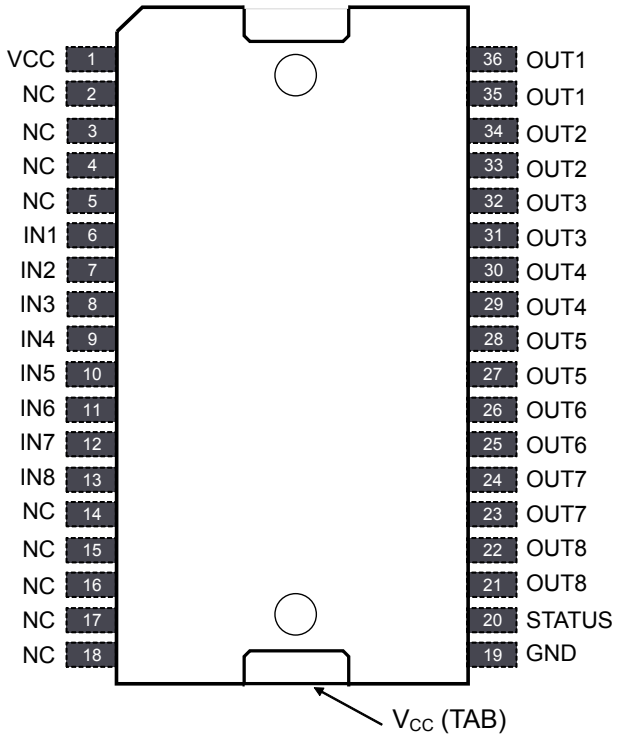


Table 8. **Pin functions**

Pin	Symbol	Description
1	V_{CC}	Positive power supply voltage
2	N.C.	Not Connected
3	N.C.	Not Connected
4	N.C.	Not Connected
5	N.C.	Not Connected
6	IN1	Channel 1 input
7	IN2	Channel 2 input
8	IN3	Channel 3 input
9	IN4	Channel 4 input
10	IN5	Channel 5 input
11	IN6	Channel 6 input
12	IN7	Channel 7 input
13	IN8	Channel 8 input
14	N.C.	Not Connected
15	N.C.	Not Connected
16	N.C.	Not Connected
17	N.C.	Not Connected

Pin	Symbol	Description
18	N.C.	Not Connected
19	GND	Output power ground
20	STATUS	Common open source diagnostic for over-temperature
21	OUT8	Channel 8 power output
22		
23	OUT7	Channel 7 power output
24		
25	OUT6	Channel 6 power output
26		
27	OUT5	Channel 5 power output
28		
29	OUT4	Channel 4 power output
30		
31	OUT3	Channel 3 power output
32		
33	OUT2	Channel 2 power output
34		
35	OUT1	Channel 1 power output
36		
TAB	V_{CC}	Exposed tab internally connected to V_{CC}, positive power supply voltage

5 Current and voltage conventions and truth table

Figure 3. **Current and voltage conventions**

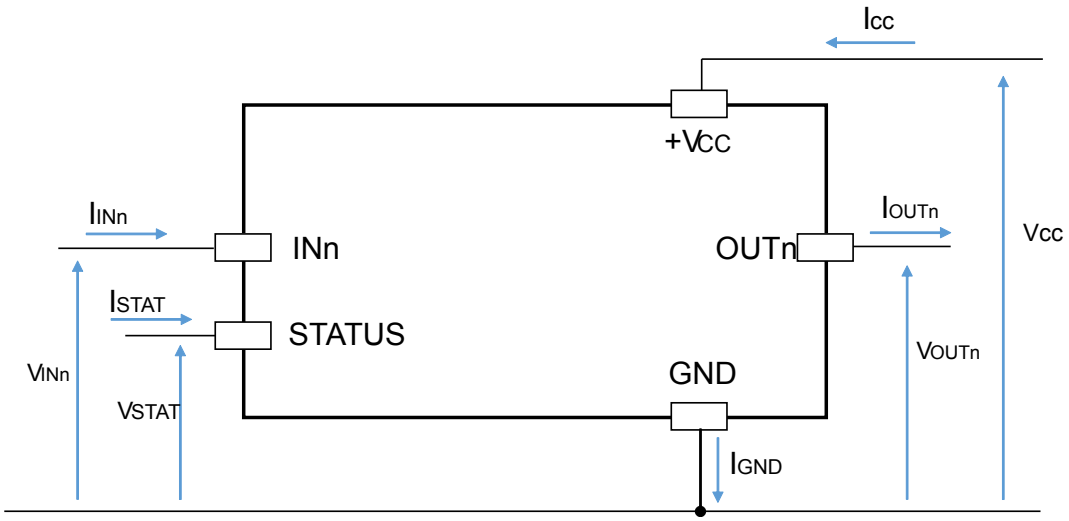


Table 9. **Truth table**

Conditions	INPUTn	OUTPUTn	STATUS
Normal operation	L H	L H	L L
Current limitation	L H	L X	L L
Over-temperature (see Figure 13 and Figure 14)	L H	L L	L H
Undervoltage	L H	L L	X X

6 Switching time waveforms

Figure 4. Turn-ON and turn-OFF

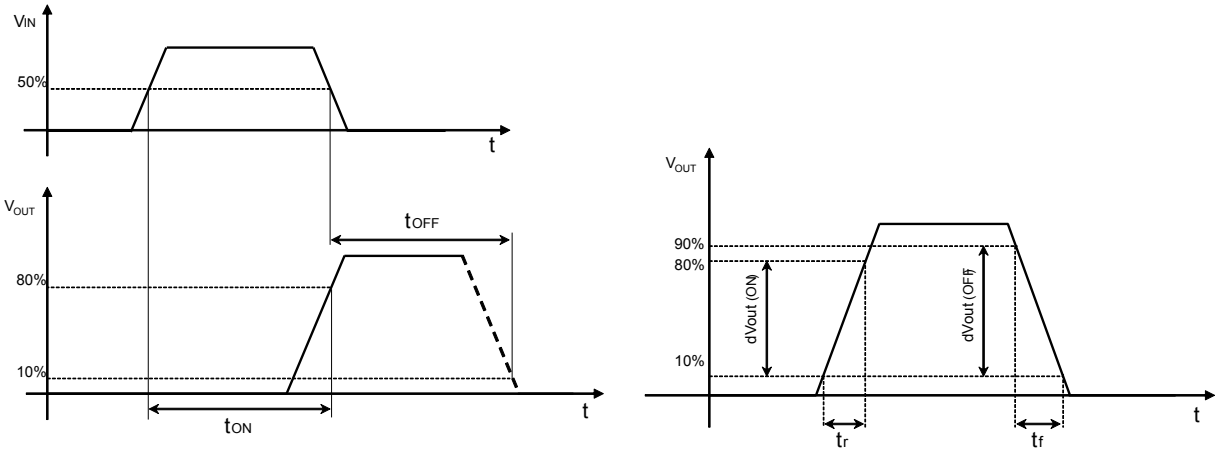
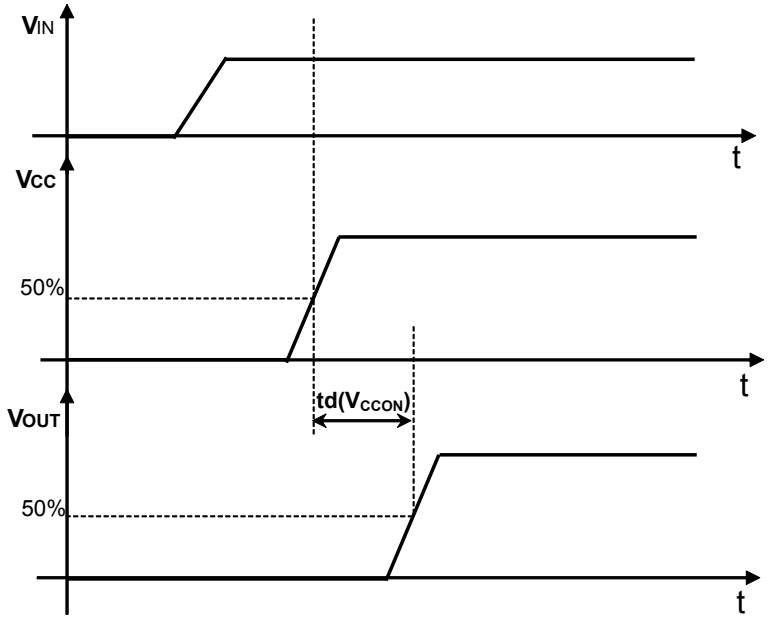


Figure 5. V_{CC} turn-ON



7 Power section

7.1 Current limitation

The current limitation process is activated when the current sense connected on the output stage measures a current value higher than a fixed threshold.

When this condition is verified, the gate voltage is modulated to prevent the output current from rising above the limitation value.

The following figures show typical output current waveforms with different load conditions.

Figure 6. Switching on resistive load

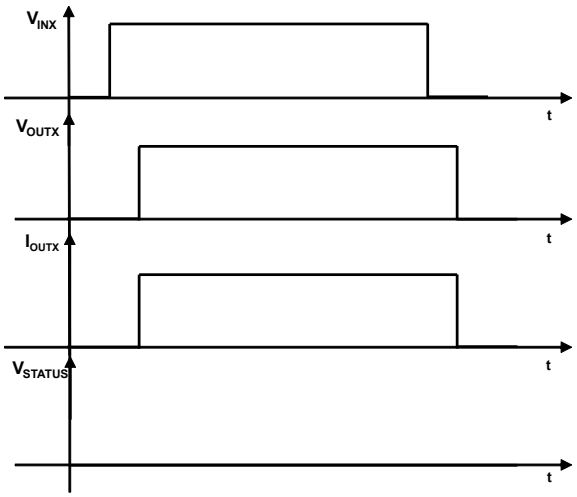


Figure 7. Switching on bulb lamp load

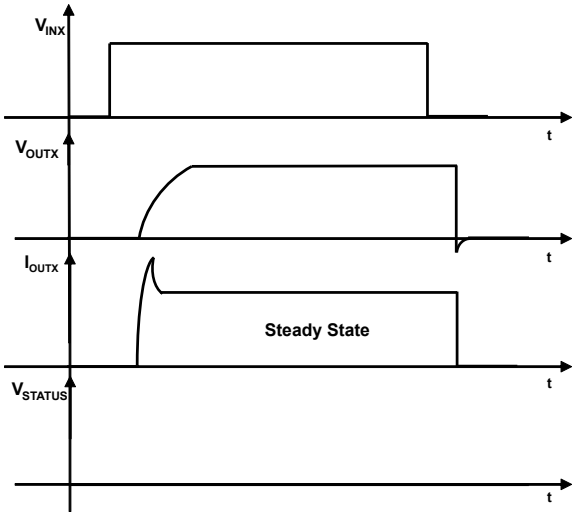


Figure 8. Switching on light inductive load

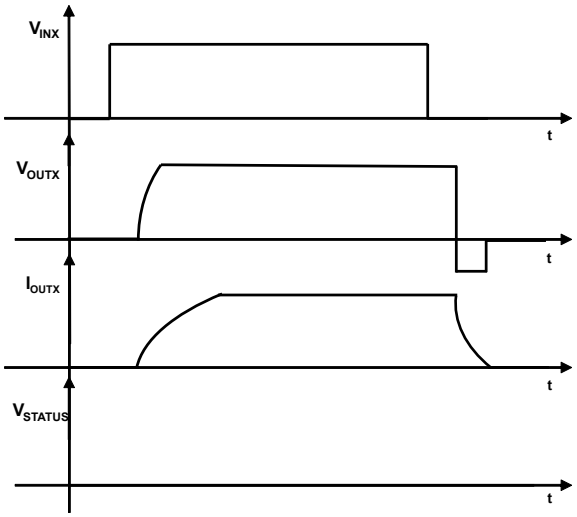


Figure 9. Switching on heavy inductive load

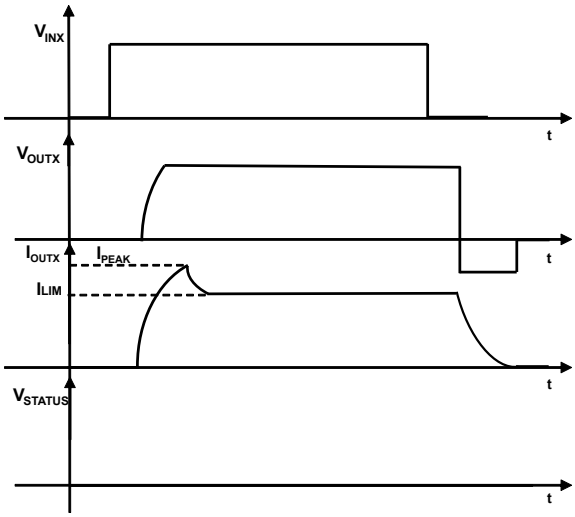


Figure 10. **Short-circuit during ON state**

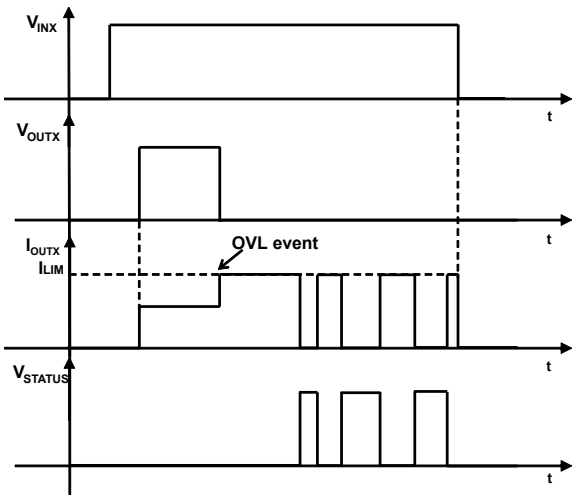
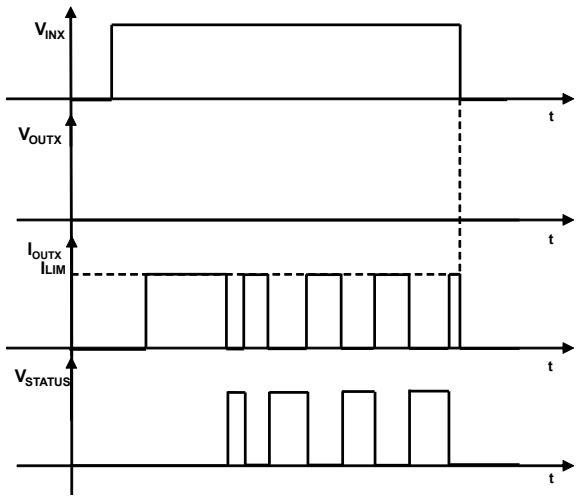


Figure 11. **Switching on short-circuit**



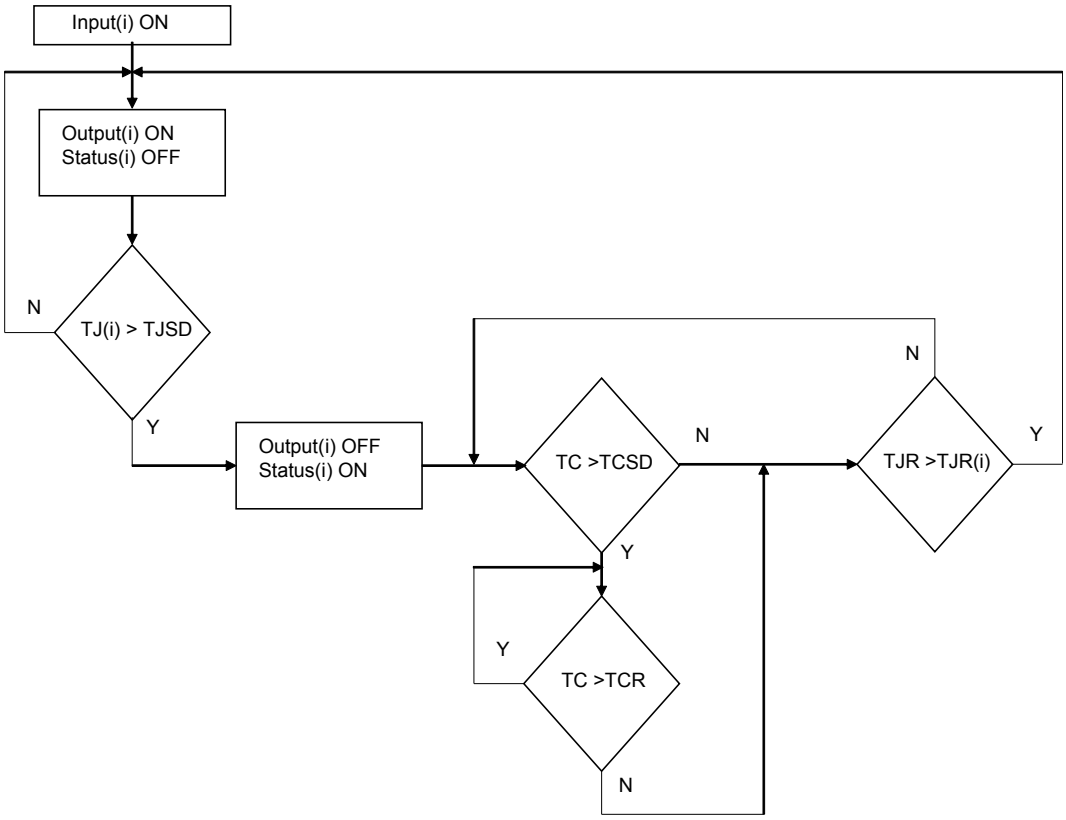
7.2 Thermal protection

The device is protected against overheating due to overload conditions. When the output is overloaded during the driving period, the device suffers two different thermal stresses: the first relates to the junction, and the second relates to the case.

The two faults have different trigger thresholds: the junction protection threshold (T_{JSD}) is higher than the case protection one (T_{CSD}); generally the first protection that is activated in thermal stress conditions is the junction thermal shut-down. The output is turned-off when the temperature is higher than its threshold and turned back on when it falls below the reset threshold (T_{JR}). This behavior continues while the fault on the output is present.

If the thermal protection is active and the temperature of the package increases above the fixed case protection threshold, the case protection is activated and the output is switched-off and back on when the junction temperature of each channel in fault and case temperature are below the respective reset thresholds.

Figure 12. **Thermal protection logic**



7.3 STATUS indication

The STATUS pin is an active high common open source output indicating fault conditions. This pin is activated in case of junction overtemperature (T_{JX} >T_{JSD}) of one or more output channels. Figure 13 and Figure 14 show the STATUS behavior when T_{JSD} is triggered before T_{CSD} and when T_{CSD} is triggered before $T_{JSD,}$ respectively.

Figure 13. Thermal protection and STATUS behavior (T_{JSD} triggered before T_{CSD})

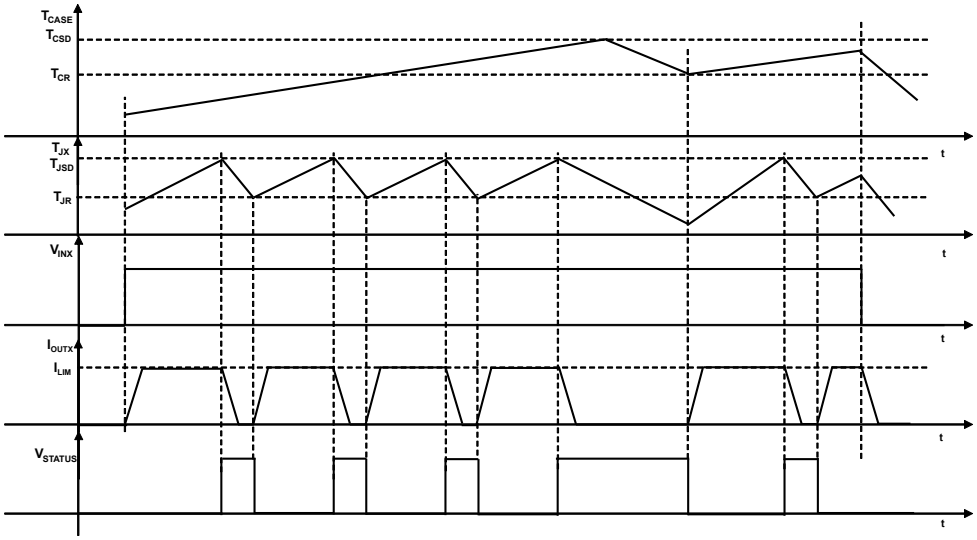
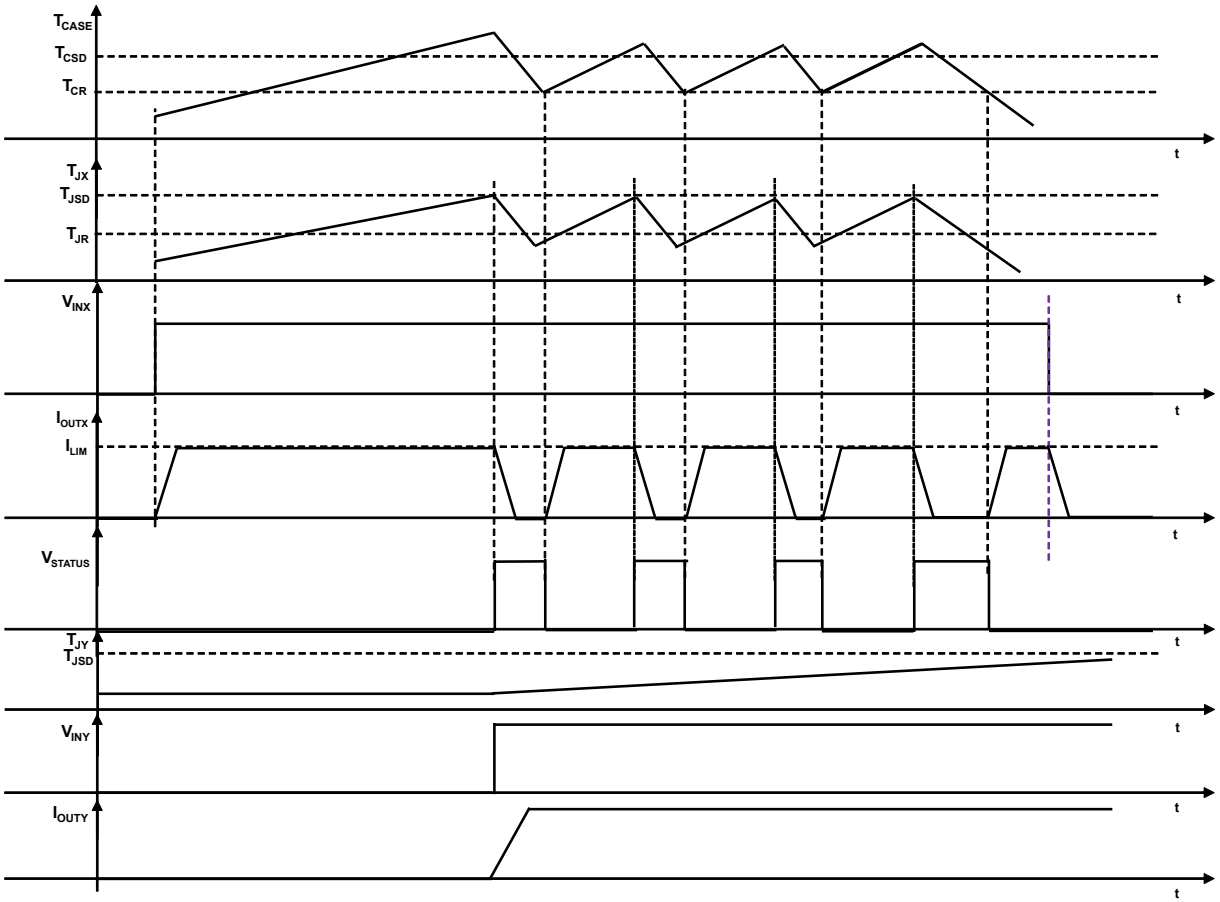


Figure 14. Thermal protection and STATUS behavior (T_{CSD} triggered before T_{JSD})



8 Reverse polarity protection

Reverse polarity protection can be implemented on board using two different solutions:

1. Placing a resistor (R_{GND}) between IC GND pin and load GND
2. Placing a diode between IC GND pin and load GND

If option 1 is selected, the minimum resistance value has to be selected according to the following equation:

$$R_{GND} \geq \frac{V_{CC}}{I_{GND}} \quad (1)$$

where I_{GND} is the DC reverse ground pin current and can be found in Maximum ratings.

Power dissipated by R_{GND} (when $V_{CC} < 0$: during reverse polarity situations) is:

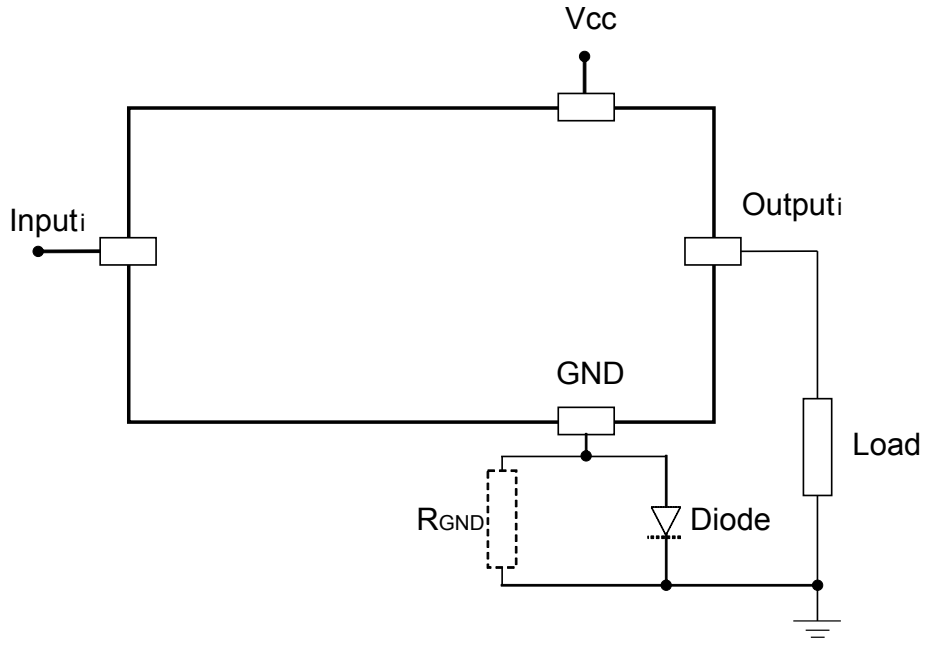
$$P_D = \frac{(V_{CC})^2}{R_{GND}} \quad (2)$$

If option 2 is selected, the diode has to be chosen by taking into account VRRM >$|V_{cc}|$ and its power dissipation capability:

$$P_D \geq I_S \times V_f \quad (3)$$

*Note: In normal operation (no reverse polarity), there is a voltage drop (ΔV) between GND of the device and GND of the system. Using option 1, ΔV = R_{GND} * I_{CC}. Using option 2, ΔV = VF@(IF).*

Figure 15. Reverse polarity protection

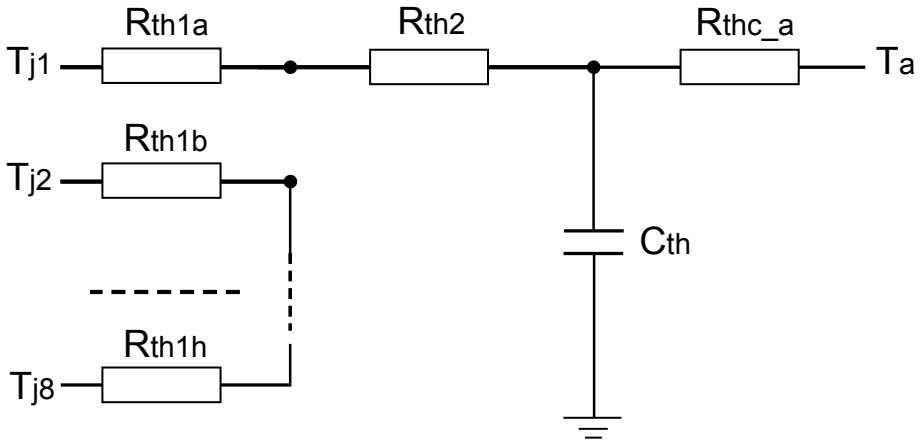


This schematic can be used with any type of load.

9 Thermal information

9.1 Thermal impedance

Figure 16. **Simplified thermal model of the process stage**



10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

10.1 PowerSO-36 package information

Figure 17. **PowerSO-36 package outline**

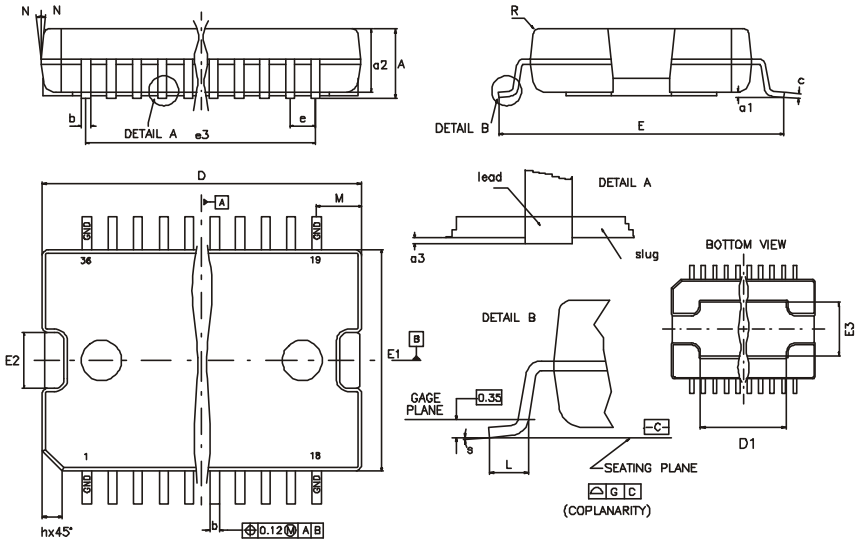


Table 10. **PowerSO-36 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A			3.60
a1	0.10		0.30
a2			3.30
a3	0		0.10
b	0.22		0.38
c	0.23		0.32
D(1)	15.80		16.00
D1	9.40		9.80
E	13.90		14.50
E1(1)	10.90		11.10
E2			2.90
E3	5.8		6.2
e		0.65	
e3		11.05	
G	0		0.10

Dim.	mm		
	Min.	Typ.	Max.
H	15.50		15.90
h			1.10
L	0.80		1.10
N			10°
S	0°		8°

1. *D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm (0.006”). Critical dimensions are "a3", "E" and "G".*

10.2 Footprint recommended data

Figure 18. **Footprint recommended data**

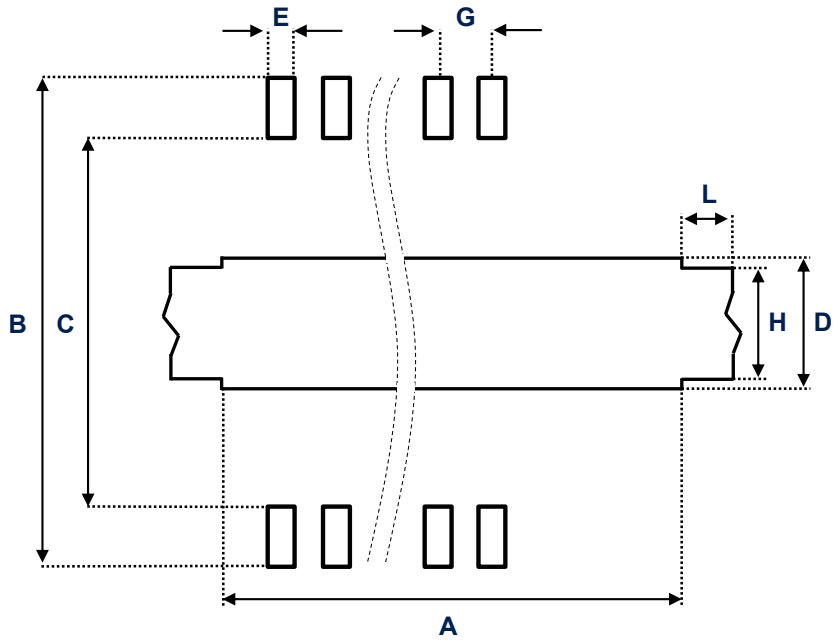


Table 11. **Footprint data**

Dim	mm
A	9.5
B	14.7 - 15.0
C	12.5 - 12.7
D	6.3
E	0.42
G	0.65
H	4.1
L	3.2

10.3 Tube shipment information

Figure 19. **Tube shipment information**

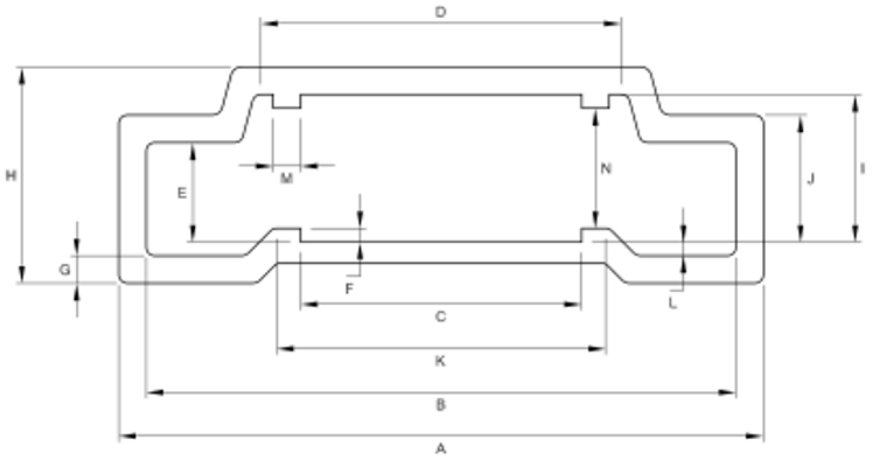


Table 12. **Tube mechanical data**

Dim	mm
A	18.80
B	17.2±0.2
C	8.20±0.2
D	10.90±0.2
E	2.90±0.2
F	0.40
G	0.80
H	6.30
I	4.30±0.2
J	3.7±0.2
K	9.4
L	0.40
M	0.80
N	3.50±0.2

10.4 Tape and reel shipment information

Figure 20. **Tape specifications**

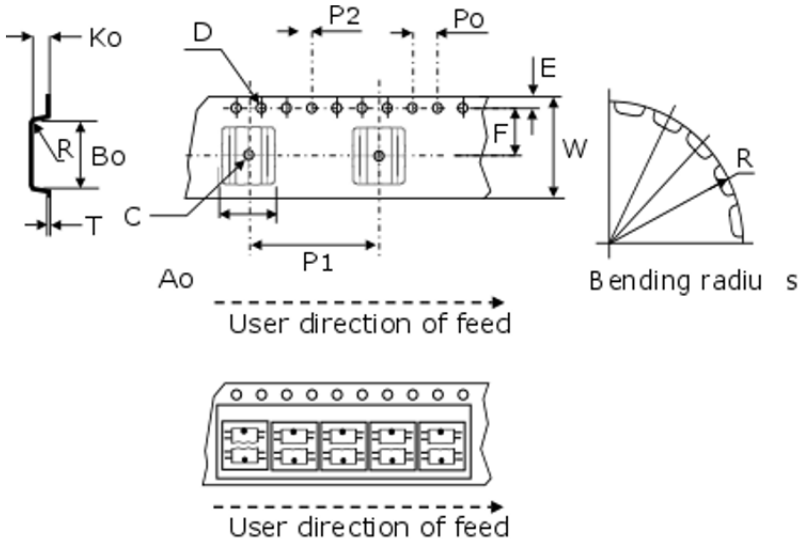


Table 13. **Tape mechanical data**

Dim	mm
D	1.50+0.1/0
E	1.75 ±0.1
PO	4.00 ±0.1
Tmax	0.40
D1min	1.50
F	11.5 ±0.05
Kmax	6.50
P2	2.00 ±0.1
R	50
W	24.00 ±0.30
P1	24.00
AO, BO, KO	0.05 min to 1.0 max

Figure 21. **Reel specifications**

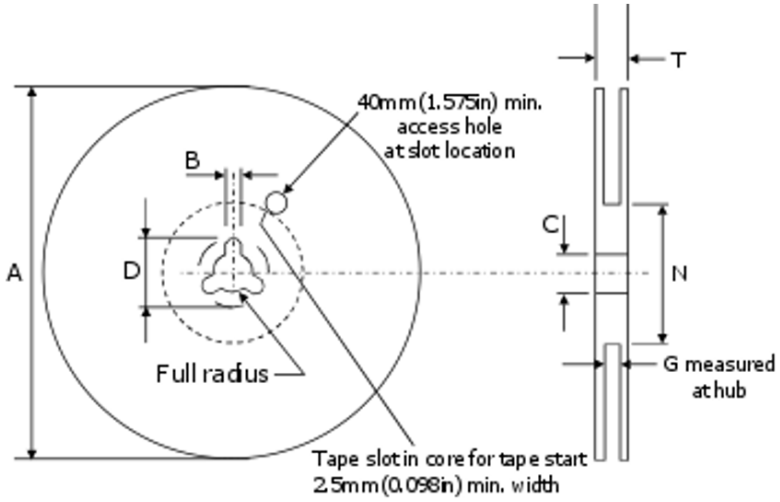


Table 14. **Reel mechanical data**

Dim	mm
Tape size	24.0±0.30
Amax	330.0
Bmin	1.5
C	13.0±0.20
Dmin	20.2
Nmin	60
G	24.4+2/-0
Tmax	30.4

11 Ordering information

Table 15. **Order code**

Order code	Package	Packaging
VN808CM-E	PowerSO-36	Tube
VN808CMTR-E		Tape and reel
VN808CM-32-E		Tube
VN808CMTR-32-E		Tape and reel

Revision history

Table 16. **Document revision history**

Date	Version	Changes
29-Jun-2005	1	Initial release
12-Sep-2005	2	New template
28-Jun-2006	3	Application schematic updated
09-Jul-2008	4	Added Section 6: Reverse polarity protection
04-Aug-2008	5	Added Figure 9: PowerSO-36 drawings
26-Aug-2009	6	Updated Section 6: Reverse polarity protection
15-Sep-2009	7	Typing mistake in cover page: Section : Features and Table 5: Input pin
24-Feb-2010	8	Updated Section 7: Package mechanical data
01-Aug-2013	9	Updated Section 7.1: Footprint recommended data
18-Dec-2013	10	Replaced L_{MAX} parameter in Table 1 by EAS parameter. Added TJ condition to Table 3. Updated Section 6.
22-Jun-2020	11	Throughout document: - Added VN808CM-32-E technical and ordering information - Updated document template - Minor text changes In Section 3 : - Updated I_{LGND} and $t_{d(Vccon)}$ test conditions In Table 4: - Updated all figure references In Table 6: - Added row I_{PEAK} - Updated I_{lim} test conditions In Table 9: - Updated figure reference for overtemperature In Section 6 : - Deleted Figure 6. Waveforms Added Section 7 Power section In Section 8 Reverse polarity protection: - Updated note “In normal…” - Updated Figure 15 Added Section 9
22-Feb-2021	12	Corrected AMR of V_{IN} to 5.5 V in Table 1 ; deleted V_{CC} operating range in Table 3.

Contents

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