Never stop thinking

32-Bit

TC1797

32-Bit Single-Chip Microcontroller

Data Sheet

V1.3 2014-08

Microcontrollers

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Revision History: V1.3, 2014-08

Previous Version: V1.2, 2009-09	
Page	Subjects (major changes since last revision)
6	add SAK-TC1797-512F180EF and SAK-TC1797-384F150EF.
185	add figure for new package P/PG-BGA-416-27.
all	add package P/PG-BGA-416-27 for new variants SAK-TC1797-512F180EF and SAK-TC1797-384F150EF.

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1 Summary of Features

- High-performance 32-bit super-scalar TriCore V1.3.1 CPU with 4-stage pipeline
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Single precision Floating Point Unit (FPU)
  - 180 or 150[1)] MHz operation at full temperature range
- 32-bit Peripheral Control Processor with single cycle instruction (PCP2)
  - 16 Kbyte Parameter Memory (PRAM)
  - 32 Kbyte Code Memory (CMEM)
  - 180 or150[1)] MHz operation at full temperature range
- Multiple on-chip memories
  - 4 or 3[1)] Mbyte Program Flash Memory (PFLASH) with ECC
  - 64 Kbyte Data Flash Memory (DFLASH) usable for EEPROM emulation
  - 128 Kbyte Data Memory (LDRAM)
  - 40 Kbyte Code Scratchpad Memory (SPRAM)
  - Instruction Cache: up to 16 Kbyte (ICACHE, configurable)
  - Data Cache: up to 4 Kbyte (DCACHE, configurable)
  - 8 Kbyte Overlay Memory (OVRAM)
  - 16 Kbyte BootROM (BROM)
- 16-Channel DMA Controller
- 32-bit External Bus Interface Unit (EBU) with
  - 32-bit demultiplexed / 16-bit multiplexed external bus interface (3.3V, 2.5V)
  - Support for Burst Flash memory devices
  - Scalable external bus timing up to 75 MHz
- Sophisticated interrupt system with 2×255 hardware priority arbitration levels serviced by CPU or PCP2
- High performing on-chip bus structure
  - 64-bit Local Memory Buses between CPU, EBU, Flash and Data Memory
  - 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
  - One bus bridges (LFI Bridge)
- Versatile On-chip Peripheral Units
  - Two Asynchronous/Synchronous Serial Channels (ASC) with baud rate generator, parity, framing and overrun error detection
  - Two High-Speed Synchronous Serial Channels (SSC) with programmable data length and shift direction
  - Two serial Micro Second Bus interface (MSC) for serial port expansion to external power devices

1) Derivative dependent.

  - Two High-Speed Micro Link interface (MLI) for serial inter-processor communication
  - One MultiCAN Module with 4 CAN nodes and 128 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer
  - One FlexRay™ module with 2 channels (E-Ray).
  - Two General Purpose Timer Array Modules (GPTA) with additional Local Timer Cell Array (LTCA2) providing a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
- 44 analog input lines for ADC
  - 3 independent kernels (ADC0, ADC1, ADC2)
  - Analog supply voltage range from 3.3 V to 5 V (single supply)
  - Performance for 12 bit resolution (@f_{ADCI} = 10 MHz)
- 4 different FADC input channels
  - channels with impedance control and overlaid with ADC1 inputs
  - Extreme fast conversion, 21 cycles of f_{FADC} clock (262.5 ns @ f_{FADC} = 80 MHz)
  - 10-bit A/D conversion (higher resolution can be achieved by averaging of consecutive conversions in digital data reduction filter)
- 221 digital general purpose I/O lines[1)] (GPIO), 4 input lines
- Digital I/O ports with 3.3 V capability
- On-chip debug support for OCDS Level 1 (CPU, PCP, DMA, On Chip Bus)
- Dedicated Emulation Device chip available (TC1797ED)
  - multi-core debugging, real time tracing, and calibration
  - four/five wire JTAG (IEEE 1149.1) or two wire DAP (Device Access Port) interface
- Power Management System
- Clock Generation Unit with PLL
- Core supply voltage of 1.5 V
- I/O voltage of 3.3 V
- Full automotive temperature range: -40° to +125°C
- Package variants: P/PG-BGA-416-10 and P/PG-BGA-416-27

1) TC1797 package variant P/PG-BGA-416-10 / P/PG-BGA-416-27: 86 GPIO´s

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- The package and the type of delivery.

For the available ordering codes for the TC1797 please refer to the **"Product Catalog Microcontrollers"**, which summarizes all available microcontroller variants.

This document describes the derivatives of the device.The **Table 1** enumerates these derivatives and summarizes the differences.

Table 1 TC1797 Derivative Synopsis

Derivative	Ambient Temperature Range	Program Flash	CPU frequency	Package
SAK-TC1797-512F180E	T_A = -40°C to +125°C	4 MBytes	180MHz	P/PG-BGA-416-10
SAK-TC1797-384F150E	T_A = -40°C to +125°C	3 MBytes	150MHz	P/PG-BGA-416-10
SAK-TC1797-512F180EF	T_A = -40°C to +125°C	4 MBytes	180MHz	P/PG-BGA-416-27
SAK-TC1797-384F150EF	T_A = -40°C to +125°C	3 MBytes	150MHz	P/PG-BGA-416-27

2 Introduction

This Data Sheet describes the Infineon TC1797, a 32-bit microcontroller DSP, based on the Infineon TriCore Architecture.

2.1 About this Document

This document is designed to be read primarily by design engineers and software engineers who need a detailed description of the interactions of the TC1797 functional units, registers, instructions, and exceptions.

This TC1797 Data Sheet describes the features of the TC1797 with respect to the TriCore Architecture. Where the TC1797 directly implements TriCore architectural functions, this manual simply refers to those functions as features of the TC1797. In all cases where this manual describes a TC1797 feature without referring to the TriCore Architecture, this means that the TC1797 is a direct implementation of the TriCore Architecture.

Where the TC1797 implements a subset of TriCore architectural features, this manual describes the TC1797 implementation, and then describes how it differs from the TriCore Architecture. Such differences between the TC1797 and the TriCore Architecture are documented in the section covering each such subject.

2.1.1 Related Documentations

A complete description of the TriCore architecture is found in the document entitled “TriCore Architecture Manual”. The architecture of the TC1797 is described separately this way because of the configurable nature of the TriCore specification: Different versions of the architecture may contain a different mix of systems components. The TriCore architecture, however, remains constant across all derivative designs in order to preserve compatibility.

This Data Sheets together with the “TriCore Architecture Manual” are required to understand the complete TC1797 micro controller functionality.

2.1.2 Text Conventions

This document uses the following text conventions for named components of the TC1797:

- Functional units of the TC1797 are given in plain UPPER CASE. For example: “The SSC supports full-duplex and half-duplex synchronous communication”.
- Pins using negative logic are indicated by an overline. For example: “The external reset pin, $\overline{\text{ESR0}}$, has a dual function.”.
- Bit fields and bits in registers are in general referenced as “Module_Register name.Bit field” or “Module_Register name.Bit”. For example: “The Current CPU Priority Number bit field CPU_ICR.CCPN is cleared”. Most of the

register names contain a module name prefix, separated by an underscore character "_" from the actual register name (for example, "ASC0_CON", where "ASC0" is the module name prefix, and "CON" is the kernel register name). In chapters describing the kernels of the peripheral modules, the registers are mainly referenced with their kernel register names. The peripheral module implementation sections mainly refer to the actual register names with module prefixes.

- Variables used to describe sets of processing units or registers appear in mixed upper and lower cases. For example, register name "MSGCFGn" refers to multiple "MSGCFG" registers with variable n. The bounds of the variables are always given where the register expression is first used (for example, "n = 0-31"), and are repeated as needed in the rest of the text.
- The default radix is decimal. Hexadecimal constants are suffixed with a subscript letter "H", as in 100_H. Binary constants are suffixed with a subscript letter "B", as in: 111_B.
- When the extent of register fields, groups register bits, or groups of pins are collectively named in the body of the document, they are represented as "NAME[A:B]", which defines a range for the named group from B to A. Individual bits, signals, or pins are given as "NAME[C]" where the range of the variable C is given in the text. For example: CFG[2:0] and SRPN[0].
- Units are abbreviated as follows:
  - **MHz** = Megahertz
  - **µs** = Microseconds
  - **kBaud, kbit** = 1000 characters/bits per second
  - **MBaud, Mbit** = 1,000,000 characters/bits per second
  - **Kbyte, KB** = 1024 bytes of memory
  - **Mbyte, MB**= 1048576 bytes of memory

    In general, the k prefix scales a unit by 1000 whereas the K prefix scales a unit by 1024. Hence, the Kbyte unit scales the expression preceding it by 1024. The kBaud unit scales the expression preceding it by 1000. The M prefix scales by 1,000,000 or 1048576, and µ scales by .000001. For example, 1 Kbyte is 1024 bytes, 1 Mbyte is 1024 × 1024 bytes, 1 kBaud/kbit are 1000 characters/bits per second, 1 MBaud/Mbit are 1000000 characters/bits per second, and 1 MHz is 1,000,000 Hz.
- Data format quantities are defined as follows:
  - **Byte** = 8-bit quantity
  - **Half-word** = 16-bit quantity
  - **Word** = 32-bit quantity
  - **Double-word** = 64-bit quantity

2.1.3 Reserved, Undefined, and Unimplemented Terminology

In tables where register bit fields are defined, the following conventions are used to indicate undefined and unimplemented function. Furthermore, types of bits and bit fields are defined using the abbreviations as shown in **Table 2**.

Table 2 Bit Function Terminology

Function of Bits	Description
Unimplemented, Reserved	Register bit fields named **0** indicate unimplemented functions with the following behavior. • Reading these bit fields returns 0. • These bit fields should be written with 0 if the bit field is defined as r or rh. • These bit fields have to be written with 0 if the bit field is defined as rw. These bit fields are reserved. The detailed description of these bit fields can be found in the register descriptions.
rw	The bit or bit field can be read and written.
rwh	As rw, but bit or bit field can be also set or reset by hardware.
r	The bit or bit field can only be read (read-only).
w	The bit or bit field can only be written (write-only). A read to this register will always give a default value back.
rh	This bit or bit field can be modified by hardware (read-hardware, typical example: status flags). A read of this bit or bit field give the actual status of this bit or bit field back. Writing to this bit or bit field has no effect to the setting of this bit or bit field.
s	Bits with this attribute are “sticky” in one direction. If their reset value is once overwritten by software, they can be switched again into their reset state only by a reset operation. Software cannot switch this type of bit into its reset state by writing the register. This attribute can be combined to “rws” or “rwhs”.
f	Bits with this attribute are readable only when they are accessed by an instruction fetch. Normal data read operations will return other values.

2.1.4 Register Access Modes

Read and write access to registers and memory locations are sometimes restricted. In memory and register access tables, the terms as defined in **Table 3** are used.

Table 3 Access Terms

Symbol	Description
U	Access Mode: Access permitted in User Mode 0 or 1.
	Reset Value: Value or bit is not changed by a reset operation.
SV	Access permitted in Supervisor Mode.
R	Read-only register.
32	Only 32-bit word accesses are permitted to this register/address range.
E	Endinit-protected register/address.
PW	Password-protected register/address.
NC	No change, indicated register is not changed.
BE	Indicates that an access to this address range generates a Bus Error.
nBE	Indicates that no Bus Error is generated when accessing this address range, even though it is either an access to an undefined address or the access does not follow the given rules.
nE	Indicates that no Error is generated when accessing this address or address range, even though the access is to an undefined address or address range. True for CPU accesses (MTCR/MFCR) to undefined addresses in the CSFR range.

2.1.5 Abbreviations and Acronyms

The following acronyms and terms are used in this document:

ADC	Analog-to-Digital Converter
AGPR	Address General Purpose Register
ALU	Arithmetic and Logic Unit
ASC	Asynchronous/Synchronous Serial Controller
BCU	Bus Control Unit
BROM	Boot ROM & Test ROM
CAN	Controller Area Network
CMEM	PCP Code Memory
CISC	Complex Instruction Set Computing
CPS	CPU Slave Interface
CPU	Central Processing Unit

CSA	Context Save Area
CSFR	Core Special Function Register
DAP	Device Access Port
DAS	Device Access Server
DCACHE	Data Cache
DFLASH	Data Flash Memory
DGPR	Data General Purpose Register
DMA	Direct Memory Access
DMI	Data Memory Interface
EBU	External Bus Interface
EMI	Electro-Magnetic Interference
FADC	Fast Analog-to-Digital Converter
FAM	Flash Array Module
FCS	Flash Command State Machine
FIM	Flash Interface and Control Module
FPI	Flexible Peripheral Interconnect (Bus)
FPU	Floating Point Unit
GPIO	General Purpose Input/Output
GPR	General Purpose Register
GPTA	General Purpose Timer Array
ICACHE	Instruction Cache
I/O	Input / Output
JTAG	Joint Test Action Group = IEEE1149.1
LBCU	Local Memory Bus Control Unit
LDRAM	Local Data RAM
LFI	Local Memory-to-FPI Bus Interface
LMB	Local Memory Bus
LTC	Local Timer Cell
MLI	Micro Link Interface
MMU	Memory Management Unit
MSB	Most Significant Bit
MSC	Micro Second Channel

NC	Not Connected
NMI	Non-Maskable Interrupt
OCDS	On-Chip Debug Support
OVRAM	Overlay Memory
PCP	Peripheral Control Processor
PMU	Program Memory Unit
PLL	Phase Locked Loop
PCODE	PCP Code Memory
PFLASH	Program Flash Memory
PMI	Program Memory Interface
PMU	Program Memory Unit
PRAM	PCP Parameter RAM
RAM	Random Access Memory
RISC	Reduced Instruction Set Computing
SBCU	System Peripheral Bus Control Unit
SCU	System Control Unit
SFR	Special Function Register
SPB	System Peripheral Bus
SPRAM	Scratch-Pad RAM
SRAM	Static Data Memory
SRN	Service Request Node
SSC	Synchronous Serial Controller
STM	System Timer
WDT	Watchdog Timer

2.2 System Architecture of the TC1797

The TC1797 combines three powerful technologies within one silicon die, achieving new levels of power, speed, and economy for embedded applications:

- Reduced Instruction Set Computing (RISC) processor architecture
- Digital Signal Processing (DSP) operations and addressing modes
- On-chip memories and peripherals

DSP operations and addressing modes provide the computational power necessary to efficiently analyze complex real-world signals. The RISC load/store architecture provides high computational bandwidth with low system cost. On-chip memory and peripherals are designed to support even the most demanding high-bandwidth real-time embedded control-systems tasks.

Additional high-level features of the TC1797 include:

- Efficient memory organization: instruction and data scratch memories, caches
- Serial communication interfaces – flexible synchronous and asynchronous modes
- Peripheral Control Processor – standalone data operations and interrupt servicing
- DMA Controller – DMA operations and interrupt servicing
- General-purpose timers
- High-performance on-chip buses
- On-chip debugging and emulation facilities
- Flexible interconnections to external components
- Flexible power-management

The TC1797 is a high-performance microcontroller with TriCore CPU, program and data memories, buses, bus arbitration, an interrupt controller, a peripheral control processor and a DMA controller and several on-chip peripherals. The TC1797 is designed to meet the needs of the most demanding embedded control systems applications where the competing issues of price/performance, real-time responsiveness, computational power, data bandwidth, and power consumption are key design elements.

The TC1797 offers several versatile on-chip peripheral units such as serial controllers, timer units, and Analog-to-Digital converters. Within the TC1797, all these peripheral units are connected to the TriCore CPU/system via the Flexible Peripheral Interconnect (FPI) Bus and the Local Memory Bus (LMB). Several I/O lines on the TC1797 ports are reserved for these peripheral units to communicate with the external world.

2.2.1 TC1797 Block Diagram

Figure 1 shows the block diagram of the TC1797.

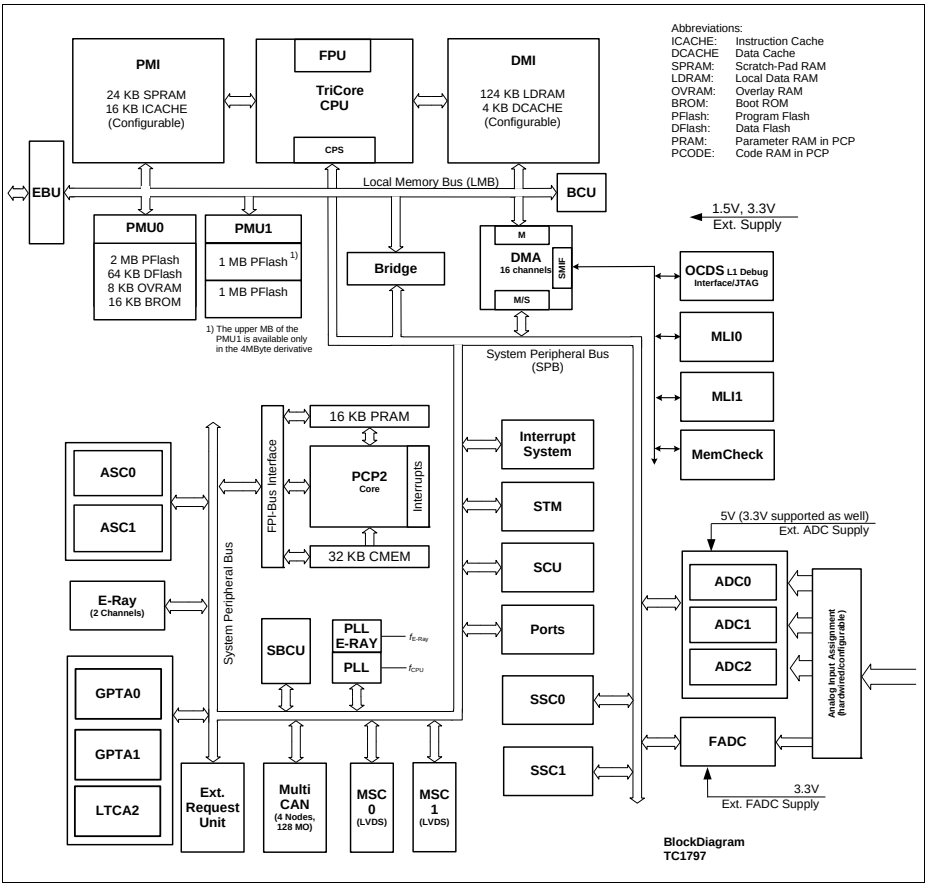


Figure 1 TC1797 Block Diagram

2.2.2 System Features

The TC1797 has the following features:

Package

- P/PG-BGA-416-10 package, 1mm pitch
- P/PG-BGA-416-27 package, 1mm pitch

Clock Frequencies for the 180 MHz derivative

- Maximum CPU clock frequency: 180 MHz[1)]
- Maximum PCP clock frequency: 180 MHz[2)]
- Maximum system clock frequency: 90 MHz[3)]

Clock Frequencies for the 150 MHz derivative

- Maximum CPU clock frequency: 150 MHz[1)]
- Maximum PCP clock frequency: 150 MHz[2)]
- Maximum system clock frequency: 90 MHz[3)]

1) For CPU frequencies > 90 MHz, 2:1 mode has to be enabled. CPU 2:1 mode means: $f_{FPI} = 0.5 * f_{CPU}$
2) For PCP frequencies > 90 MHz, 2:1 mode has to be enabled. PCP 2:1 mode means: $f_{FPI} = 0.5 * f_{PCP}$
3) CPU 1:1 Mode means: $f_{FPI} = f_{CPU}$. PCP 1:1 mode means: $f_{FPI} = f_{PCP}$

2.2.3 CPU Cores of the TC1797

The TC1797 includes a high Performance CPU and a Peripheral Control Processor.

2.2.3.1 High-performance 32-bit CPU

This chapter gives an overview about the TriCore 1 architecture.

TriCore (TC1.3.1) Architectural Highlights

- Unified RISC MCU/DSP
- 32-bit architecture with 4 Gbytes unified data, program, and input/output address space
- Fast automatic context-switching
- Multiply-accumulate unit
- Floating point unit
- Saturating integer arithmetic
- High-performance on-chip peripheral bus (FPI Bus)
- Register based design with multiple variable register banks
- Bit handling
- Packed data operations
- Zero overhead loop
- Precise exceptions
- Flexible power management

High-efficiency TriCore Instruction Set

- 16/32-bit instructions for reduced code size
- Data types include: Boolean, array of bits, character, signed and unsigned integer, integer with saturation, signed fraction, double-word integers, and IEEE-754 single-precision floating point
- Data formats include: Bit, 8-bit byte, 16-bit half-word, 32-bit word, and 64-bit double-word data formats
- Powerful instruction set
- Flexible and efficient addressing mode for high code density

Integrated CPU related On-Chip Memories

- Instruction memory: 40 KB total. After reset, configured into:[1)]
  - 40 Kbyte Scratch-Pad RAM (SPRAM)
  - 0 Kbyte Instruction Cache (ICACHE)
- Data memory: 128 KB total. After reset, configured into:[1)]
  - 128 Kbyte Local Data RAM (LDRAM)

1) Software configurable. Available options are described in the CPU chapter.

  – 0 Kbyte Data Cache (DACHE)
- On-chip SRAMs with parity error detection

2.2.3.2 High-performance 32-bit Peripheral Control Processor

The PCP is a flexible Peripheral Control Processor optimized for interrupt handling and thus unloading the CPU.

Features

- Data move between any two memory or I/O locations
- Data move until predefined limit supported
- Read-Modify-Write capabilities
- Full computation capabilities including basic MUL/DIV
- Read/move data and accumulate it to previously read data
- Read two data values and perform arithmetic or logical operation and store result
- Bit-handling capabilities (testing, setting, clearing)
- Flow control instructions (conditional/unconditional jumps, breakpoint)
- Dedicated Interrupt System
- PCP SRAMs with parity error detection
- PCP/FPI clock mode 1:1 and 2:1 available

Integrated PCP related On-Chip Memories

- 32 Kbyte Code Memory (CMEM)
- 16 Kbyte Parameter Memory (PRAM)

2.3 On-Chip System Units

The TC1797 microcontroller offers several versatile on-chip system peripheral units such as DMA controller, embedded Flash module, interrupt system and ports.

2.3.1 Flexible Interrupt System

The TC1797 includes a programmable interrupt system with the following features:

Features

- Fast interrupt response
- Independent interrupt systems for CPU and PCP
- Each SRN can be mapped to the CPU or PCP interrupt system
- Flexible interrupt-prioritizing scheme with 255 interrupt priority levels per interrupt system

2.3.2 Direct Memory Access Controller

The TC1797 includes a fast and flexible DMA controller with 16 independant DMA channels (two DMA Move Engines).

Features

- 8 independent DMA channels
  - 8 DMA channels in the DMA Sub-Block
  - Up to 16 selectable request inputs per DMA channel
  - 2-level programmable priority of DMA channels within the DMA Sub-Block
  - Software and hardware DMA request
  - Hardware requests by selected on-chip peripherals and external inputs
- 3-level programmable priority of the DMA Sub-Block at the on chip bus interfaces
- Buffer capability for move actions on the buses (at least 1 move per bus is buffered)
- Individually programmable operation modes for each DMA channel
  - Single Mode: stops and disables DMA channel after a predefined number of DMA transfers
  - Continuous Mode: DMA channel remains enabled after a predefined number of DMA transfers; DMA transaction can be repeated
  - Programmable address modification
  - Two shadow register modes (with / w/o automatic re-set and direct write access).
- Full 32-bit addressing capability of each DMA channel
  - 4 Gbyte address range
  - Data block move supports > 32 Kbyte moves per DMA transaction
  - Circular buffer addressing mode with flexible circular buffer sizes
- Programmable data width of DMA transfer/transaction: 8-bit, 16-bit, or 32-bit
- Register set for each DMA channel

  - Source and destination address register
  - Channel control and status register
  - Transfer count register
- Flexible interrupt generation (the service request node logic for the MLI channel is also implemented in the DMA module)
- DMA module is working on SPB frequency, LMB interface on LMB frequency.
- Dependant on the target/destination address, Read/write requests from the Move Engine are directed to the SPB, LMB, MLI or to the the Cerberus.

2.3.3 System Timer

The TC1797's STM is designed for global system timing applications requiring both high precision and long range.

Features

- Free-running 56-bit counter
- All 56 bits can be read synchronously
- Different 32-bit portions of the 56-bit counter can be read synchronously
- Flexible interrupt generation based on compare match with partial STM content
- Driven by maximum 90 MHz (= f_{SYS}, default after reset = $f_{SYS}/2$)
- Counting starts automatically after a reset operation
- STM registers are reset by an application reset if bit ARSTDIS.STMDIS is cleared. If bit ARSTDIS.STMDIS is set, the STM is not reset.
- STM can be halted in debug/suspend mode

Special STM register semantics provide synchronous views of the entire 56-bit counter, or 32-bit subsets at different levels of resolution.

The maximum clock period is $2^{56} \times f_{STM}$. At f_{STM} = 90 MHz, for example, the STM counts 25.39 years before overflowing. Thus, it is capable of continuously timing the entire expected product life time of a system without overflowing.

In case of a power-on reset, a watchdog reset, or a software reset, the STM is reset. After one of these reset conditions, the STM is enabled and immediately starts counting up. It is not possible to affect the content of the timer during normal operation of the TC1797.

The STM can be optionally disabled for power-saving purposes, or suspended for debugging purposes via its clock control register. In suspend mode of the TC1797 (initiated by writing an appropriate value to STM_CLC register), the STM clock is stopped but all registers are still readable.

Due to the 56-bit width of the STM, it is not possible to read its entire content with one instruction. It needs to be read with two load instructions. Since the timer would continue to count between the two load operations, there is a chance that the two values read are not consistent (due to possible overflow from the low part of the timer to the high part between the two read operations). To enable a synchronous and consistent reading of the STM content, a capture register (STM_CAP) is implemented. It latches the content of the high part of the STM each time when one of the registers STM_TIM0 to STM_TIM5 is read. Thus, STM_CAP holds the upper value of the timer at exactly the same time when the lower part is read. The second read operation would then read the content of the STM_CAP to get the complete timer value.

The content of the 56-bit System Timer can be compared against the content of two compare values stored in the STM_CMP0 and STM_CMP1 registers. Interrupts can be generated on a compare match of the STM with the STM_CMP0 or STM_CMP1 registers.

Figure 2 provides an overview on the STM module. It shows the options for reading parts of STM content.

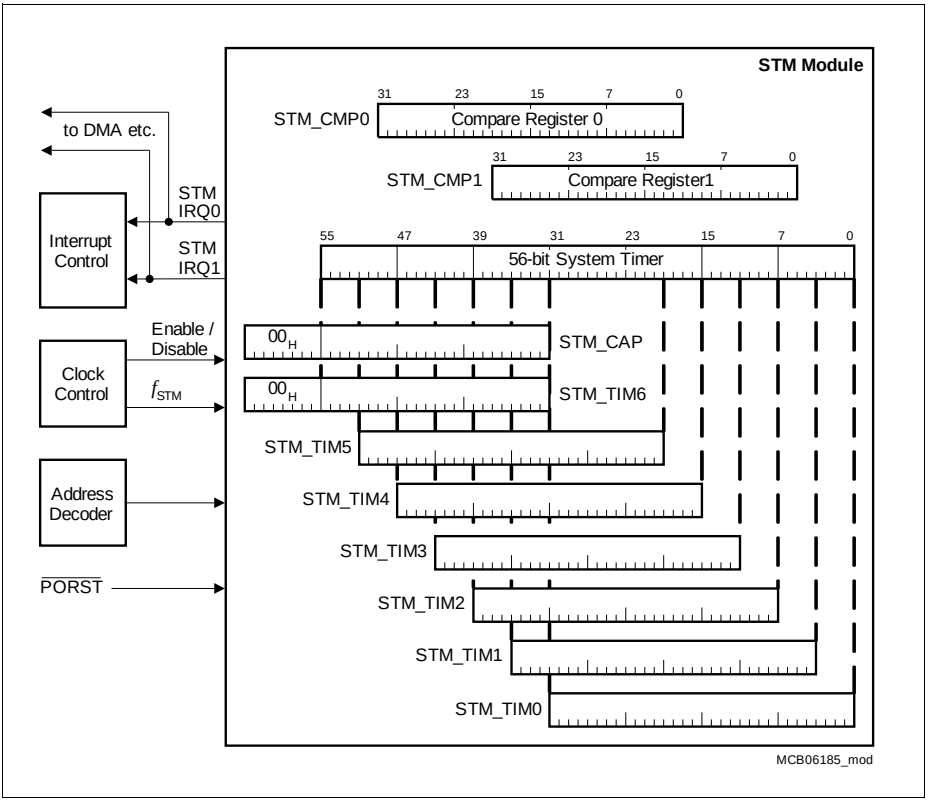


Figure 2 General Block Diagram of the STM Module Registers

2.3.4 System Control Unit

The following SCU introduction gives an overview about the TC1797 System Control Unit (SCU) For Information about the SCU see chapter 3.

2.3.4.1 Clock Generation Unit

The Clock Generation Unit (CGU) allows a very flexible clock generation for the TC1797. During user program execution the frequency can be programmed for an optimal ratio between performance and power consumption.

2.3.4.2 Features of the Watchdog Timer

The main features of the WDT are summarized here.

- 16-bit Watchdog counter
- Selectable input frequency: $f_{FPI}/256$ or $f_{FPI}/16384$
- 16-bit user-definable reload value for normal Watchdog operation, fixed reload value for Time-Out and Prewarning Modes
- Incorporation of the ENDINIT bit and monitoring of its modifications
- Sophisticated Password Access mechanism with fixed and user-definable password fields
- Access Error Detection: Invalid password (during first access) or invalid guard bits (during second access) trigger the Watchdog reset generation
- Overflow Error Detection: An overflow of the counter triggers the Watchdog reset generation
- Watchdog function can be disabled; access protection and ENDINIT monitor function remain enabled
- Double Reset Detection

2.3.4.3 Reset Operation

The following reset request triggers are available:

- 1 External power-on hardware reset request trigger; $\overline{\text{PORST}}$, (cold reset)
- 2 External System Request reset triggers; $\overline{\text{ESR0}}$ and $\overline{\text{ESR1}}$,(warm reset)
- Watchdog Timer (WDT) reset request trigger, (warm reset)
- Software reset (SW), (warm reset)
- Debug (OCDS) reset request trigger, (warm reset)
- Resets via the JTAG interface

There are two basic types of reset request triggers:

- Trigger sources that do not depend on a clock, such as the $\overline{\text{PORST}}$. This trigger force the device into an asynchronous reset assertion independently of any clock. The activation of an asynchronous reset is asynchronous to the system clock, whereas its de-assertion is synchronized.

- Trigger sources that need a clock in order to be asserted, such as the input signals $\overline{ESR0}$, $\overline{ESR1}$, the WDT trigger, the parity trigger, or the SW trigger.

2.3.4.4 External Interface

The SCU provides interface pads for system purpose. Various functions are covered by these pins. Due to the different tasks some of the pads can not be shared with other functions but most of them can be shared with other functions. The following functions are covered by the SCU controlled pads:

- Reset request triggers
- Reset indication
- Trap request triggers
- Interrupt request triggers
- Non SCU module triggers

The first three points are covered by the ESR pads and the last two points by the ERU pads.

2.3.4.5 Die Temperature Measurement

The Die Temperature Sensor (DTS) generates a measurement result that indicates directly the current temperature. The result of the measurement can be read via an DTS register.

2.3.5 General Purpose I/O Ports and Peripheral I/O Lines

The TC1797 includes a flexible Ports structure with the following features:

Features

- Digital General-Purpose Input/Output (GPIO) port lines
- Input/output functionality individually programmable for each port line
- Programmable input characteristics (pull-up, pull-down, no pull device)
- Programmable output driver strength for EMI minimization (weak, medium, strong)
- Programmable output characteristics (push-pull, open drain)
- Programmable alternate output functions
- Output lines of each port can be updated port-wise or set/reset/toggled bit-wise

2.3.6 Program Memory Unit (PMU)

The devices of the AudoF family contain at least one Program Memory Unit. This is named “PMU0”. Some devices contain additional PMUs which are named “PMU1”, …

In the TC1797, the PMU0 contains the following submodules:

- The Flash command and fetch control interface for Program Flash and Data Flash.
- The Overlay RAM interface with Online Data Acquisition (OLDA) support.

- The Boot ROM interface.
- The Emulation Memory interface.
- The Local Memory Bus LMB slave interface.

Following memories are controlled by and belong to the PMU0:

- 2 Mbyte of Program Flash memory (PFlash)
- 64 Kbyte of Data Flash memory (DFlash, represents 16 Kbyte EEPROM)
- 16 Kbyte of Boot ROM (BROM)
- 8 Kbyte Overlay RAM (OVRAM)

In the TC1797 an additional PMU is included with only a subset of PMU0's submodules:

- The Flash command and fetch control interface but only for Program Flash.
- The Local Memory Bus LMB slave interface.

The following memories are controlled and belong to the PMU1:

- 2 Mbyte of Program Flash memory (PFlash).

Because of its independence from PMU0 this second PMU enables additional functionality: Read while Write (RWW), Write while Write (WWW) or concurrent data and instruction accesses, if those are operating on different PMUs.

The following figure shows the block diagram of the PMU0:

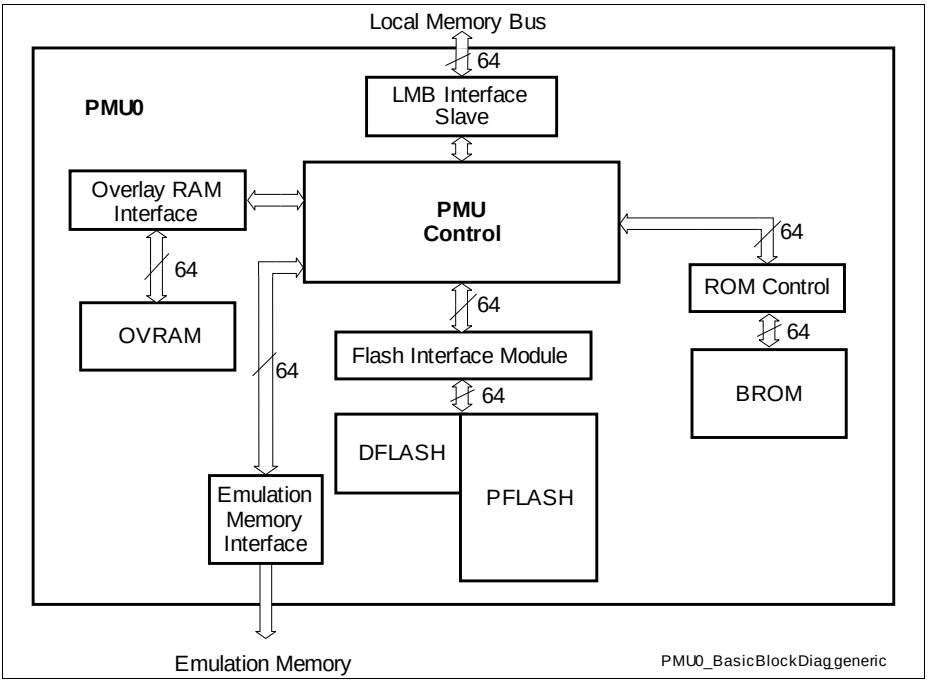


Figure 3 PMU0 Basic Block Diagram

As described before the PMU1 is reduced to the PFLASH and its controlling submodules.

2.3.6.1 Boot ROM

The internal 16 Kbyte Boot ROM (BROM) is divided into two parts, used for:

- firmware (Boot ROM), and
- factory test routines (Test ROM).

The different sections of the firmware in Boot ROM provide startup and boot operations after reset. The TestROM is reserved for special routines, which are used for testing, stressing and qualification of the component.

2.3.6.2 Overlay RAM and Data Acquisition

The overlay memory OVRAM is provided in the PMU especially for redirection of data accesses to program memory to the OVRAM by using the data overlay function. The data overlay functionality itself is controlled in the DMI module.

For online data acquisition (OLDA) of application or calibration data a virtual 32 KB memory range is provided which can be accessed without error reporting. Accesses to this OLDA range can also be redirected to an overlay memory.

2.3.6.3 Emulation Memory Interface

In TC1797 Emulation Device, an Emulation Memory (EMEM) is provided, which can fully be used for calibration via program memory or OLDA overlay. The Emulation Memory interface shown in **Figure 4** is a 64-bit wide memory interface that controls the CPU-accesses to the Emulation Memory in the TC1797 Emulation Device. In the TC1797 production device, the EMEM interface is always disabled.

2.3.6.4 Tuning Protection

Tuning protection is required by the user to absolutely protect control data (e.g. for engine control), serial number and user software, stored in the Flash, from being manipulated, and to safely detect changed or disturbed data. For the internal Flash, these protection requirements are excellently fulfilled in the TC1797 with

- Flash read and write protection with user-specific protection levels, and with
- dedicated HW and firmware, supporting the internal Flash read protection, and with
- the Alternate Boot Mode.

Special tuning protection support is provided for external Flash, which must also be protected.

2.3.6.5 Program and Data Flash

The embedded Flash modules of PMU0 includes 2 Mbyte of Flash memory for code or constant data (called Program Flash) and additionally 64 Kbyte of Flash memory used for emulation of EEPROM data (called Data Flash). The Program Flash is realized as one independent Flash bank, whereas the Data Flash is built of two Flash banks, allowing the following combinations of concurrent Flash operations:

- Read code or data from Program Flash, while one bank of Data Flash is busy with a program or erase operation.
- Read data from one bank of Data Flash, while the other bank of Data Flash is busy with a program or erase operation.
- Program one bank of Data Flash while erasing the other bank of Data Flash, read from Program Flash.

In TC1797 the PMU1 contains 2 Mbyte of Program Flash realized as one Flash bank. It does not contain any Data Flash.

Since in TC1797 the two PMUs can work in parallel, further combinations of concurrent operations are supported if those are operating on Flash modules in different PMUs, e.g.

- Read data from Flash1 while accessing code from Flash0.
- Read code or data from one Flash while the other Flash is busy with program or erase operation.
- Both Flash modules are concurrently busy with program or erase operation.

Both, the Program Flash and the Data Flash, provide error correction of single-bit errors within a 64-bit read double-word, resulting in an extremely low failure rate. Read accesses to Program Flash are executed in 256-bit width, to Data Flash in 64-bit width (both plus ECC). Single-cycle burst transfers of up to 4 double-words and sequential prefetching with control of prefetch hit are supported for Program Flash.

The minimum programming width is the page, including 256 bytes in Program Flash and 128 bytes in Data Flash. Concurrent programming and erasing in Data Flash is performed using an automatic erase suspend and resume function.

A basic block diagram of the Flash Module is shown in the following figure.

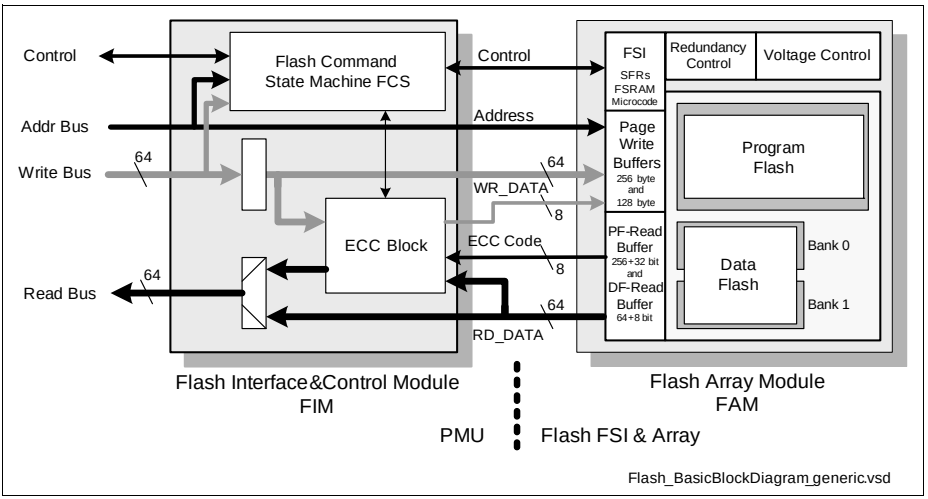


Figure 4 Basic Block Diagram of Flash Module

All Flash operations are controlled simply by transferring command sequences to the Flash which are based on JEDEC standard. This user interface of the embedded Flash is very comfortable, because all operations are controlled with high level commands, such as “Erase Sector”. State transitions, such as termination of command execution, or errors are reported to the user by maskable interrupts. Command sequences are

normally written to Flash by the CPU, but may also be issued by the DMA controller (or OCDS).

The Flash also features an advanced read/write protection architecture, including a read protection for the whole Flash array (optionally without Data Flash) and separate write protection for all sectors (only Program Flash). Write protected sectors can be made re-programmable (enabled with passwords), or they can be locked for ever (ROM function). Each sector can be assigned to up to three different users for write protection. The different users are organized hierarchically.

Program Flash Features and Functions

- 2 Mbyte on-chip Program Flash in PMU0.
- 2 Mbyte on-chip Program Flash in PMU1.
- Any use for instruction code or constant data.
- Double Flash module system approach:
  - Concurrent read access of code and data.
  - Read while write (RWW).
  - Concurrent program/erase in both modules.
- 256 bit read interface (burst transfer operation).
- Dynamic correction of single-bit errors during read access.
- Transfer rate in burst mode: One 64-bit double-word per clock cycle.
- Sector architecture:
  - Eight 16 Kbyte, one 128 Kbyte and seven 256 Kbyte sectors.
  - Each sector separately erasable.
  - Each sector lockable for protection against erase and program (write protection).
- One additional configuration sector (not accessible to the user).
- Optional read protection for whole Flash, with sophisticated read access supervision. Combined with whole Flash write protection — thus supporting protection against Trojan horse programs.
- Sector specific write protection with support of re-programmability or locked forever.
- Comfortable password checking for temporary disable of write or read protection.
- User controlled configuration blocks (UCB) in configuration sector for keywords and for sector-specific lock bits (one block for every user; up to three users).
- Pad supply voltage (V_{DDP}) also used for program and erase (no VPP pin).
- Efficient 256 byte page program operation.
- All Flash operations controlled by CPU per command sequences (unlock sequences) for protection against unintended operation.
- End-of-busy as well as error reporting with interrupt and bus error trap.
- Write state machine for automatic program and erase, including verification of operation quality.
- Support of margin check.
- Delivery in erased state (read all zeros).
- Global and sector status information.

- Overlay support with SRAM for calibration applications.
- Configurable wait state selection for different CPU frequencies.
- Endurance = 1000; minimum 1000 program/erase cycles per physical sector; reduced endurance of 100 per 16 KB sector.
- Operating lifetime (incl. Retention): 20 years with endurance=1000.
- For further operating conditions see data sheet section “Flash Memory Parameters”.

Data Flash Features and Functions

Note: Only available in PMU0.

- 64 Kbyte on-chip Flash, configured in two independent Flash banks of equal size.
- 64 bit read interface.
- Erase/program one bank while data read access from the other bank.
- Programming one bank while erasing the other bank using an automatic suspend/resume function.
- Dynamic correction of single-bit errors during read access.
- Sector architecture:
  – Two sectors of equal size.
  – Each sector separately erasable.
- 128 byte pages to be written in one step.
- Operational control per command sequences (unlock sequences, same as those of Program Flash) for protection against unintended operation.
- End-of-busy as well as error reporting with interrupt and bus error trap.
- Write state machine for automatic program and erase.
- Margin check for detection of problematic Flash bits.
- Endurance = 30000 (can be device dependent); i.e. 30000 program/erase cycles per sector are allowed, with a retention of min. 5 years.
- Dedicated DFlash status information.
- Other characteristics: Same as Program Flash.

2.3.7 Data Access Overlay

The data overlay functionality provides the capability to redirect data accesses by the TriCore to program memory (internal Program Flash or external memory) to the Overlay SRAM in the PMU, or to the Emulation Memory in Emulation Device ED, or to the external memory. This functionality makes it possible, for example, to modify the application's test and calibration parameters (which are typically stored in the program memory) during run time of a program. Note that read and write data accesses from/to program memory are redirected.

Attention: As the address translation is implemented in the DMI, it is only effective for data accesses by the TriCore. Instruction fetches by the TriCore or accesses by any other master (including the debug interface) are not affected!

Note: The external memory can be used as overlay memory only in Emulation Devices "ED" with an EBU. Generally this feature is not supported in Production Devices "PD". However, this function is fully described here in this spec.

Summary of Features and Functions

- 16 overlay ranges ("blocks") configurable for Program Flash and external memory
- Support of 8 Kbyte embedded Overlay SRAM (OVRAM) in PMU
- Support of up to 512 Kbyte overlay/calibration memory in Emulation Device (EMEM)
- Support of up to 2 MB overlay memory in external memory (EBU space)
- Support of Online Data Acquisition into range of up to 32 KB and of its overlay
- Support of different overlay memory selections for every enabled overlay block
- Sizes of overlay blocks selectable from 16 byte to 2 Kbyte for redirection to OVRAM
- Sizes of overlay blocks selectable from 1 Kbyte to 128 Kbyte for redirection to EMEM or to external memory
- All configured overlay ranges can be enabled with only one register write access
- Programmable flush (invalidate) control for data cache in DMI

2.4 Development Support

Overview about the TC1797 development environment:

Complete Development Support

A variety of software and hardware development tools for the 32-bit microcontroller TC1797 are available from experienced international tool suppliers. The development environment for the Infineon 32-bit microcontroller includes the following tools:

- Embedded Development Environment for TriCore Products
- The TC1797 On-chip Debug Support (OCDS) provides a JTAG port for communication between external hardware and the system

- Flexible Peripheral Interconnect Buses (FPI Bus) for on-chip interconnections and its FPI Bus control unit (SBCU)
- The System Timer (STM) with high-precision, long-range timing capabilities
- The TC1797 includes a power management system, a watchdog timer as well as reset logic

2.5 On-Chip Peripheral Units of the TC1797

The TC1797 microcontroller offers several versatile on-chip peripheral units such as serial controllers, timer units, and Analog-to-Digital converters. Several I/O lines on the TC1797 ports are reserved for these peripheral units to communicate with the external world.

On-Chip Peripheral Units

- Two Asynchronous/Synchronous Serial Channels (ASC) with baud-rate generator, parity, framing and overrun error detection
- Two Synchronous Serial Channels (SSC) with programmable data length and shift direction
- Two Micro Second Bus Interfaces (MSC) for serial communication
- One CAN Module with four CAN nodes (MultiCAN) for high-efficiency data handling via FIFO buffering and gateway data transfer
- Two Micro Link Serial Bus Interfaces (MLI) for serial multiprocessor communication
- Two General Purpose Timer Arrays (GPTA) with a powerful set of digital signal filtering and timer functionality to accomplish autonomous and complex Input/Output management. One additional Local Timer Cell Array (LCTA).
- Three Analog-to-Digital Converter Units (ADC) with 8-bit, 10-bit, or 12-bit resolution.
- One fast Analog-to-Digital Converter Unit (FADC)
- One FlexRay™ module with 2 channels (E-Ray).
- One External Bus Interface (EBU)

2.5.1 Asynchronous/Synchronous Serial Interfaces

The TC1797 includes two Asynchronous/Synchronous Serial Interfaces, ASC0 and ASC1. Both ASC modules have the same functionality.

Figure 5 shows a global view of the Asynchronous/Synchronous Serial Interface (ASC).

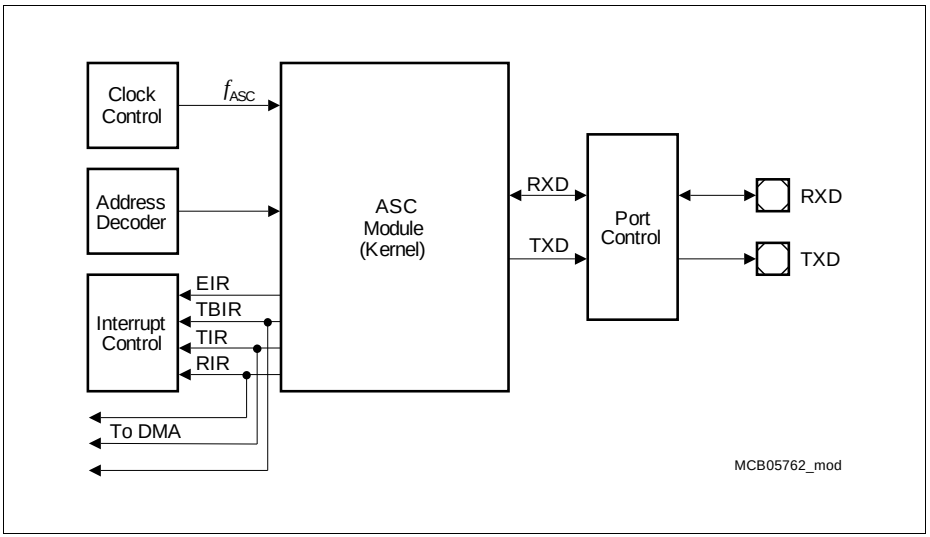


Figure 5 General Block Diagram of the ASC Interface

The ASC provides serial communication between the TC1797 and other microcontrollers, microprocessors, or external peripherals.

The ASC supports full-duplex asynchronous communication and half-duplex synchronous communication. In Synchronous Mode, data is transmitted or received synchronous to a shift clock that is generated by the ASC internally. In Asynchronous Mode, 8-bit or 9-bit data transfer, parity generation, and the number of stop bits can be selected. Parity, framing, and overrun error detection are provided to increase the reliability of data transfers. Transmission and reception of data is double-buffered. For multiprocessor communication, a mechanism is included to distinguish address bytes from data bytes. Testing is supported by a loop-back option. A 13-bit baud rate generator provides the ASC with a separate serial clock signal, which can be accurately adjusted by a prescaler implemented as fractional divider.

Features

- Full-duplex asynchronous operating modes
  - 8-bit or 9-bit data frames, LSB first
  - Parity-bit generation/checking
  - One or two stop bits
  - Baud rate from 5.625 Mbit/s to 1.34 bit/s (@ 90 MHz module clock)
  - Multiprocessor mode for automatic address/data byte detection
  - Loop-back capability
- Half-duplex 8-bit synchronous operating mode
  - Baud rate from 11.25 Mbit/s to 915.5 bit/s (@ 90 MHz module clock)
- Double-buffered transmitter/receiver
- Interrupt generation
  - On a transmit buffer empty condition
  - On a transmit last bit of a frame condition
  - On a receive buffer full condition
  - On an error condition (frame, parity, overrun error)
- Implementation features
  - Connections to DMA Controller
  - Connections of receiver input to GPTA (LTC) for baud rate detection and LIN break signal measuring

2.5.2 High-Speed Synchronous Serial Interfaces

The TC1797 includes two High-Speed Synchronous Serial Interfaces, SSC0 and SSC1. Both SSC modules have the same functionality.

Figure 6 shows a global view of the Synchronous Serial interface (SSC).

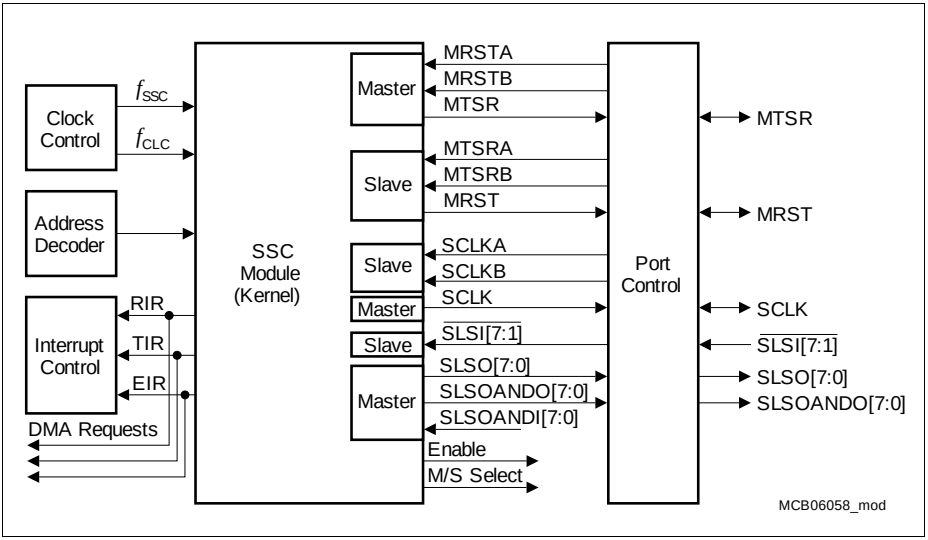


Figure 6 General Block Diagram of the SSC Interface

The SSC supports full-duplex and half-duplex serial synchronous communication up to 45 Mbit/s (@ 90 MHz module clock, Master Mode). The serial clock signal can be generated by the SSC itself (Master Mode) or can be received from an external master (Slave Mode). Data width, shift direction, clock polarity and phase are programmable. This allows communication with SPI-compatible devices. Transmission and reception of data are double-buffered. A shift clock generator provides the SSC with a separate serial clock signal. One slave select input is available for slave mode operation. Eight programmable slave select outputs (chip selects) are supported in Master Mode.

Features

- Master and Slave Mode operation
  - Full-duplex or half-duplex operation
  - Automatic pad control possible
- Flexible data format
  - Programmable number of data bits: 2 to 16 bits
  - Programmable shift direction: LSB or MSB shift first
  - Programmable clock polarity: Idle low or idle high state for the shift clock
  - Programmable clock/data phase: Data shift with leading or trailing edge of the shift clock
- Baud rate generation
  - Master Mode:
  - Slave Mode:
- Interrupt generation
  - On a transmitter empty condition
  - On a receiver full condition
  - On an error condition (receive, phase, baud rate, transmit error)
- Flexible SSC pin configuration
- Seven slave select inputs $\overline{\text{SLSI}}$[7:1] in Slave Mode
- Eight programmable slave select outputs SLSO[7:0] in Master Mode
  - Automatic SLSO generation with programmable timing
  - Programmable active level and enable control
  - Combinable with SLSO output signals from other SSC modules

2.5.3 Micro Second Channel Interface

The TC1797 includes two Micro Second Channel interfaces, MSC0 and MSC1. Both MSC modules have the same functionality.

Each Micro Second Channel (MSC) interface provides serial communication links typically used to connect power switches or other peripheral devices. The serial communication link includes a fast synchronous downstream channel and a slow asynchronous upstream channel. **Figure 7** shows a global view of the interface signals of an MSC interface.

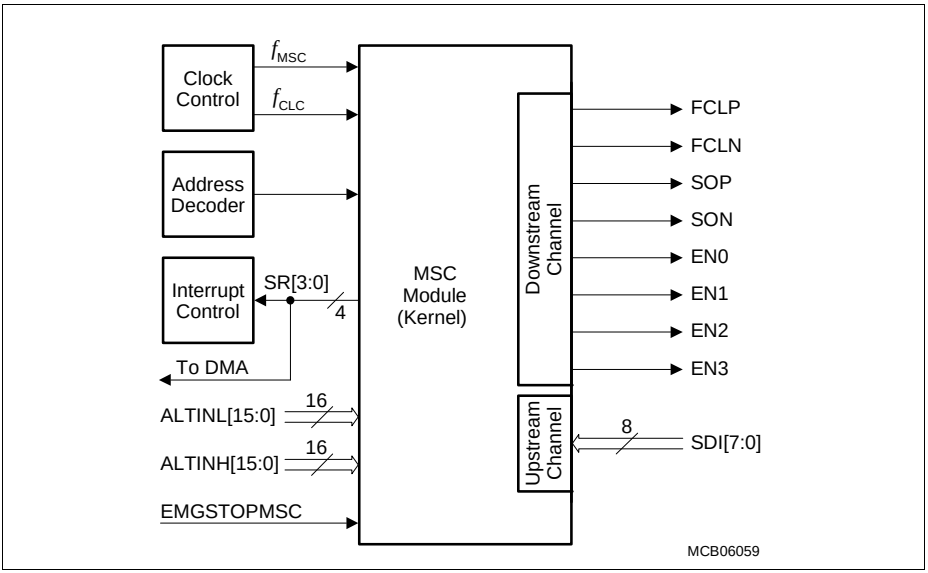


Figure 7 General Block Diagram of the MSC Interface

The downstream and upstream channels of the MSC module communicate with the external world via nine I/O lines. Eight output lines are required for the serial communication of the downstream channel (clock, data, and enable signals). One out of eight input lines SDI[7:0] is used as serial data input signal for the upstream channel. The source of the serial data to be transmitted by the downstream channel can be MSC register contents or data that is provided on the ALTINL/ALTINH input lines. These input lines are typically connected with other on-chip peripheral units (for example with a timer unit such as the GPTA). An emergency stop input signal makes it possible to set bits of the serial data stream to dedicated values in an emergency case.

Clock control, address decoding, and interrupt service request control are managed outside the MSC module kernel. Service request outputs are able to trigger an interrupt or a DMA request.

Features

- Fast synchronous serial interface to connect power switches in particular, or other peripheral devices via serial buses
- High-speed synchronous serial transmission on downstream channel
  - Serial output clock frequency: $f_{FCL} = f_{MSC}/2$ (f_{MSCmax} = 90 MHz)
  - Fractional clock divider for precise frequency control of serial clock f_{MSC}
  - Command, data, and passive frame types
  - Start of serial frame: Software-controlled, timer-controlled, or free-running
  - Programmable upstream data frame length (16 or 12 bits)
  - Transmission with or without SEL bit
  - Flexible chip select generation indicates status during serial frame transmission
  - Emergency stop without CPU intervention
- Low-speed asynchronous serial reception on upstream channel
  - Baud rate: f_{MSC} divided by 4, 8, 16, 32, 64, 128, or 256 (f_{MSCmax} = 90 MHz)
  - Standard asynchronous serial frames
  - Parity error checker
  - 8-to-1 input multiplexer for SDI lines
  - Built-in spike filter on SDI lines
- Selectable pin types of downstream channel interface:
  four LVDS differential output drivers or four digital GPIO pins

2.5.4 FlexRay™ Protocol Controller (Mod_Name)

The Mod_Name IP-module performs communication according to the FlexRay™ [1] protocol specification v2.1. With maximum specified clock the bitrate can be programmed to values up to 10 Mbit/s. Additional bus driver (BD) hardware is required for connection to the physical layer.

2.5.4.1 Mod_Name Kernel Description

Figure 2.5.4.1 shows a global view of the Mod_Name interface.

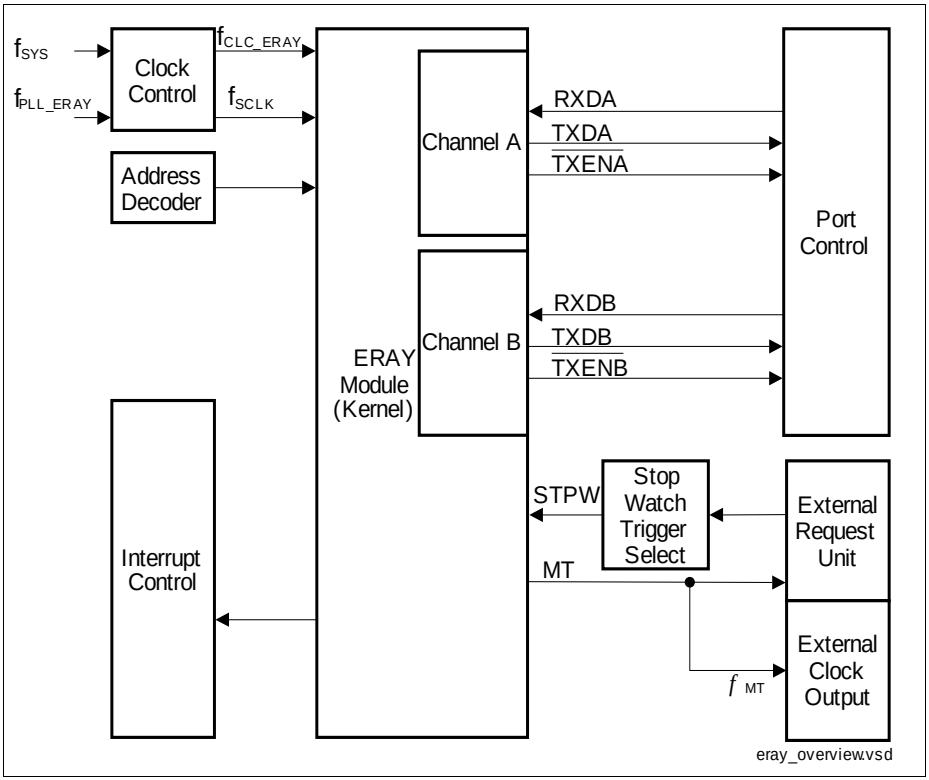


Figure 8 General Block Diagram of the Mod_Name Interface

1) Infineon®, Infineon Technologies®, are trademarks of Infineon Technologies AG. FlexRay™ is a trademark of FlexRay Consortium.

The Mod_Name module communicates with the external world via three I/O lines each channel. The RXDAx and RXDBx lines are the receive data input signals, TXDA and TXDB lines are the transmit output signals, TXENA and TXENB the transmit enable signals.

Clock control, address decoding, and service request control are managed outside the Mod_Name module kernel.

2.5.4.2 Overview

For communication on a FlexRay™ network, individual Message Buffers with up to 254 data byte are configurable. The message storage consists of a single-ported Message RAM that holds up to 128 Message Buffers. All functions concerning the handling of messages are implemented in the Message Handler. Those functions are the acceptance filtering, the transfer of messages between the two FlexRay™ Channel Protocol Controllers and the Message RAM, maintaining the transmission schedule as well as providing message status information.

The register set of the Mod_Name IP-module can be accessed directly by an external Host via the module's Host interface. These registers are used to control/configure/monitor the FlexRay™ Channel Protocol Controllers, Message Handler, Global Time Unit, System Universal Control, Frame and Symbol Processing, Network Management, Service Request Control, and to access the Message RAM via Input / Output Buffer.

The Mod_Name IP-module supports the following features:

- Conformance with FlexRay™ protocol specification v2.1
- Data rates of up to 10 Mbit/s on each channel
- Up to 128 Message Buffers configurable
- 8 Kbyte of Message RAM for storage of e.g. 128 Message Buffers with max. 48 byte data field or up to 30 Message Buffers with 254 byte Data Sections
- Configuration of Message Buffers with different payload lengths possible
- One configurable receive FIFO
- Each Message Buffer can be configured as receive buffer, as transmit buffer or as part of the receive FIFO
- Host access to Message Buffers via Input and Output Buffer.
  Input Buffer: Holds message to be transferred to the Message RAM
  Output Buffer: Holds message read from the Message RAM
- Filtering for slot counter, cycle counter, and channel
- Maskable module service requests
- Network Management supported
- Four service request lines
- Automatic delayed read access to Output Command Request Register (OBCR) if a data transfer from Message RAM to Output Shadow Buffer (initiated by a previous write access to the OBCR) is ongoing.

- Automatic delayed read access to Input Command Request Register (IBCR) if a data transfer from Input Shadow Buffer to Message RAM to (initiated by a previous write access to the IBCR) is ongoing.
- Four Input Buffer for building up transmission Frames in parallel.
- Flag indicating which Input Buffer is currently accessible by the host.

2.5.5 MultiCAN Controller

The MultiCAN module provides four independent CAN nodes, representing four serial communication interfaces. The number of available message objects is 128.

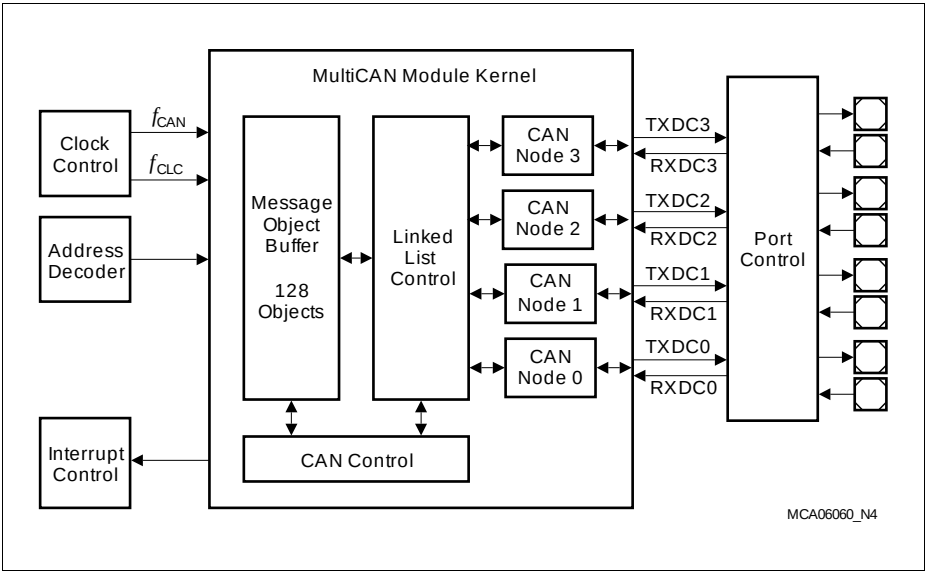


Figure 9 Overview of the MultiCAN Module

The MultiCAN module contains four independently operating CAN nodes with Full-CAN functionality that are able to exchange Data and Remote Frames via a gateway function. Transmission and reception of CAN frames is handled in accordance to CAN specification V2.0 B (active). Each CAN node can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

All four CAN nodes share a common set of message objects. Each message object can be individually allocated to one of the CAN nodes. Besides serving as a storage container for incoming and outgoing frames, message objects can be combined to build gateways between the CAN nodes or to set up a FIFO buffer.

The message objects are organized in double-chained linked lists, where each CAN node has its own list of message objects. A CAN node stores frames only into message objects that are allocated to the message object list of the CAN node, and it transmits only messages belonging to this message object list. A powerful, command-driven list controller performs all message object list operations.

The bit timings for the CAN nodes are derived from the module timer clock (f_{CAN}) and are programmable up to a data rate of 1 Mbit/s. External bus transceivers are connected to a CAN node via a pair of receive and transmit pins.

Features

- Compliant with ISO 11898
- CAN functionality according to CAN specification V2.0 B active
- Dedicated control registers for each CAN node
- Data transfer rates up to 1 Mbit/s
- Flexible and powerful message transfer control and error handling capabilities
- Advanced CAN bus bit timing analysis and baud rate detection for each CAN node via a frame counter
- Full-CAN functionality: A set of 128 message objects can be individually
  - Allocated (assigned) to any CAN node
  - Configured as transmit or receive object
  - Setup to handle frames with 11-bit or 29-bit identifier
  - Identified by a timestamp via a frame counter
  - Configured to remote monitoring mode
- Advanced Acceptance Filtering
  - Each message object provides an individual acceptance mask to filter incoming frames.
  - A message object can be configured to accept standard or extended frames or to accept both standard and extended frames.
  - Message objects can be grouped into four priority classes for transmission and reception.
  - The selection of the message to be transmitted first can be based on frame identifier, IDE bit and RTR bit according to CAN arbitration rules, or on its order in the list.
- Advanced message object functionality
  - Message objects can be combined to build FIFO message buffers of arbitrary size, limited only by the total number of message objects.
  - Message objects can be linked to form a gateway that automatically transfers frames between 2 different CAN buses. A single gateway can link any two CAN nodes. An arbitrary number of gateways can be defined.
- Advanced data management
  - The message objects are organized in double-chained lists.
  - List reorganizations can be performed at any time, even during full operation of the CAN nodes.
  - A powerful, command-driven list controller manages the organization of the list structure and ensures consistency of the list.
  - Message FIFOs are based on the list structure and can easily be scaled in size during CAN operation.
  - Static allocation commands offer compatibility with MultiCAN applications that are not list-based.
- Advanced interrupt handling

– Up to 16 interrupt output lines are available. Interrupt requests can be routed individually to one of the 16 interrupt output lines.
– Message post-processing notifications can be combined flexibly into a dedicated register field of 256 notification bits.

2.5.6 Micro Link Serial Bus Interface

This TC1797 contains two Micro Link Serial Bus Interfaces, MLI0 and MLI1.

The Micro Link Interface (MLI) is a fast synchronous serial interface to exchange data between microcontrollers or other devices, such as stand-alone peripheral components. **Figure 10** shows how two microcontrollers are typically connected together via their MLI interfaces.

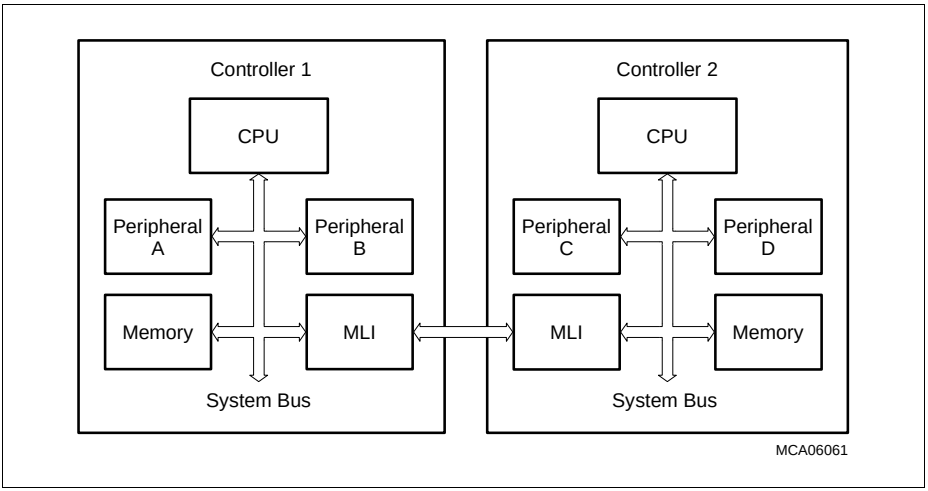


Figure 10 Typical Micro Link Interface Connection

Features

- Synchronous serial communication between an MLI transmitter and an MLI receiver
- Different system clock speeds supported in MLI transmitter and MLI receiver due to full handshake protocol (4 lines between a transmitter and a receiver)
- Fully transparent read/write access supported (= remote programming)
- Complete address range of target device available
- Specific frame protocol to transfer commands, addresses and data
- Error detection by parity bit
- 32-bit, 16-bit, or 8-bit data transfers supported
- Programmable baud rate: $f_{MLI}/2$ (max. $f_{MLI} = f_{SYS}$)
- Address range protection scheme to block unauthorized accesses
- Multiple receiving devices supported

Figure 11 shows a general block diagram of the MLI module.

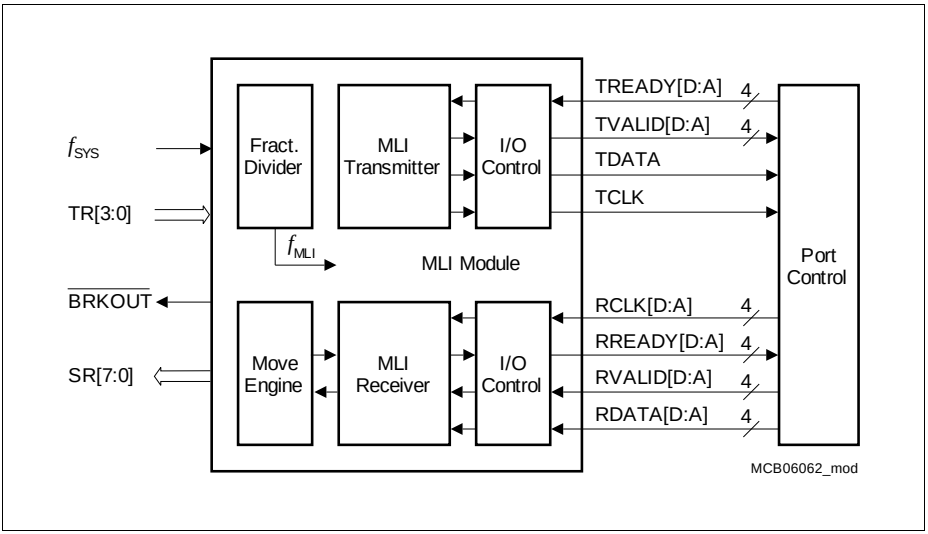


Figure 11 General Block Diagram of the MLI Modules

The MLI transmitter and MLI receiver communicate with other MLI receivers and MLI transmitters via a four-line serial connection each. Several I/O lines of these connections are available outside the MLI module kernel as a four-line output or input vector with index numbering A, B, C and D. The MLI module internal I/O control blocks define which signal of a vector is actually taken into account and also allow polarity inversions (to adapt to different physical interconnection means)

2.5.7 General Purpose Timer Array (GPTA)

The TC1797 contains the General Purpose Timer Array (GPTA0), plus the additional Local Timer Cell Array (LTCA2). **Figure 12** shows a global view of the GPTA modules.

The GPTA provides a set of timer, compare, and capture functionalities that can be flexibly combined to form signal measurement and signal generation units. They are optimized for tasks typical of engine, gearbox, and electrical motor control applications, but can also be used to generate simple and complex signal waveforms required for other industrial applications.

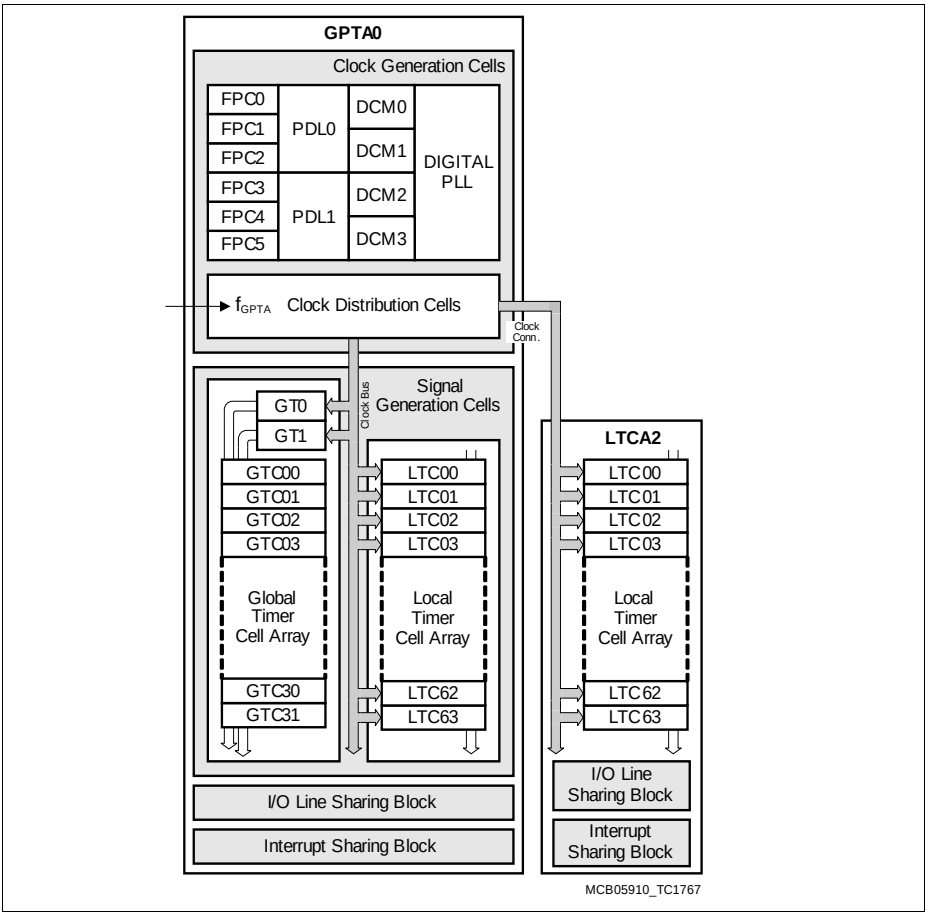


Figure 12 General Block Diagram of the GPTA Modules in the TC1797

2.5.7.1 Functionality of GPTA0

The General Purpose Timer Array (GPTA0) provides a set of hardware modules required for high-speed digital signal processing:

- Filter and Prescaler Cells (FPC) support input noise filtering and prescaler operation.
- Phase Discrimination Logic units (PDL) decode the direction information output by a rotation tracking system.
- Duty Cycle Measurement Cells (DCM) provide pulse-width measurement capabilities.
- A Digital Phase Locked Loop unit (PLL) generates a programmable number of GPTA module clock ticks during an input signal's period.
- Global Timer units (GT) driven by various clock sources are implemented to operate as a time base for the associated Global Timer Cells.
- Global Timer Cells (GTC) can be programmed to capture the contents of a Global Timer on an external or internal event. A GTC may also be used to control an external port pin depending on the result of an internal compare operation. GTCs can be logically concatenated to provide a common external port pin with a complex signal waveform.
- Local Timer Cells (LTC) operating in Timer, Capture, or Compare Mode may also be logically tied together to drive a common external port pin with a complex signal waveform. LTCs – enabled in Timer Mode or Capture Mode – can be clocked or triggered by various external or internal events.
- On-chip Trigger and Gating Signals (OTGS) can be configured to provide trigger or gating signals to integrated peripherals.

Input lines can be shared by an LTC and a GTC to trigger their programmed operation simultaneously.

The following list summarizes the specific features of the GPTA units.

Clock Generation Unit

- Filter and Prescaler Cell (FPC)
  - Six independent units
  - Three basic operating modes:
    Prescaler, Delayed Debounce Filter, Immediate Debounce Filter
  - Selectable input sources:
    Port lines, GPTA module clock, FPC output of preceding FPC cell
  - Selectable input clocks:
    GPTA module clock, prescaled GPTA module clock, DCM clock, compensated or uncompensated PLL clock.
  - $f_{GPTA}/2$ maximum input signal frequency in Filter Modes
- Phase Discriminator Logic (PDL)
  - Two independent units
  - Two operating modes (2- and 3- sensor signals)

  - f_{GPTA}/4 maximum input signal frequency in 2-sensor Mode, f_{GPTA}/6 maximum input signal frequency in 3-sensor Mode
- Duty Cycle Measurement (DCM)
  - Four independent units
  - 0 - 100% margin and time-out handling
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency
- Digital Phase Locked Loop (PLL)
  - One unit
  - Arbitrary multiplication factor between 1 and 65535
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency
- Clock Distribution Unit (CDU)
  - One unit
  - Provides nine clock output signals:
    f_{GPTA}, divided f_{GPTA} clocks, FPC1/FPC4 outputs, DCM clock, LTC prescaler clock

Signal Generation Unit

- Global Timers (GT)
  - Two independent units
  - Two operating modes (Free-Running Timer and Reload Timer)
  - 24-bit data width
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency
- Global Timer Cell (GTC)
  - 32 units related to the Global Timers
  - Two operating modes (Capture, Compare and Capture after Compare)
  - 24-bit data width
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency
- Local Timer Cell (LTC)
  - 64 independent units
  - Three basic operating modes (Timer, Capture and Compare) for 63 units
  - Special compare modes for one unit
  - 16-bit data width
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency

Interrupt Sharing Unit

- 286 interrupt sources, generating up to 92 service requests

On-chip Trigger Unit

- 16 on-chip trigger signals

I/O Sharing Unit

- Interconnecting inputs and outputs from internal clocks, FPC, GTC, LTC, ports, and MSC interface

2.5.7.2 Functionality of LTCA2

The Local Timer Cell Array (LTCA2) provides a set of hardware modules required for high-speed digital signal processing:

- Local Timer Cells (LTC) operating in Timer, Capture, or Compare Mode may also be logically tied together to drive a common external port pin with a complex signal waveform. LTCs – enabled in Timer Mode or Capture Mode – can be clocked or triggered by various external or internal events.

The following list summarizes the specific features of the LTCA unit.

The Local Timer Arrays (LTCA2) provides a set of hardware modules required for high-speed digital signal processing:

Signal Generation Unit

- Local Timer Cell (LTC)
  - 32 independent units
  - Three basic operating modes (Timer, Capture and Compare) for 63 units
  - Special compare modes for one unit
  - 16-bit data width
  - f_{GPTA} maximum resolution
  - $f_{GPTA}/2$ maximum input signal frequency

I/O Sharing Unit

- Interconnecting inputs and outputs from internal clocks, LTC, ports, and MSC interface

2.5.8 Analog-to-Digital Converters

The TC1797 includes three Analog to Digital Converter modules (ADC0, ADC1, ADC2) and one Fast Analog to Digital Converter (FADC).

2.5.8.1 ADC Block Diagram

The analog to digital converter module (ADC) allows the conversion of analog input values into discrete digital values based on the successive approximation method.
This module contains 3 independent kernels (ADC0, ADC1, ADC2) that can operate autonomously or can be synchronized to each other. An ADC kernel is a unit used to convert an analog input signal (done by an analog part) and provides means for triggering conversions, data handling and storage (done by a digital part).

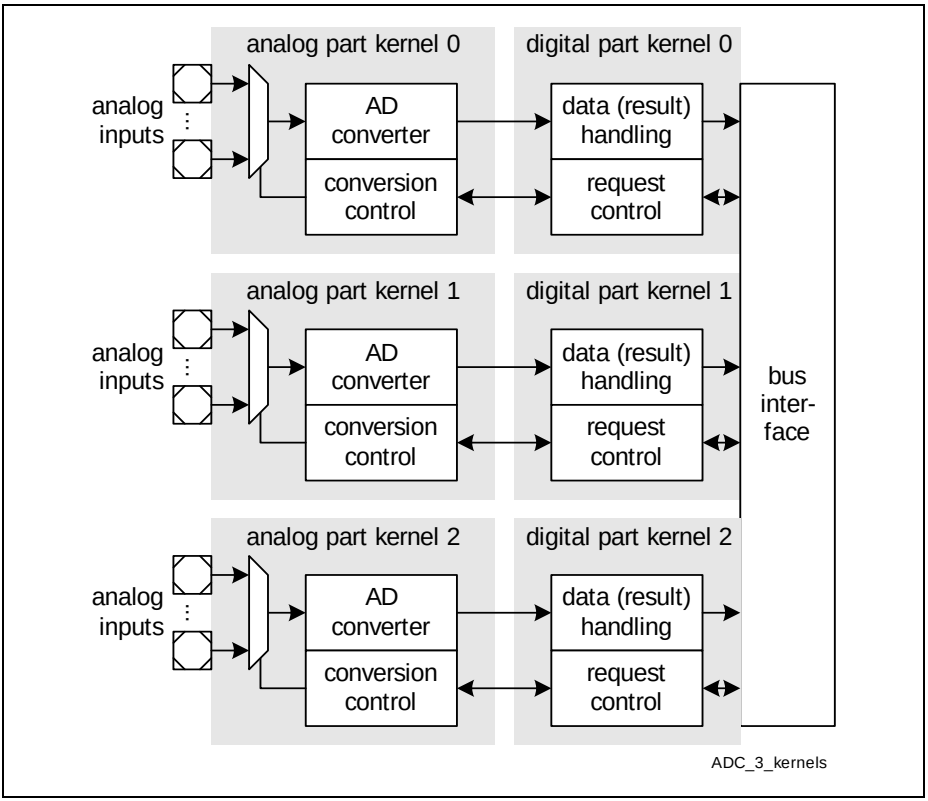


Figure 13 ADC Module with three ADC Kernels

Features of the analog part of each ADC kernel:

- Input voltage range from 0V to analog supply voltage
- Analog supply voltage range from 3.3 V to 5 V (single supply)
  (5V nominal supply voltage, performance degradation accepted for lower voltages)
- Input multiplexer width of 16 possible analog input channels (not all of them are necessarily available on pins)
- Performance for 12 bit resolution (@f_{ADCI} = 10 MHz):
  - conversion time about 2µs, TUE[1] of ±4 LSB_{12} @ operating voltage 5 V
  - conversion time about 2µs, TUE of ±4 LSB_{12} @ operating voltage 3.3 V
- V_{AREF} and 1 alternative reference input at channel 0
- Programmable sample time (in periods of f_{ADCI})
- Wide range of accepted analog clock frequencies f_{ADCI}
- Multiplexer test mode (channel 7 input can be connected to ground via a resistor for test purposes during run time by specific control bit)
- Power saving mechanisms

Features of the digital part of each ADC kernel:

- Independent result registers (16 independent registers)
- 5 conversion request sources (e.g. for external events, auto-scan, programmable sequence, etc.)
- Synchronization of the ADC kernels for concurrent conversion starts
- Control an external analog multiplexer, respecting the additional set up time
- Programmable sampling times for different channels
- Possibility to cancel running conversions on demand with automatic restart
- Flexible interrupt generation (possibility of DMA support)
- Limit checking to reduce interrupt load
- Programmable data reduction filter by adding conversion results
- Support of conversion data FIFO
- Support of suspend and power down modes
- Individually programmable reference selection for each channel (with exception of dedicated channels always referring to V_{AREF})

1) This value reflects the ADC module capability in an adapted electrical environment, e.g. characterized by “clean” routing of analog and digital signals and separation of analog and digital PCB areas, low noise on analog power supply (< 30mV), low switching activity of digital pins near to the ADC, etc.

2.5.8.2 FADC Short Description

General Features

- Extreme fast conversion, 21 cycles of f_{FADC} clock (262.5 ns @ f_{FADC} = 80 MHz)
- 10-bit A/D conversion (higher resolution can be achieved by averaging of consecutive conversions in digital data reduction filter)
- Successive approximation conversion method
- Two differential input channels with impedance control available on dedicated pins
- Two differential input channels with impedance control overlaid with ADC1 inputs
- Each differential input channel can also be used as single-ended input
- Offset calibration support for each channel
- Programmable gain of 1, 2, 4, or 8 for each channel
- Free-running (Channel Timers) or triggered conversion modes
- Trigger and gating control for external signals
- Built-in Channel Timers for internal triggering
- Channel timer request periods independently selectable for each channel
- Selectable, programmable digital anti-aliasing and data reduction filter block with four independent filter units

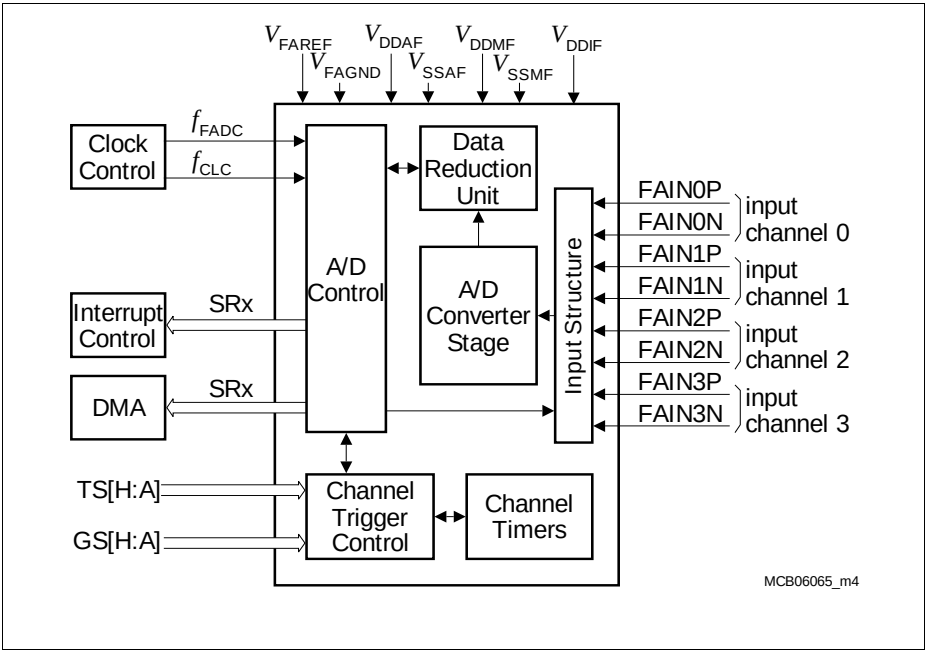


Figure 14 Block Diagram of the FADC Module with 4 Input Channels

As shown in **Figure 14**, the main FADC functional blocks are:

- An Input Structure containing the differential inputs and impedance control.
- An A/D Converter Stage responsible for the analog-to-digital conversion including an input multiplexer to select between the channel amplifiers
- A Data Reduction Unit containing programmable anti-aliasing and data reduction filters
- A Channel Trigger Control block determining the trigger and gating conditions for the FADC channels
- A Channel Timer for each channel to independently trigger the conversions
- An A/D Control block responsible for the overall FADC functionality

FADC Power Supply and References

The FADC module is supplied by the following power supply and reference voltage lines:

- V_{DDMF} / V_{SSMF}: FADC Analog Channel Amplifier Power Supply (3.3 V)
- V_{DDIF} / V_{SSMF}: FADC Analog Input Stage Power Supply (3.3 - 5 V),
  the V_{DDIF} supply does not appear as supply pin, because it is internally connected to the V_{DDM} supply of the ADC that is sharing the FADC input pins.
- V_{DDAF} / V_{SSAF}: FADC Analog Part Power Supply (1.5 V),
  to be fed in externally
- V_{FAREF} / V_{FAGND}: FADC Reference Voltage (3.3 V max.) and FADC Reference Ground

Input Structure

The input structure of the FADC in the TC1797 contains:

- A differential analog input stage for each input channel to select the input impedance (differential or single-ended measurement) and to decouple the FADC input signal from the pins.
- Input channels 2 and 3 are overlaid with ADC1 input signals (AN28, AN29, AN30, AN31), whereas input channels 0 and 1 are available on dedicated input pins (AN32, AN33, AN34, AN35).
- A channel amplifier for each input channel with a settling time (about 5µs) when changing the characteristics of an input stage (changing between unused, differential, single-ended N, or single-ended P mode).

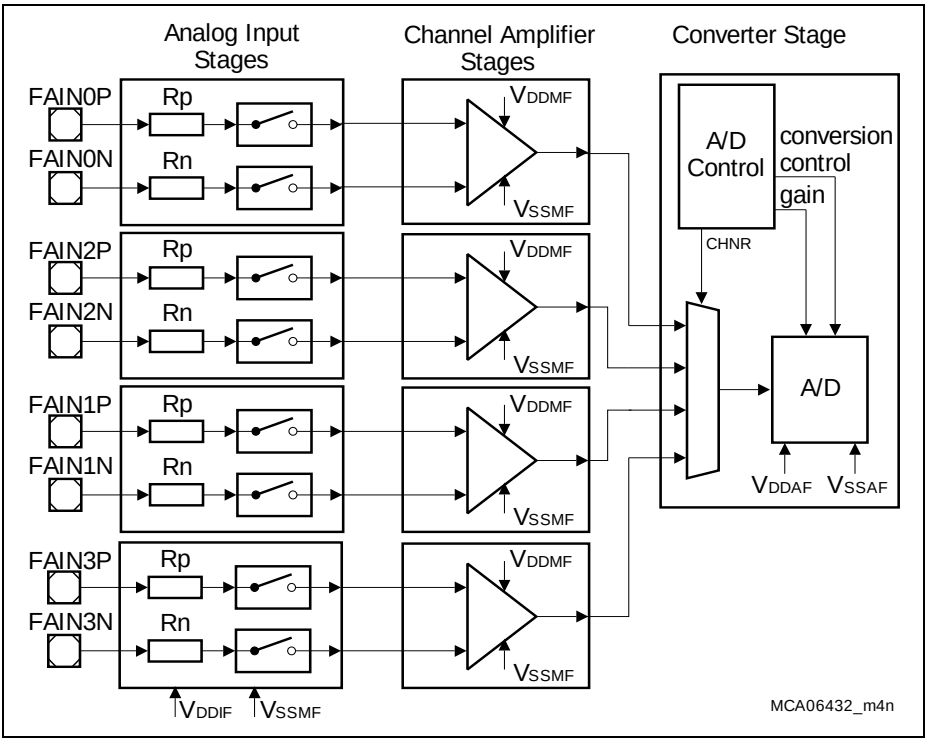


Figure 15 FADC Input Structure in TC1797

2.5.9 External Bus Interface

The External Bus Unit (EBU) of the TC1797 controls the accesses from peripheral units to external memories.

Features:

- 64-bit internal LMB interface
- 32-bit demultiplexed / 16-bit multiplexed external bus interface (3.3V, 2.5V)
  - Support for Intel-style and Motorola-style interface signals
  - Support for Burst Flash memory devices
  - Flexibly programmable access parameters
  - Programmable chip select lines
  - Little-endian support
- Examples for memories that has to be supported
  - Burst Flash:
  - Spansion: S29CD016, S29CD032
  - Spansion: S29CL032J1RFAM010 @3,3V
  - ST: M58BW016, M58BW032
  - ST: M58BW032GB B45ZA3T @3,3V
  - Flash (for 16 bit muxed mode):
  - http://www.spansion.com/products/Am29LV160B.html
  - SRAM (for 16 bit muxed mode):
  - http://www.idt.com/products/files/10372/71V016saautomotive.pdf
  - http://213.174.55.51/zmd.biz/pdf/ UL62H1616A.pdf
  - IDT 71V416YS15BEI
- Scalable external bus frequency
  - Derived from LMB frequency (f_{CPU}) divided by 1, 2, 3, or 4
  - Maximum 75 MHz[1)]
- Data buffering supported
  - Code prefetch buffer
  - Read/write buffer

2.6 On-Chip Debug Support (OCDS)

The TC1797 contains resources for different kinds of “debugging”, covering needs from software development to real-time-tuning. These resources are either embedded in specific modules (e.g. breakpoint logic of the TriCore) or part of a central peripheral (known as CERBERUS).

1) Maximum frequency of today available automotive Burst Flash devices.

2.6.1 On-Chip Debug Support

The classic software debug approach (start/stop, single-stepping) is supported by several features labelled “OCDS Level 1”:

- Run/stop and single-step execution independently for TriCore and PCP.
- Means to request all kinds of reset without usage of sideband pins.
- Halt-after-Reset for repeatable debug sessions.
- Different Boot modes to use application software not yet programmed to the Flash.
- A total of four hardware breakpoints for the TriCore based on instruction address, data address or combination of both.
- Unlimited number of software breakpoints (DEBUG instruction) for TriCore and PCP.
- Debug event generated by access to a specific address via the system bus.
- Tool access to all SFRs and internal memories independent of the Cores.
- Two central Break Switches to collect debug events from all modules (TriCore, PCP, DMA, BCU, break input pins) and distribute them selectively to breakable modules (TriCore, PCP, break output pins).
- Central Suspend Switch to suspend parts of the system (TriCore, PCP, Peripherals) instead if breaking them as reaction to a debug event.
- Dedicated interrupt resources to handle debug events inside TriCore (breakpoint trap, software interrupt) and Cerberus (can trigger PCP), e.g. for implementing Monitor programs.
- Access to all OCDS Level 1 resources also for TriCore and PCP themselves for debug tools integrated into the application code.
- Triggered Transfer of data in response to a debug event; if target is programmed to be a device interface simple variable tracing can be done.
- In depth performance analysis and profiling support given by the Emulation Device through MCDS Event Counters driven by a variety of trigger signals (e.g. cache hit, wait state, interrupt accepted).

2.6.2 Real Time Trace

For detailed tracing of the system’s behavior a pin-compatible Emulation Device will be available.[1)]

2.6.3 Calibration Support

Two main use cases are catered for by resources in addition the OCDS Level 1 infrastructure: Overlay of non-volatile on-chip memory and non-intrusive signaling:

- 8 KB SRAM for Overlay.
- Can be split into up to 16 blocks which can overlay independent regions of on-chip Data Flash.

1) The OCDS L2 interface of AudoNG is not available.

- Changing the configuration is triggered by a single SFR access to maintain consistency.
- Overlay configuration switch does not require the TriCore to be stopped or suspended.
- Invalidation of the Data Cache (maintaining write-back data) can be done concurrently with the same SFR.
- 256 KB additional Overlay RAM on Emulation Device.
- The 256 KB Trace memory of the Emulation Device can optionally be used for Overlay also.
- A dedicated trigger SFR with 32 independent status bits is provided to centrally post requests from application code to the host computer.
- The host is notified automatically when the trigger SFR is updated by the TriCore or PCP. No polling via a system bus is required.

2.6.4 Tool Interfaces

Three options exist for the communication channel between Tools (e.g. Debugger, Calibration Tool) and TC1797:

- Two wire DAP (Device Access Port) protocol for long connections or noisy environments.
- Four (or five) wire JTAG (IEEE 1149.1) for standardized manufacturing tests.
- CAN (plus software linked into the application code) for low bandwidth deeply embedded purposes.
- DAP and JTAG are clocked by the tool.
- Bit clock up to 40 MHz for JTAG, up to 80 MHz for DAP.
- Hot attach (i.e. physical disconnect/reconnect of the host connection without reset of the TC1797) for all interfaces.
- Infineon standard DAS (Device Access Server) implementation for seamless, transparent tool access over any supported interface.
- Lock mechanism to prevent unauthorized tool access to critical application code.

2.6.5 Self-Test Support

Some manufacturing tests can be invoked by the application (e.g. after power-on) if needed:

- Hardware-accelerated checksum calculation (e.g. for Flash content).
- RAM tests optimized for the implemented architecture.

2.6.6 FAR Support

To efficiently locate and identify faults after integration of a TC1797 into a system special functions are available:

- Boundary Scan (IEEE 1149.1) via JTAG and DAP.

- SSCM (Single Scan Chain Mode[1)]) for structural scan testing of the chip itself.

1) This function requires access to some device pins (e.g. $\overline{\text{TESTMODE}}$) in addition to those needed for OCDS.

3 Pinning

3.1 TC1797 Pin Definition and Functions: P/PG-BGA-416-10 / P/PG-BGA-416-27

Figure 16 is showing the TC1797 Logic Symbol for the package variants: P/PG-BGA-416-10 / P/PG-BGA-416-27.

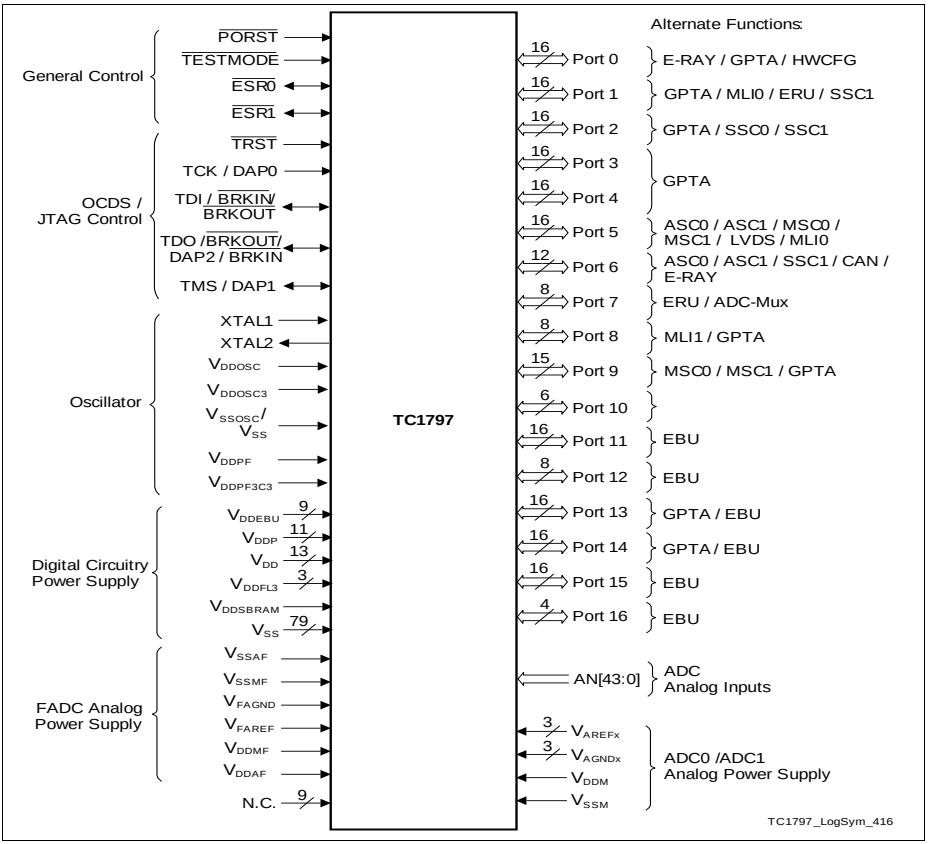


Figure 16 TC1797 Logic Symbol for the package variants P/PG-BGA-416-10 / P/PG-BGA-416-27

3.1.1 TC1797 P/PG-BGA-416-27P/PG-BGA-416-10 / Package Variant Pin Configuration

Figure 18 shows the TC1797 pin configuration for the P/PG-BGA-416-10 / P/PG-BGA-416-27 package variant.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	N.C.	P2.9	P2.13	P2.15	P0.14	P0.5	P0.2	P0.1	P0.0	P3.14	P3.5	P3.1	P5.1	P5.2	P5.7	P5.12	P5.15	V_{DDFL3}	P9.0	P9.3	P9.9	$\overline{ESR1}$	$\overline{ESR0}$	N.C.	V_{DDP}	V_{SS}	A
B	P2.6	P2.7	P2.10	P2.14	P0.9	P0.6	P0.4	P0.3	P3.15	P3.6	P3.3	P3.0	P5.0	P5.3	P5.6	P5.13	P5.14	V_{DDFL3}	P9.1	P9.2	P9.10	$\overline{PO}$ $\overline{RST}$	TEST MODE	V_{DDP}	V_{SS}	V_{DD}	B
C	P2.5	P2.8	P2.11	P2.12	P0.12	P0.10	P0.8	P0.7	P3.7	P3.10	P3.9	P3.4	P3.2	P5.5	P5.4	P5.9	P5.10	P5.11	P9.6	P9.8	P9.11	N.C.	V_{DDP}	V_{SS}	V_{DD}	P9.13	C
D	P2.4	P2.3	P2.2	P0.15	P0.13	P0.11	V_{DDP}	V_{SS}	V_{DD}	P3.8	P3.12	P3.13	P3.11	V_{DDP}	V_{SS}	V_{DD}	P5.8	P9.4	P9.5	P9.7	P9.12	V_{DDP}	V_{SS}	V_{DD}	TDO	P9.14	D
E	P6.12	P6.11	P6.6	P6.9																			V_{DD}	TCK	TDI	V_{DD} OSC3	E
F	P6.14	P6.10	P6.4	P6.8																			$\overline{TRST}$	TMS	V_{SS} OSC	V_{DD} OSC	F
G	P6.15	P6.13	P6.7	P6.5																			V_{DDPF}	V_{DDPF3}	XTAL 2	XTAL 1	G
H	P8.1	P8.0	V_{DDFL3}	V_{DD}																			V_{DDEBU}	V_{DDEBU}	V_{DDEBU}	V_{DDEBU}	H
J	P8.4	P8.3	P8.2	V_{SS}																			P11.3	P12.6	P12.7	P11.0	J
K	P8.7	P8.5	P8.6	V_{DDP}						V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}						P11.7	P11.4	P11.1	P11.2	K
L	P1.15	P1.14	P1.13	P1.11						V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}						V_{SS}	P11. 11	P11.5	P11.6	L
M	P1.10	P1.9	P1.8	P1.5						V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}						V_{DDEBU}	P11. 10	P11.9	P11.8	M
N	P1.3	P1.7	P1.6	P1.4						V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}						P11. 13	P11. 14	P11. 15	P11. 12	N
P	P1.2	P1.1	P1.0	P1.12						V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}						V_{DD}	P12.1	P12.2	P12.0	P
R	V_{DD} SBRAM	P7.1	P7.0	V_{DD}						V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}						V_{SS}	P12.3	P12.5	P12.4	R
T	P7.6	P7.5	P7.4	V_{SS}						V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}						V_{DDEBU}	P13.1	P13.3	P13.0	T
U	AN23	P7.7	P7.3	P7.2						V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}						P13.6	P13.9	P13.5	P13.2	U
V	AN22	AN21	AN19	AN16																			V_{DD}	P13. 13	P13.8	P13.4	V
W	AN20	AN17	AN13	V_{DDM}																			V_{SS}	P14.0	P13. 12	P13.7	W
Y	AN18	AN14	AN10	V_{SSM}																			V_{DDEBU}	P14.2	P13. 14	P13. 10	Y
AA	AN15	AN11	AN5	AN2																			P14.3	P14.6	P14.1	P13. 11	AA
AB	AN12	AN9	AN3	AN7																			V_{DD}	P14.5	P14.4	P13. 15	AB
AC	AN8	AN4	AN32	AN38	AN42	V_{AGND1}	AN26	AN24	V_{DDAF}	V_{SS}	V_{DD}	P4.4	P4.8	P4.12	P10.5	V_{DDP}	V_{SS}	V_{DDEBU}	V_{SS}	V_{DD}	N.C.	V_{DDEBU}	V_{SS}	P14. 12	P14.9	P14.7	AC
AD	AN6	AN1	AN34	AN40	AN35	V_{AREF1}	AN27	AN25	V_{AREF2}	P4.0	P4.2	P4.5	P4.11	P4.15	P10.2	V_{DDP}	P15.5	P16.1	P15.3	P15.2	P15.1	P16.2	N.C.	P14. 15	P14. 11	P14.8	AD
AE	AN0	AN33	AN36	AN41	V_{AREF0}	AN28	AN30	V_{FAGND}	V_{DDMF}	P4.1	P4.3	P4.7	P4.13	P10.4	P10.0	V_{DDP}	P15.4	P15.7	P16.3	P15. 11	P15.0	N.C.	N.C.	P14. 14	P14. 13	P14. 10	AE
AF	N.C.	AN37	AN39	AN43	V_{AGND0}	AN29	AN31	V_{FAREF}	V_{SSMF}	P4.6	P4.9	P4.10	P4.14	P10.3	P10.1	V_{DDP}	P16.0	P15.6	P15. 12	P15.8	P15.9	P15. 10	P15. 13	P15. 14	P15. 15	N.C.	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

mca05584_97.vsd

Figure 17 TC1797 Pinning for P/PG-BGA-416-10 / P/PG-BGA-416-27 Package

Table 4 Pin Definitions and Functions (BGA-416 Package)

Pin	Symbol	Ctrl.	Type	Function
Port 0				
A9	P0.0	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 0**
	HWCFG0	I		**Hardware Configuration Input 0**
	OUT56	O1		**OUT56 Line of GPTA0**
	OUT56	O2		**OUT56 Line of GPTA1**
	OUT80	O3		**OUT80 Line of LTCA2**
A8	P0.1	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 1**
	HWCFG1	I		**Hardware Configuration Input 1**
	OUT57	O1		**OUT57 Line of GPTA0**
	OUT57	O2		**OUT57 Line of GPTA1**
	OUT81	O3		**OUT81 Line of LTCA2**
A7	P0.2	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 2**
	HWCFG2	I		**Hardware Configuration Input 2**
	OUT58	O1		**OUT58 Line of GPTA0**
	OUT58	O2		**OUT58 Line of GPTA1**
	OUT82	O3		**OUT82 Line of LTCA2**
B8	P0.3	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 3**
	HWCFG3	I		**Hardware Configuration Input 3**
	OUT59	O1		**OUT59 Line of GPTA0**
	OUT59	O2		**OUT59 Line of GPTA1**
	OUT83	O3		**OUT83 Line of LTCA2**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
B7	P0.4	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 4**
	HWCFG4	I		**Hardware Configuration Input 4**
	OUT60	O1		**OUT60 Line of GPTA0**
	OUT60	O2		**OUT60 Line of GPTA1**
	OUT84	O3		**OUT84 Line of LTCA2**
A6	P0.5	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 5**
	HWCFG5	I		**Hardware Configuration Input 5**
	OUT61	O1		**OUT61 Line of GPTA0**
	OUT61	O2		**OUT61 Line of GPTA1**
	OUT85	O3		**OUT85 Line of LTCA2**
B6	P0.6	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 6**
	HWCFG6	I		**Hardware Configuration Input 6**
	OUT62	O1		**OUT62 Line of GPTA0**
	OUT62	O2		**OUT62 Line of GPTA1**
	OUT86	O3		**OUT86 Line of LTCA2**
C8	P0.7	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 7**
	HWCFG7	I		**Hardware Configuration Input 7**
	OUT63	O1		**OUT63 Line of GPTA0**
	OUT63	O2		**OUT63 Line of GPTA1**
	OUT87	O3		**OUT87 Line of LTCA2**
C7	P0.8	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 8**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
B5	P0.9	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 9**
	RXDA0	I		**E-Ray Channel A Receive Data Input 0**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
C6	P0.10	I/O0	A2/ PU	**Port 0 General Purpose I/O Line 10**
	TXENA	O1		**E-Ray Channel A Transmit Data Output enable**
	Reserved	O2		**-**
	Reserved	O3		**-**
D6	P0.11	I/O0	A2/ PU	**Port 0 General Purpose I/O Line 11**
	TXENB	O1		**E-Ray Channel B Transmit Data Output enable**
	Reserved	O2		**-**
	Reserved	O3		**-**
C5	P0.12	I/O0	A2/ PU	**Port 0 General Purpose I/O Line 12**
	TXDB	O1		**E-Ray Channel B Transmit Data Output**
	Reserved	O2		**-**
	Reserved	O3		**-**
D5	P0.13	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 13**
	RXDB0	I		**E-Ray Channel B Receive Data Input 0**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
A5	P0.14	I/O0	A2/ PU	**Port 0 General Purpose I/O Line 14**
	TXDA	O1		**E-Ray Channel A Transmit Data Output**
	Reserved	O2		-
	Reserved	O3		-
D4	P0.15	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 15**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
Port 1				
P3	P1.0	I/O0	A2/ PU	**Port 1 General Purpose I/O Line 0**
	REQ0	I		**External trigger Input 0**
	EXTCLK1	O1		**External Clock Output 1**
	Reserved	O2		-
	Reserved	O3		-
P2	P1.1	I/O0	A1/ PU	**Port 1 General Purpose I/O Line 1**
	REQ1	I		**External trigger Input 1**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
P1	P1.2	I/O0	A1/ PU	**Port 1 General Purpose I/O Line 2**
	REQ2	I		**External trigger Input 2**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
N1	P1.3	I/O0	A1/ PU	**Port 1 General Purpose I/O Line 3**
	REQ3	I		**External trigger Input 3**
	TREADY0B	I		**MLI0 Transmit Channel ready Input B**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
N4	P1.4	I/O0	A2/ PU	**Port 1 General Purpose I/O Line 4**
	TCLK0	O1		**MLI0 Transmit Channel Clock Output**
	Reserved	O2		-
	Reserved	O3		-
M4	P1.5	I/O0	A1/ PU	**Port 1 General Purpose I/O Line 35**
	TREADY0A	I		**MLI0 Transmit Channel ready Input A**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
N3	P1.6	I/O0	A2/ PU	**Port 1 General Purpose I/O Line 6**
	TVALID0A	O1		**MLI0 Transmit Channel valid Output A**
	SLSO10	O2		**Slave Select Output Line 10**
	Reserved	O3		-
N2	P1.7	I/O0	A2/ PU	**Port 1 General Purpose I/O Line 7**
	TData0	O1		**MLI0 Transmit Channel Data Output**
	Reserved	O2		-
	Reserved	O3		-

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
M3	P1.8	I/O0	A1/ PU	**Port 1 General Purpose I/O Line 8**
	RCLK0A	I		**MLI0 Receive Channel Clock Input A**
	OUT64	O1		**OUT64 Line of GPTA0**
	OUT64	O2		**OUT64 Line of GPTA1**
	OUT88	O3		**OUT88 Line of LTCA2**
M2	P1.9	I/O0	A2/ PU	**Port 1 General Purpose I/O Line 9**
	RREADY0A	O1		**MLI0 Receive Channel ready Output A**
	SLSO11	O2		**Slave Select Output Line 11**
	OUT65	O3		**OUT65 Line of GPTA0**
M1	P1.10	I/O0	A1/ PU	**Port 1 General Purpose I/O Line 10**
	RVALID0A	I		**MLI0 Receive Channel valid Input A**
	OUT66	O1		**OUT66 Line of GPTA0**
	OUT66	O2		**OUT66 Line of GPTA1**
	OUT90	O3		**OUT90 Line of LTCA2**
L4	P1.11	I/O0	A1/ PU	**Port 1 General Purpose I/O Line 11**
	RData0A	I		**MLI0 Receive Channel Data Input A**
	OUT67	O1		**OUT67 Line of GPTA0**
	OUT67	O2		**OUT67 Line of GPTA1**
	OUT91	O3		**OUT91 Line of LTCA2**
P4	P1.12	I/O0	A2/ PU	**Port 1 General Purpose I/O Line 12**
	EXTCLK0	O1		**External Clock Output 0**
	OUT68	O2		**OUT68 Line of GPTA0**
	OUT68	O3		**OUT68 Line of GPTA1**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
L3	P1.13	I/O0	A1/ PU	**Port 1 General Purpose I/O Line 13**
	RCLK0B	I		**MLI0 Receive Channel Clock Input B**
	OUT69	O1		**OUT69 Line of GPTA0**
	OUT69	O2		**OUT69 Line of GPTA1**
	OUT93	O3		**OUT93 Line of LTCA2**
L2	P1.14	I/O0	A1/ PU	**Port 1 General Purpose I/O Line 14**
	RVALID0B	I		**MLI0 Receive Channel valid Input B**
	OUT70	O1		**OUT70 Line of GPTA0**
	OUT70	O2		**OUT70 Line of GPTA1**
	OUT94	O3		**OUT94 Line of LTCA2**
L1	P1.15	I/O0	A1/ PU	**Port 1 General Purpose I/O Line 15**
	RData0B	I		**MLI0 Receive Channel Data Input B**
	OUT70	O1		**OUT71 Line of GPTA0**
	OUT70	O2		**OUT71 Line of GPTA1**
	OUT95	O3		**OUT95 Line of LTCA2**
Port 2				
D3	P2.2	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 2**
	SLSO02	O1		**Slave Select Output Line 2**
	SLSO12	O2		**Slave Select Output Line 12**
	SLSO02 AND SLSO12	O3		**Slave Select Output Line 2 AND Slave Select Output Line 12**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
D2	P2.3	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 3**
	SLSO03	O1		**Slave Select Output Line 3**
	SLSO13	O2		**Slave Select Output Line 13**
	SLSO03 AND SLSO13	O3		**Slave Select Output Line 3 AND Slave Select Output Line 13**
D1	P2.4	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 4**
	SLSO04	O1		**Slave Select Output Line 4**
	SLSO14	O2		**Slave Select Output Line 14**
	SLSO04 AND SLSO14	O3		**Slave Select Output Line 4 AND Slave Select Output Line 14**
C1	P2.5	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 5**
	SLSO05	O1		**Slave Select Output Line 5**
	SLSO15	O2		**Slave Select Output Line 15**
	SLSO05 AND SLSO15	O3		**Slave Select Output Line 5 AND Slave Select Output Line 15**
B1	P2.6	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 6**
	SLSO06	O1		**Slave Select Output Line 6**
	SLSO16	O2		**Slave Select Output Line 16**
	SLSO06 AND SLSO16	O3		**Slave Select Output Line 6 AND Slave Select Output Line 16**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
B2	P2.7	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 7**
	SLSO07	O1		**Slave Select Output Line 7**
	SLSO17	O2		**Slave Select Output Line 17**
	SLSO07 AND SLSO17	O3		**Slave Select Output Line 7AND Slave Select Output Line 17**
C2	P2.8	I/O0	A1/ PU	**Port 2 General Purpose I/O Line 8**
	IN0	I		**IN0 Line of GPTA0**
	IN0	I		**IN0 Line of GPTA1**
	IN0	I		**IN0 Line of LTCA2**
	OUT0	O1		**OUT0 Line of GPTA0**
	OUT0	O2		**OUT0 Line of GPTA1**
	OUT0	O3		**OUT0 Line of LTCA2**
A2	P2.9	I/O0	A1/ PU	**Port 2 General Purpose I/O Line 9**
	IN1	I		**IN1 Line of GPTA0**
	IN1	I		**IN1 Line of GPTA1**
	IN1	I		**IN1 Line of LTCA2**
	OUT1	O1		**OUT1 Line of GPTA0**
	OUT1	O2		**OUT1 Line of GPTA1**
	OUT1	O3		**OUT1 Line of LTCA2**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
B3	P2.10	I/O0	A1/ PU	**Port 2 General Purpose I/O Line 10**
	IN2	I		**IN2 Line of GPTA0**
	IN2	I		**IN2 Line of GPTA1**
	IN2	I		**IN2 Line of LTCA2**
	OUT2	O1		**OUT2 Line of GPTA0**
	OUT2	O2		**OUT2 Line of GPTA1**
	OUT2	O3		**OUT2 Line of LTCA2**
C3	P2.11	I/O0	A1/ PU	**Port 2 General Purpose I/O Line 11**
	IN3	I		**IN3 Line of GPTA0**
	IN3	I		**IN3 Line of GPTA1**
	IN3	I		**IN3 Line of LTCA2**
	OUT3	O1		**OUT3 Line of GPTA0**
	OUT3	O2		**OUT3 Line of GPTA1**
	OUT3	O3		**OUT3 Line of LTCA2**
C4	P2.12	I/O0	A1/ PU	**Port 2 General Purpose I/O Line 12**
	IN4	I		**IN4 Line of GPTA0**
	IN4	I		**IN4 Line of GPTA1**
	IN4	I		**IN4 Line of LTCA2**
	OUT4	O1		**OUT4 Line of GPTA0**
	OUT4	O2		**OUT4 Line of GPTA1**
	OUT4	O3		**OUT4 Line of LTCA2**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
A3	P2.13	I/O0	A1/ PU	**Port 2 General Purpose I/O Line 13**
	IN5	I		**IN5 Line of GPTA0**
	IN5	I		**IN5 Line of GPTA1**
	IN5	I		**IN5 Line of LTCA2**
	OUT5	O1		**OUT5 Line of GPTA0**
	OUT5	O2		**OUT5 Line of GPTA1**
	OUT5	O3		**OUT5 Line of LTCA2**
B4	P2.14	I/O0	A1/ PU	**Port 2 General Purpose I/O Line 14**
	IN6	I		**IN6 Line of GPTA0**
	IN6	I		**IN6 Line of GPTA1**
	IN6	I		**IN6 Line of LTCA2**
	OUT6	O1		**OUT6 Line of GPTA0**
	OUT6	O2		**OUT6 Line of GPTA1**
	OUT6	O3		**OUT6 Line of LTCA2**
A4	P2.15	I/O0	A1/ PU	**Port 2 General Purpose I/O Line 15**
	IN7	I		**IN7 Line of GPTA0**
	IN7	I		**IN7 Line of GPTA1**
	IN7	I		**IN7 Line of LTCA2**
	OUT7	O1		**OUT7 Line of GPTA0**
	OUT7	O2		**OUT7 Line of GPTA1**
	OUT7	O3		**OUT7 Line of LTCA2**
Port 3				

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
B12	P3.0	I/O0	A1/ PU	**Port 3 General Purpose I/O Line 0**
	IN8	I		**IN8 Line of GPTA0**
	IN8	I		**IN8 Line of GPTA1**
	IN8	I		**IN8 Line of LTCA2**
	OUT8	O1		**OUT8 Line of GPTA0**
	OUT8	O2		**OUT8 Line of GPTA1**
	OUT8	O3		**OUT8 Line of LTCA2**
A12	P3.1	I/O0	A1/ PU	**Port 3 General Purpose I/O Line 1**
	IN9	I		**IN9 Line of GPTA0**
	IN9	I		**IN9 Line of GPTA1**
	IN9	I		**IN9 Line of LTCA2**
	OUT9	O1		**OUT9 Line of GPTA0**
	OUT9	O2		**OUT9 Line of GPTA1**
	OUT9	O3		**OUT9 Line of LTCA2**
C13	P3.2	I/O0	A1/ PU	**Port 3 General Purpose I/O Line 2**
	IN10	I		**IN10 Line of GPTA0**
	IN10	I		**IN10 Line of GPTA1**
	IN10	I		**IN10 Line of LTCA2**
	OUT10	O1		**OUT10 Line of GPTA0**
	OUT10	O2		**OUT10 Line of GPTA1**
	OUT10	O3		**OUT10 Line of LTCA2**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
B11	P3.3	I/O0	A1/ PU	**Port 3 General Purpose I/O Line 3**
	IN11	I		**IN11 Line of GPTA0**
	IN11	I		**IN11 Line of GPTA1**
	IN11	I		**IN11 Line of LTCA2**
	OUT11	O1		**OUT11 Line of GPTA0**
	OUT11	O2		**OUT11 Line of GPTA1**
	OUT11	O3		**OUT11 Line of LTCA2**
C12	P3.4	I/O0	A1/ PU	**Port 3 General Purpose I/O Line 4**
	IN12	I		**IN12 Line of GPTA0**
	IN12	I		**IN12 Line of GPTA1**
	IN12	I		**IN12 Line of LTCA2**
	OUT12	O1		**OUT12 Line of GPTA0**
	OUT12	O2		**OUT12 Line of GPTA1**
	OUT12	O3		**OUT12 Line of LTCA2**
A11	P3.5	I/O0	A1/ PU	**Port 3 General Purpose I/O Line 5**
	IN13	I		**IN13 Line of GPTA0**
	IN13	I		**IN13 Line of GPTA1**
	IN13	I		**IN13 Line of LTCA2**
	OUT13	O1		**OUT13 Line of GPTA0**
	OUT13	O2		**OUT13 Line of GPTA1**
	OUT13	O3		**OUT13 Line of LTCA2**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
B10	P3.6	I/O0	A1/ PU	**Port 3 General Purpose I/O Line 6**
	IN14	I		**IN14 Line of GPTA0**
	IN14	I		**IN14 Line of GPTA1**
	IN14	I		**IN14 Line of LTCA2**
	OUT14	O1		**OUT14 Line of GPTA0**
	OUT14	O2		**OUT14 Line of GPTA1**
	OUT14	O3		**OUT14 Line of LTCA2**
C9	P3.7	I/O0	A1/ PU	**Port 3 General Purpose I/O Line 7**
	IN15	I		**IN15 Line of GPTA0**
	IN15	I		**IN15 Line of GPTA1**
	IN15	I		**IN15 Line of LTCA2**
	OUT15	O1		**OUT15 Line of GPTA0**
	OUT15	O2		**OUT15 Line of GPTA1**
	OUT15	O3		**OUT15 Line of LTCA2**
D10	P3.8	I/O0	A1/ PU	**Port 3 General Purpose I/O Line 8**
	IN16	I		**IN16 Line of GPTA0**
	IN16	I		**IN16 Line of GPTA1**
	IN16	I		**IN16 Line of LTCA2**
	OUT16	O1		**OUT16 Line of GPTA0**
	OUT16	O2		**OUT16 Line of GPTA1**
	OUT16	O3		**OUT16 Line of LTCA2**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
C11	P3.9	I/O0	A1/ PU	**Port 3 General Purpose I/O Line 9**
	IN17	I		**IN17 Line of GPTA0**
	IN17	I		**IN17 Line of GPTA1**
	IN17	I		**IN17 Line of LTCA2**
	OUT17	O1		**OUT17 Line of GPTA0**
	OUT17	O2		**OUT17 Line of GPTA1**
	OUT17	O3		**OUT17 Line of LTCA2**
C10	P3.10	I/O0	A1/ PU	**Port 3 General Purpose I/O Line 10**
	IN18	I		**IN18 Line of GPTA0**
	IN18	I		**IN18 Line of GPTA1**
	IN18	I		**IN18 Line of LTCA2**
	OUT18	O1		**OUT18 Line of GPTA0**
	OUT18	O2		**OUT18 Line of GPTA1**
	OUT18	O3		**OUT18 Line of LTCA2**
D13	P3.11	I/O0	A1/ PU	**Port 3 General Purpose I/O Line 11**
	IN19	I		**IN19 Line of GPTA0**
	IN19	I		**IN19 Line of GPTA1**
	IN19	I		**IN19 Line of LTCA2**
	OUT19	O1		**OUT19 Line of GPTA0**
	OUT19	O2		**OUT19 Line of GPTA1**
	OUT19	O3		**OUT19 Line of LTCA2**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
D11	P3.12	I/O0	A1/ PU	**Port 3 General Purpose I/O Line 12**
	IN20	I		**IN20 Line of GPTA0**
	IN20	I		**IN20 Line of GPTA1**
	IN20	I		**IN20 Line of LTCA2**
	OUT20	O1		**OUT20 Line of GPTA0**
	OUT20	O2		**OUT20 Line of GPTA1**
	OUT20	O3		**OUT20 Line of LTCA2**
D12	P3.13	I/O0	A1/ PU	**Port 3 General Purpose I/O Line 13**
	IN21	I		**IN21 Line of GPTA0**
	IN21	I		**IN21 Line of GPTA1**
	IN21	I		**IN21 Line of LTCA2**
	OUT21	O1		**OUT21 Line of GPTA0**
	OUT21	O2		**OUT21 Line of GPTA1**
	OUT21	O3		**OUT21 Line of LTCA2**
A10	P3.14	I/O0	A1/ PU	**Port 3 General Purpose I/O Line 14**
	IN22	I		**IN22 Line of GPTA0**
	IN22	I		**IN22 Line of GPTA1**
	IN22	I		**IN22 Line of LTCA2**
	OUT22	O1		**OUT22 Line of GPTA0**
	OUT22	O2		**OUT22 Line of GPTA1**
	OUT22	O3		**OUT22 Line of LTCA2**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
B9	P3.15	I/O0	A1/ PU	**Port 3 General Purpose I/O Line 15**
	IN23	I		**IN23 Line of GPTA0**
	IN23	I		**IN23 Line of GPTA1**
	IN23	I		**IN23 Line of LTCA2**
	OUT23	O1		**OUT23 Line of GPTA0**
	OUT23	O2		**OUT23 Line of GPTA1**
	OUT23	O3		**OUT23 Line of LTCA2**
Port 4				
AD10	P4.0	I/O0	A2/ PU	**Port 4 General Purpose I/O Line 0**
	IN24	I		**IN24 Line of GPTA0**
	IN24	I		**IN24 Line of GPTA1**
	IN24	I		**IN24 Line of LTCA2**
	OUT24	O1		**OUT24 Line of GPTA0**
	OUT24	O2		**OUT24 Line of GPTA1**
	OUT24	O3		**OUT24 Line of LTCA2**
AE10	P4.1	I/O0	A2/ PU	**Port 4 General Purpose I/O Line 1**
	IN25	I		**IN25 Line of GPTA0**
	IN25	I		**IN25 Line of GPTA1**
	IN25	I		**IN25 Line of LTCA2**
	OUT25	O1		**OUT25 Line of GPTA0**
	OUT25	O2		**OUT25 Line of GPTA1**
	OUT25	O3		**OUT25 Line of LTCA2**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AD11	P4.2	I/O0	A2/ PU	**Port 4 General Purpose I/O Line 2**
	IN26	I		**IN26 Line of GPTA0**
	IN26	I		**IN26 Line of GPTA1**
	IN26	I		**IN26 Line of LTCA2**
	OUT26	O1		**OUT26 Line of GPTA0**
	OUT26	O2		**OUT26 Line of GPTA1**
	OUT26	O3		**OUT26 Line of LTCA2**
AE11	P4.3	I/O0	A2/ PU	**Port 4 General Purpose I/O Line 3**
	IN27	I		**IN27 Line of GPTA0**
	IN27	I		**IN27 Line of GPTA1**
	IN27	I		**IN27 Line of LTCA2**
	OUT27	O1		**OUT27 Line of GPTA0**
	OUT27	O2		**OUT27 Line of GPTA1**
	OUT27	O3		**OUT27 Line of LTCA2**
AC12	P4.4	I/O0	A2/ PU	**Port 4 General Purpose I/O Line 4**
	IN28	I		**IN28 Line of GPTA0**
	IN28	I		**IN28 Line of GPTA1**
	IN28	I		**IN28 Line of LTCA2**
	OUT28	O1		**OUT28 Line of GPTA0**
	OUT28	O2		**OUT28 Line of GPTA1**
	OUT28	O3		**OUT28 Line of LTCA2**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AD12	P4.5	I/O0	A2/ PU	**Port 4 General Purpose I/O Line 5**
	IN29	I		**IN29 Line of GPTA0**
	IN29	I		**IN29 Line of GPTA1**
	IN29	I		**IN29 Line of LTCA2**
	OUT29	O1		**OUT29 Line of GPTA0**
	OUT29	O2		**OUT29 Line of GPTA1**
	OUT29	O3		**OUT29 Line of LTCA2**
AF10	P4.6	I/O0	A2/ PU	**Port 4 General Purpose I/O Line 6**
	IN30	I		**IN30 Line of GPTA0**
	IN30	I		**IN30 Line of GPTA1**
	IN30	I		**IN30 Line of LTCA2**
	OUT30	O1		**OUT30 Line of GPTA0**
	OUT30	O2		**OUT30 Line of GPTA1**
	OUT30	O3		**OUT30 Line of LTCA2**
AE12	P4.7	I/O0	A2/ PU	**Port 4 General Purpose I/O Line 7**
	IN31	I		**IN31 Line of GPTA0**
	IN31	I		**IN31 Line of GPTA1**
	IN31	I		**IN31Line of LTCA2**
	OUT31	O1		**OUT31 Line of GPTA0**
	OUT31	O2		**OUT31 Line of GPTA1**
	OUT31	O3		**OUT31 Line of LTCA2**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AC13	P4.8	I/O0	A1/ PU	**Port 4 General Purpose I/O Line 8**
	IN32	I		**IN32 Line of GPTA0**
	IN32	I		**IN32 Line of GPTA1**
	OUT32	O1		**OUT32 Line of GPTA0**
	OUT32	O2		**OUT32 Line of GPTA1**
	OUT0	O3		**OUT0 Line of LTCA2**
AF11	P4.9	I/O0	A1/ PU	**Port 4 General Purpose I/O Line 9**
	IN33	I		**IN33 Line of GPTA0**
	IN33	I		**IN33 Line of GPTA1**
	OUT33	O1		**OUT33 Line of GPTA0**
	OUT33	O2		**OUT33 Line of GPTA1**
	OUT1	O3		**OUT1 Line of LTCA2**
AF12	P4.10	I/O0	A1/ PU	**Port 4 General Purpose I/O Line 10**
	IN34	I		**IN34 Line of GPTA0**
	IN34	I		**IN34 Line of GPTA1**
	OUT34	O1		**OUT34 Line of GPTA0**
	OUT34	O2		**OUT34 Line of GPTA1**
	OUT2	O3		**OUT2 Line of LTCA2**
AD13	P4.11	I/O0	A1/ PU	**Port 4 General Purpose I/O Line 11**
	IN35	I		**IN35 Line of GPTA0**
	IN35	I		**IN35 Line of GPTA1**
	OUT35	O1		**OUT35 Line of GPTA0**
	OUT35	O2		**OUT35 Line of GPTA1**
	OUT3	O3		**OUT3 Line of LTCA2**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AC14	P4.12	I/O0	A1/ PU	**Port 4 General Purpose I/O Line 12**
	IN36	I		**IN36 Line of GPTA0**
	IN36	I		**IN36 Line of GPTA1**
	OUT36	O1		**OUT36 Line of GPTA0**
	OUT36	O2		**OUT36 Line of GPTA1**
	OUT4	O3		**OUT4 Line of LTCA2**
AE13	P4.13	I/O0	A1/ PU	**Port 4 General Purpose I/O Line 13**
	IN37	I		**IN37 Line of GPTA0**
	IN37	I		**IN37 Line of GPTA1**
	OUT37	O1		**OUT37 Line of GPTA0**
	OUT37	O2		**OUT37 Line of GPTA1**
	OUT5	O3		**OUT5 Line of LTCA2**
AF13	P4.14	I/O0	A1/ PU	**Port 4 General Purpose I/O Line 14**
	IN38	I		**IN38 Line of GPTA0**
	IN38	I		**IN38 Line of GPTA1**
	OUT38	O1		**OUT38 Line of GPTA0**
	OUT38	O2		**OUT38 Line of GPTA1**
	OUT6	O3		**OUT6 Line of LTCA2**
AD14	P4.15	I/O0	A1/ PU	**Port 4 General Purpose I/O Line 15**
	IN39	I		**IN39 Line of GPTA0**
	IN39	I		**IN39 Line of GPTA1**
	OUT39	O1		**OUT39 Line of GPTA0**
	OUT39	O2		**OUT39 Line of GPTA1**
	OUT7	O3		**OUT7 Line of LTCA2**
Port 5				

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
B13	P5.0	I/O0	A2/ PU	**Port 5 General Purpose I/O Line 0**
	RXD0A	I		**ASC0 Receiver Input/Output A**
	RXD0A	O1		**ASC0 Receiver Input/Output A**
	OUT72	O2		**OUT72 Line of GPTA0**
	OUT72	O3		**OUT72 Line of GPTA1**
A13	P5.1	I/O0	A2/ PU	**Port 5 General Purpose I/O Line 1**
	TXD0	O1		**ASC0 Transmitter Output A**
	OUT73	O2		**OUT73 Line of GPTA0**
	OUT73	O3		**OUT73 Line of GPTA1**
A14	P5.2	I/O0	A2/ PU	**Port 5 General Purpose I/O Line 2**
	RXD1A	I		**ASC1 Receiver Input/Output A**
	RXD1A	O1		**ASC1 Receiver Input/Output A**
	OUT74	O2		**OUT74 Line of GPTA0**
	OUT74	O3		**OUT74 Line of GPTA1**
B14	P5.3	I/O0	A2/ PU	**Port 5 General Purpose I/O Line 3**
	TXD1	O1		**ASC1 Transmitter Output A**
	OUT75	O2		**OUT75 Line of GPTA0**
	OUT75	O3		**OUT75 Line of GPTA1**
C15	P5.4	I/O0	A2/ PU	**Port 5 General Purpose I/O Line 4**
	EN00	O1		**MSC0 Device Select Output 0**
	RREADY0B	O2		**MLI0 Receive Channel ready Output B**
	OUT76	O3		**OUT76 Line of GPTA0**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
C14	P5.5	I/O0	A2/ PU	**Port 5 General Purpose I/O Line 5**
	SDI0	I		**MSC0 serial Data Input**
	OUT77	O1		**OUT77 Line of GPTA0**
	OUT77	O2		**OUT77 Line of GPTA1**
	OUT101	O3		**OUT101 Line of LTCA2**
B15	P5.6	I/O0	A2/ PU	**Port 5 General Purpose I/O Line 6**
	EN10	O1		**MSC1 Device Select Output 0**
	TVALID0B	O2		**MLI0 Transmit Channel valid Output B**
	OUT78	O3		**OUT78 Line of GPTA0**
A15	P5.7	I/O0	A2/ PU	**Port 5 General Purpose I/O Line 7**
	SDI1	I		**MSC1 serial Data Input**
	OUT79	O1		**OUT79 Line of GPTA0**
	OUT79	O2		**OUT79 Line of GPTA1**
	OUT103	O3		**OUT103 Line of LTCA2**
D17	P5.8	I/O0	F/ PU	**Port 5 General Purpose I/O Line 8**
	SON0	O1		**MSC0 Differential Driver serial Data Output Negative**
	OUT80	O2		**OUT80 Line of GPTA0**
	OUT80	O3		**OUT 80 Line of GPTA1**
C16	P5.9	I/O0	F/ PU	**Port 5 General Purpose I/O Line 9**
	SOP0A	O1		**MSC0 Differential Driver serial Data Output Positive A**
	OUT81	O2		**OUT81 Line of GPTA0**
	OUT81	O3		**OUT81 Line of GPTA1**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
C17	P5.10	I/O0	F/ PU	**Port 5 General Purpose I/O Line 10**
	FCLN0	O1		**MSC0 Differential Driver Clock Output Negative**
	OUT82	O2		**OUT82 Line of GPTA0**
	OUT82	O3		**OUT82 Line of GPTA1**
C18	P5.11	I/O0	F/ PU	**Port 5 General Purpose I/O Line 11**
	FCLP0A	O1		**MSC0 Differential Driver Clock Output Positive A**
	OUT83	O2		**OUT83 Line of GPTA0**
	OUT83	O3		**OUT83 Line of GPTA1**
A16	P5.12	I/O0	F/ PU	**Port 5 General Purpose I/O Line 12**
	SON1	O1		**MSC1 Differential Driver serial Data OutputNegative**
	OUT84	O2		**OUT84 Line of GPTA0**
	OUT84	O3		**OUT84 Line of GPTA1**
B16	P5.13	I/O0	F/ PU	**Port 5 General Purpose I/O Line 13**
	SOP1A	O1		**MSC1 Differential Driver serial Data Output Positive A**
	OUT85	O2		**OUT85 Line of GPTA0**
	OUT85	O3		**OUT85 Line of GPTA1**
B17	P5.14	I/O0	F/ PU	**Port 5 General Purpose I/O Line 14**
	FCLN1	O1		**MSC1 Differential Driver Clock Output Negative**
	OUT86	O2		**OUT86 Line of GPTA0**
	OUT86	O3		**OUT86 Line of GPTA1**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
A17	P5.15	I/O0	F/ PU	**Port 5 General Purpose I/O Line 15**
	FCLNP1A	O1		**MSC1 Differential Driver Clock Output Positive A**
	OUT87	O2		**OUT87 Line of GPTA0**
	OUT87	O3		**OUT87 Line of GPTA1**
Port 6				
F3	P6.4	I/O0	A2/ PU	**Port 6 General Purpose I/O Line 4**
	MTSR1	I		**SSC1 Slave Receive Input (Slave Mode)**
	MTSR1	O1		**SSC1 Master Transmit Output (Master Mode)**
	Reserved	O2		**-**
	Reserved	O3		**-**
G4	P6.5	I/O0	A2/ PU	**Port 6 General Purpose I/O Line 5**
	MRST1	I		**SSC1 Master Receive Input (Master Mode)**
	MRST1	O1		**SSC1 Slave Transmit Output (Slave Mode)**
	Reserved	O2		**-**
	Reserved	O3		**-**
E3	P6.6	I/O0	A2/ PU	**Port 6 General Purpose I/O Line 6**
	SCLK1	I		**SSC1 Clock Input/Output**
	SCLK1	O1		**SSC1 Clock Input/Output**
	Reserved	O2		**-**
	Reserved	O3		**-**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
G3	P6.7	I/O0	A2/ PU	**Port 6 General Purpose I/O Line 7**
	SLSI11	I		**SSC1 Slave Select Input**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
F4	P6.8	I/O0	A2/ PU	**Port 6 General Purpose I/O Line 8**
	RXDCAN0	I		**CAN Node 0 Receiver Input 0** **CAN Node 3 Receiver Input 1**
	RXD0B	I		**ASC0 Receiver Input/Output B**
	Reserved	O1		**-**
	RXD0B	O2		**ASC0 Receiver Input/Output B**
	Reserved	O3		**-**
E4	P6.9	I/O0	A2/ PU	**Port 6 General Purpose I/O Line 9**
	TXDCAN0	O1		**CAN Node 0 Transmitter Output**
	TXD0	O2		**ASC0 Transmitter Output B**
	Reserved	O3		**-**
F2	P6.10	I/O0	A2/ PU	**Port 6 General Purpose I/O Line 10**
	RXDCAN1	I		**CAN Node 1 Receiver Input 0** **CAN Node 0 Receiver Input 1**
	RXD1B	I		**ASC1 Receiver Input/Output B**
	Reserved	O1		**-**
	RXD1B	O2		**ASC1 Receiver Input/Output B**
	TXENA	O3		**E-Ray Channel A Transmit Data Output enable**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
E2	P6.11	I/O0	A2/ PU	**Port 6 General Purpose I/O Line 11**
	TXDCAN1	O1		**CAN Node 1 Transmitter Output**
	TXD1	O2		**ASC1 Transmitter Output B**
	TXENB	O3		**E-Ray Channel B Transmit Data Output enable**
E1	P6.12	I/O0	A1/ PU	**Port 6 General Purpose I/O Line 12**
	RXDCAN2	I		**CAN Node 2 Receiver Input 0** **CAN Node 1 Receiver Input 1**
	RXDA1	I		**E-Ray Channel A Receive Data Input 1**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
G2	P6.13	I/O0	A2/ PU	**Port 6 General Purpose I/O Line 13**
	TXDCAN2	O1		**CAN Node 2 Transmitter Output**
	TXDA	O2		**E-Ray Channel A Transmit Data Output**
	Reserved	O3		**-**
F1	P6.14	I/O0	A1/ PU	**Port 6 General Purpose I/O Line 14**
	RXDCAN3	I		**CAN Node 3 Receiver Input 0** **CAN Node 2 Receiver Input 1**
	RXDB1	I		**E-Ray Channel B Receive Data Input 1**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
G1	P6.15	I/O0	A2/ PU	**Port 6 General Purpose I/O Line 15**
	TXDCAN3	O1		**CAN Node 3 Transmitter Output**
	TXDB	O2		**E-Ray Channel B Transmit Data Output**
	Reserved	O3		**-**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
Port 7				
R3	P7.0	I/O0	A1/ PU	**Port 7 General Purpose I/O Line 0**
	REQ4	I		**External trigger Input 4**
	AD2EMUX2	O1		**ADC2 external multiplexer Control Output 2**
	Reserved	O2		**-**
	Reserved	O3		**-**
R2	P7.1	I/O0	A1/ PU	**Port 7 General Purpose I/O Line 1**
	REQ5	I		**External trigger Input 5**
	AD0EMUX2	O1		**ADC0 external multiplexer Control Output 2**
	Reserved	O2		**-**
	Reserved	O3		**-**
U4	P7.2	I/O0	A1/ PU	**Port 7 General Purpose I/O Line 2**
	AD0EMUX0	O1		**ADC0 external multiplexer Control Output 0**
	Reserved	O2		**-**
	Reserved	O3		**-**
U3	P7.3	I/O0	A1/ PU	**Port 7 General Purpose I/O Line 3**
	AD0EMUX1	O1		**ADC0 external multiplexer Control Output 1**
	Reserved	O2		**-**
	Reserved	O3		**-**
T3	P7.4	I/O0	A1/ PU	**Port 7 General Purpose I/O Line 4**
	REQ6	I		**External trigger Input 6**
	AD2EMUX0	O1		**ADC2 external multiplexer Control Output 0**
	Reserved	O2		**-**
	Reserved	O3		**-**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
T2	P7.5	I/O0	A1/ PU	**Port 7 General Purpose I/O Line 5**
	REQ7	I		**External trigger Input 7**
	AD2EMUX1	O1		**ADC2 external multiplexer Control Output 1**
	Reserved	O2		**-**
	Reserved	O3		**-**
T1	P7.6	I/O0	A1/ PU	**Port 7 General Purpose I/O Line 6**
	AD1EMUX0	O1		**ADC1 external multiplexer Control Output 0**
	Reserved	O2		**-**
	Reserved	O3		**-**
U2	P7.7	I/O0	A1/ PU	**Port 7 General Purpose I/O Line 7**
	AD1EMUX1	O1		**ADC1 external multiplexer Control Output 1**
	Reserved	O2		**-**
	Reserved	O3		**-**
Port 8				
H2	P8.0	I/O0	A2/ PU	**Port 8 General Purpose I/O Line 0**
	IN40	I		**I/O Line of GPTA0**
	IN40	I		**I/O Line of GPTA1**
	OUT40	O1		**I/O Line of GPTA0**
	OUT40	O2		**I/O Line of GPTA1**
	TCLK1	O3		**MLI1 Transmit Channel Clock Output**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
H1	P8.1	I/O0	A1/ PU	**Port 8 General Purpose I/O Line 1**
	IN41	I		**I/O Line of GPTA0**
	IN41	I		**I/O Line of GPTA1**
	TREADY1A	I		**MLI1 Transmit Channel ready Input A**
	OUT41	O1		**I/O Line of GPTA0**
	OUT41	O2		**I/O Line of GPTA1**
	Reserved	O3		**-**
J3	P8.2	I/O0	A2/ PU	**Port 8 General Purpose I/O Line 2**
	IN42	I		**I/O Line of GPTA0**
	IN42	I		**I/O Line of GPTA1**
	OUT42	O1		**I/O Line of GPTA0**
	OUT42	O2		**I/O Line of GPTA1**
	TVALID1A	O3		**MLI1 Transmit Channel valid Output A**
J2	P8.3	I/O0	A2/ PU	**Port 8 General Purpose I/O Line 3**
	IN43	I		**I/O Line of GPTA0**
	IN43	I		**I/O Line of GPTA1**
	OUT43	O1		**I/O Line of GPTA0**
	OUT43	O2		**I/O Line of GPTA1**
	TData1	O3		**MLI1 Transmit Channel Data Output A**
J1	P8.4	I/O0	A1/ PU	**Port 8 General Purpose I/O Line 4**
	IN44	I		**I/O Line of GPTA0**
	IN44	I		**I/O Line of GPTA1**
	RCLK1A	I		**MLI1 Receive Channel Clock Input A**
	OUT44	O1		**I/O Line of GPTA0**
	OUT44	O2		**I/O Line of GPTA1**
	Reserved	O3		**-**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
K2	P8.5	I/O0	A2/ PU	**Port 8 General Purpose I/O Line 5**
	IN45	I		**I/O Line of GPTA0**
	IN45	I		**I/O Line of GPTA1**
	OUT45	O1		**I/O Line of GPTA0**
	OUT45	O2		**I/O Line of GPTA1**
	RREADY1A	O3		**MLI1 Receive Channel ready Output A**
K3	P8.6	I/O0	A1/ PU	**Port 8 General Purpose I/O Line 6**
	IN46	I		**I/O Line of GPTA0**
	IN46	I		**I/O Line of GPTA1**
	RVALID1A	I		**MLI1 Receive Channel valid Input A**
	OUT46	O1		**I/O Line of GPTA0**
	OUT46	O2		**I/O Line of GPTA1**
	Reserved	O3		**-**
K1	P8.7	I/O0	A1/ PU	**Port 8 General Purpose I/O Line 7**
	IN47	I		**I/O Line of GPTA0**
	IN47	I		**I/O Line of GPTA1**
	RData1A	I		**MLI1 Receive Channel Data Input A**
	OUT47	O1		**I/O Line of GPTA0**
	OUT47	O2		**I/O Line of GPTA1**
	Reserved	O3		**-**
Port 9				

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
A19	P9.0	I/O0	A2/ PU	**Port 9 General Purpose I/O Line 0**
	IN48	I		**I/O Line of GPTA0**
	IN48	I		**I/O Line of GPTA1**
	OUT48	O1		**I/O Line of GPTA0**
	OUT48	O2		**I/O Line of GPTA1**
	EN12	O3		**MSC1 Device Select Output 2**
B19	P9.1	I/O0	A2/ PU	**Port 9 General Purpose I/O Line 1**
	IN49	I		**I/O Line of GPTA0**
	IN49	I		**I/O Line of GPTA1**
	OUT49	O1		**I/O Line of GPTA0**
	OUT49	O2		**I/O Line of GPTA1**
	EN11	O3		**MSC1 Device Select Output 1**
B20	P9.2	I/O0	A2/ PU	**Port 9 General Purpose I/O Line 2**
	IN50	I		**I/O Line of GPTA0**
	IN50	I		**I/O Line of GPTA1**
	OUT50	O1		**I/O Line of GPTA0**
	OUT50	O2		**I/O Line of GPTA1**
	SOP1B	O3		**MSC1 serial Data Output**
A20	P9.3	I/O0	A2/ PU	**Port 9 General Purpose I/O Line 3**
	IN51	I		**I/O Line of GPTA0**
	IN51	I		**I/O Line of GPTA1**
	OUT51	O1		**I/O Line of GPTA0**
	OUT51	O2		**I/O Line of GPTA1**
	FCLP1B	O3		**MSC1 Clock Output**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
D18	P9.4	I/O0	A2/ PU	**Port 9 General Purpose I/O Line 4**
	IN52	I		**I/O Line of GPTA0**
	IN52	I		**I/O Line of GPTA1**
	OUT52	O1		**I/O Line of GPTA0**
	OUT52	O2		**I/O Line of GPTA1**
	EN03	O3		**MSC0 Device Select Output 3**
'D19	P9.5	I/O0	A2/ PU	**Port 9 General Purpose I/O Line 5**
	IN53	I		**I/O Line of GPTA0**
	IN53	I		**I/O Line of GPTA1**
	OUT53	O1		**I/O Line of GPTA0**
	OUT53	O2		**I/O Line of GPTA1**
	EN02	O3		**MSC0 Device Select Output 2**
C19	P9.6	I/O0	A2/ PU	**Port 9 General Purpose I/O Line 6**
	IN54	I		**I/O Line of GPTA0**
	IN54	I		**I/O Line of GPTA1**
	OUT54	O1		**I/O Line of GPTA0**
	OUT54	O2		**I/O Line of GPTA1**
	EN01	O3		**MSC0 Device Select Output 1**
D20	P9.7	I/O0	A2/ PU	**Port 9 General Purpose I/O Line 7**
	IN55	I		**I/O Line of GPTA0**
	IN55	I		**I/O Line of GPTA1**
	OUT55	O1		**I/O Line of GPTA0**
	OUT55	O2		**I/O Line of GPTA1**
	SOP0B	O3		**MSC0 serial Data Output**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
C20	P9.8	I/O0	A2/ PU	**Port 9 General Purpose I/O Line 8**
	FCLP0B	O1		**MSC0 Clock Output**
	FCLP0B	O2		**MSC0 Clock Output**
	FCLP0B	O3		**MSC0 Clock Output**
A21	P9.9	I/O0	A1/ PU	**Port 9 General Purpose I/O Line 9**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
B21	P9.10	I/O0	A1/ PU	**Port 9 General Purpose I/O Line 10**
	EMGSTOP	I		**Emergency Stop**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
C21	P9.11	I/O0	A1/ PU	**Port 9 General Purpose I/O Line 11**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
D21	P9.12	I/O0	A1/ PU	**Port 9 General Purpose I/O Line 12**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
C26	P9.13	I/O0	A2/ PU	**Port 9 General Purpose I/O Line 13**
	$\overline{\text{BRKIN}}$	I		**OCDS Break Input**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
	$\overline{\text{BRKOUT}}$	O		**OCDS Break Output**
D26	P9.14	I/O0	A2/ PU	**Port 9 General Purpose I/O Line 14**
	$\overline{\text{BRKIN}}$	I		**OCDS Break Input**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
	$\overline{\text{BRKOUT}}$	O		**OCDS Break Output**
Port 10				
AE15	P10.0	I/O0	A2/ PU	**Port 10 General Purpose I/O Line 0**
	MRST0	I		**SSC0 Master Receive Input (Master Mode)**
	MRST0	O1		**SSC0 Slave Transmit Output (Slave Mode)**
	Reserved	O2		**-**
	Reserved	O3		**-**
AF15	P10.1	I/O0	A2/ PU	**Port 10 General Purpose I/O Line 1**
	MTSR0	I		**SSC0 Slave Receive Input (Slave Mode)**
	MTSR0	O1		**SSC0 Master Transmit Output (Master Mode)**
	Reserved	O2		**-**
	Reserved	O3		**-**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AD15	P10.2	I/O0	A1/ PU	**Port 10 General Purpose I/O Line 2**
	SLSI01	I		**SSC0 Slave Select Input**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
AF14	P10.3	I/O0	A2/ PU	**Port 10 General Purpose I/O Line 3**
	SCLK0	I		**SSC0 Clock Input/Output**
	SCLK0	O1		**SSC0 Clock Input/Output**
	Reserved	O2		-
	Reserved	O3		-
AE14	P10.4	I/O0	A2/ PU	**Port 10 General Purpose I/O Line 4**
	SLSO00	O1		**SSC0 Slave Select Output Line 0**
	Reserved	O2		-
	Reserved	O3		-
AC15	P10.5	I/O0	A2/ PU	**Port 10 General Purpose I/O Line 5**
	SLSO01	O1		**SSC0 Slave Select Output Line 1**
	Reserved	O2		-
	Reserved	O3		-
Port 11				
J26	P11.0	I/O0	B1/ PU	**Port 11 General Purpose I/O Line 0**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A0	O		**EBU Address Bus Line 0**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
K25	P11.1	I/O0	B1/ PU	**Port 11 General Purpose I/O Line 1**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A1	O		**EBU Address Bus Line 1**
K26	P11.2	I/O0	B1/ PU	**Port 11 General Purpose I/O Line 2**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A2	O		**EBU Address Bus Line 2**
J23	P11.3	I/O0	B1/ PU	**Port 11 General Purpose I/O Line 3**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A3	O		**EBU Address Bus Line 3**
K24	P11.4	I/O0	B1/ PU	**Port 11 General Purpose I/O Line 4**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A4	O		**EBU Address Bus Line 4**
L25	P11.5	I/O0	B1/ PU	**Port 11 General Purpose I/O Line 5**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A5	O		**EBU Address Bus Line 5**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
L26	P11.6	I/O0	B1/ PU	**Port 11 General Purpose I/O Line 6**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A6	O		**EBU Address Bus Line 6**
K23	P11.7	I/O0	B1/ PU	**Port 11 General Purpose I/O Line 7**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A7	O		**EBU Address Bus Line 7**
M26	P11.8	I/O0	B1/ PU	**Port 11 General Purpose I/O Line 8**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A8	O		**EBU Address Bus Line 8**
M25	P11.9	I/O0	B1/ PU	**Port 11 General Purpose I/O Line 9**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A9	O		**EBU Address Bus Line 9**
M24	P11.10	I/O0	B1/ PU	**Port 11 General Purpose I/O Line 10**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A10	O		**EBU Address Bus Line 10**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
L24	P11.11	I/O0	B1/ PU	**Port 11 General Purpose I/O Line 11**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A11	O		**EBU Address Bus Line 11**
N26	P11.12	I/O0	B1/ PU	**Port 11 General Purpose I/O Line 12**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A12	O		**EBU Address Bus Line 12**
N23	P11.13	I/O0	B1/ PU	**Port 11 General Purpose I/O Line 13**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A13	O		**EBU Address Bus Line 13**
N24	P11.14	I/O0	B1/ PU	**Port 11 General Purpose I/O Line 14**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A14	O		**EBU Address Bus Line 14**
N25	P11.15	I/O0	B1/ PU	**Port 11 General Purpose I/O Line 15**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A15	O		**EBU Address Bus Line 15**
Port 12				

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
P26	P12.0	I/O0	B1/ PU	**Port 12 General Purpose I/O Line 0**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A16	O		**EBU Address Bus Line 16**
P24	P12.1	I/O0	B1/ PU	**Port 12 General Purpose I/O Line 1**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A17	O		**EBU Address Bus Line 17**
P25	P12.2	I/O0	B1/ PU	**Port 12 General Purpose I/O Line 2**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A18	O		**EBU Address Bus Line 18**
R24	P12.3	I/O0	B1/ PU	**Port 12 General Purpose I/O Line 3**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A19	O		**EBU Address Bus Line 19**
R26	P12.4	I/O0	B1/ PU	**Port 12 General Purpose I/O Line 4**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A20	O		**EBU Address Bus Line 20**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
R25	P12.5	I/O0	B1/ PU	**Port 12 General Purpose I/O Line 5**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
	A21	O		**EBU Address Bus Line 21**
J24	P12.6	I/O0	B1/ PU	**Port 12 General Purpose I/O Line 6**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
	A22	O		**EBU Address Bus Line 22**
J25	P12.7	I/O0	B1/ PU	**Port 12 General Purpose I/O Line 7**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
	A23	O		**EBU Address Bus Line 23**
Port 13				
T26	P13.0	I/O0	B1/ PU	**Port 13 General Purpose I/O Line 0**
	AD0	I		**EBU Address/Data Bus Line 0**
	OUT88	O1		**OUT88 Line of GPTA0**
	OUT88	O2		**OUT88 Line of GPTA1**
	OUT80	O3		**OUT80 Line of LTCA2**
	AD0	O		**EBU Address/Data Bus Line 0**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
T24	P13.1	I/O0	B1/ PU	**Port 13 General Purpose I/O Line 1**
	AD1	I		**EBU Address/Data Bus Line 1**
	OUT89	O1		**OUT89 Line of GPTA0**
	OUT89	O2		**OUT89 Line of GPTA1**
	OUT81	O3		**OUT81 Line of LTCA2**
	AD1	O		**EBU Address/Data Bus Line 1**
U26	P13.2	I/O0	B1/ PU	**Port 13 General Purpose I/O Line 2**
	AD2	I		**EBU Address/Data Bus Line 2**
	OUT90	O1		**OUT90 Line of GPTA0**
	OUT90	O2		**OUT90 Line of GPTA1**
	OUT82	O3		**OUT82 Line of LTCA2**
	AD2	O		**EBU Address/Data Bus Line 2**
T25	P13.3	I/O0	B1/ PU	**Port 13 General Purpose I/O Line 3**
	AD3	I		**EBU Address/Data Bus Line 3**
	OUT91	O1		**OUT91 Line of GPTA0**
	OUT91	O2		**OUT91 Line of GPTA1**
	OUT83	O3		**OUT83 Line of LTCA2**
	AD3	O		**EBU Address/Data Bus Line 3**
V26	P13.4	I/O0	B1/ PU	**Port 13 General Purpose I/O Line 4**
	AD4	I		**EBU Address/Data Bus Line 4**
	OUT92	O1		**OUT92 Line of GPTA0**
	OUT92	O2		**OUT92 Line of GPTA1**
	OUT84	O3		**OUT84 Line of LTCA2**
	AD4	O		**EBU Address/Data Bus Line 4**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
U25	P13.5	I/O0	B1/ PU	**Port 13 General Purpose I/O Line 5**
	AD5	I		**EBU Address/Data Bus Line 5**
	OUT93	O1		**OUT93 Line of GPTA0**
	OUT93	O2		**OUT93 Line of GPTA1**
	OUT85	O3		**OUT85 Line of LTCA2**
	AD5	O		**EBU Address/Data Bus Line 5**
U23	P13.6	I/O0	B1/ PU	**Port 13 General Purpose I/O Line 6**
	AD6	I		**EBU Address/Data Bus Line 6**
	OUT94	O1		**OUT94 Line of GPTA0**
	OUT94	O2		**OUT94 Line of GPTA1**
	OUT86	O3		**OUT86 Line of LTCA2**
	AD6	O		**EBU Address/Data Bus Line 6**
W26	P13.7	I/O0	B1/ PU	**Port 13 General Purpose I/O Line 7**
	AD7	I		**EBU Address/Data Bus Line 7**
	OUT95	O1		**OUT95 Line of GPTA0**
	OUT95	O2		**OUT95 Line of GPTA1**
	OUT87	O3		**OUT87 Line of LTCA2**
	AD7	O		**EBU Address/Data Bus Line 7**
V25	P13.8	I/O0	B1/ PU	**Port 13 General Purpose I/O Line 8**
	AD8	I		**EBU Address/Data Bus Line 8**
	OUT96	O1		**OUT96 Line of GPTA0**
	OUT96	O2		**OUT96 Line of GPTA1**
	OUT88	O3		**OUT88 Line of LTCA2**
	AD8	O		**EBU Address/Data Bus Line 8**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
U24	P13.9	I/O0	B1/ PU	**Port 13 General Purpose I/O Line 9**
	AD9	I		**EBU Address/Data Bus Line 9**
	OUT97	O1		**OUT97 Line of GPTA0**
	OUT97	O2		**OUT97 Line of GPTA1**
	OUT89	O3		**OUT89 Line of LTCA2**
	AD9	O		**EBU Address/Data Bus Line 9**
Y26	P13.10	I/O0	B1/ PU	**Port 13 General Purpose I/O Line 10**
	AD10	I		**EBU Address/Data Bus Line 10**
	OUT98	O1		**OUT98 Line of GPTA0**
	OUT98	O2		**OUT98 Line of GPTA1**
	OUT90	O3		**OUT90 Line of LTCA2**
	AD10	O		**EBU Address/Data Bus Line 10**
AA26	P13.11	I/O0	B1/ PU	**Port 13 General Purpose I/O Line 11**
	AD11	I		**EBU Address/Data Bus Line 11**
	OUT99	O1		**OUT99 Line of GPTA0**
	OUT99	O2		**OUT99 Line of GPTA1**
	OUT91	O3		**OUT91 Line of LTCA2**
	AD11	O		**EBU Address/Data Bus Line 11**
W25	P13.12	I/O0	B1/ PU	**Port 13 General Purpose I/O Line 12**
	AD12	I		**EBU Address/Data Bus Line 12**
	OUT100	O1		**OUT100 Line of GPTA0**
	OUT100	O2		**OUT100 Line of GPTA1**
	OUT92	O3		**OUT92 Line of LTCA2**
	AD12	O		**EBU Address/Data Bus Line 12**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
V24	P13.13	I/O0	B1/ PU	**Port 13 General Purpose I/O Line 13**
	AD13	I		**EBU Address/Data Bus Line 13**
	OUT101	O1		**OUT101 Line of GPTA0**
	OUT101	O2		**OUT101 Line of GPTA1**
	OUT93	O3		**OUT93 Line of LTCA2**
	AD13	O		**EBU Address/Data Bus Line 13**
Y25	P13.14	I/O0	B1/ PU	**Port 13 General Purpose I/O Line 14**
	AD14	I		**EBU Address/Data Bus Line 14**
	OUT102	O1		**OUT102 Line of GPTA0**
	OUT102	O2		**OUT102 Line of GPTA1**
	OUT94	O3		**OUT94 Line of LTCA2**
	AD14	O		**EBU Address/Data Bus Line 14**
AB26	P13.15	I/O0	B1/ PU	**Port 13 General Purpose I/O Line 15**
	AD15	I		**EBU Address/Data Bus Line 15**
	OUT103	O1		**OUT103 Line of GPTA0**
	OUT103	O2		**OUT103 Line of GPTA1**
	OUT95	O3		**OUT95 Line of LTCA2**
	AD15	O		**EBU Address/Data Bus Line 15**
Port 14				
W24	P14.0	I/O0	B1/ PU	**Port 14 General Purpose I/O Line 0**
	AD16	I		**EBU Address/Data Bus Line 16**
	OUT96	O1		**OUT96 Line of GPTA0**
	OUT96	O2		**OUT96 Line of GPTA1**
	OUT96	O3		**OUT96 Line of LTCA2**
	AD16	O		**EBU Address/Data Bus Line 16**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AA25	P14.1	I/O0	B1/ PU	**Port 14 General Purpose I/O Line 1**
	AD17	I		**EBU Address/Data Bus Line 17**
	OUT97	O1		**OUT97 Line of GPTA0**
	OUT97	O2		**OUT97 Line of GPTA1**
	OUT97	O3		**OUT97 Line of LTCA2**
	AD17	O		**EBU Address/Data Bus Line 17**
Y24	P14.2	I/O0	B1/ PU	**Port 14 General Purpose I/O Line 2**
	AD18	I		**EBU Address/Data Bus Line 18**
	OUT98	O1		**OUT98 Line of GPTA0**
	OUT98	O2		**OUT98 Line of GPTA1**
	OUT98	O3		**OUT98 Line of LTCA2**
	AD18	O		**EBU Address/Data Bus Line 18**
AA23	P14.3	I/O0	B1/ PU	**Port 14 General Purpose I/O Line 3**
	AD19	I		**EBU Address/Data Bus Line 19**
	OUT99	O1		**OUT99 Line of GPTA0**
	OUT99	O2		**OUT99 Line of GPTA1**
	OUT99	O3		**OUT99 Line of LTCA2**
	AD19	O		**EBU Address/Data Bus Line 19**
AB25	P14.4	I/O0	B1/ PU	**Port 14 General Purpose I/O Line 4**
	AD20	I		**EBU Address/Data Bus Line 20**
	OUT100	O1		**OUT100 Line of GPTA0**
	OUT100	O2		**OUT100 Line of GPTA1**
	OUT100	O3		**OUT100 Line of LTCA2**
	AD20	O		**EBU Address/Data Bus Line 20**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AB24	P14.5	I/O0	B1/ PU	**Port 14 General Purpose I/O Line 5**
	AD21	I		**EBU Address/Data Bus Line 21**
	OUT101	O1		**OUT101 Line of GPTA0**
	OUT101	O2		**OUT101 Line of GPTA1**
	OUT101	O3		**OUT101 Line of LTCA2**
	AD21	O		**EBU Address/Data Bus Line 21**
AA24	P14.6	I/O0	B1/ PU	**Port 14 General Purpose I/O Line 6**
	AD22	I		**EBU Address/Data Bus Line 22**
	OUT102	O1		**OUT102 Line of GPTA0**
	OUT102	O2		**OUT102 Line of GPTA1**
	OUT102	O3		**OUT102 Line of LTCA2**
	AD22	O		**EBU Address/Data Bus Line 22**
AC26	P14.7	I/O0	B1/ PU	**Port 14 General Purpose I/O Line 7**
	AD23	I		**EBU Address/Data Bus Line 23**
	OUT103	O1		**OUT103 Line of GPTA0**
	OUT103	O2		**OUT103 Line of GPTA1**
	OUT103	O3		**OUT103 Line of LTCA2**
	AD23	O		**EBU Address/Data Bus Line 23**
AD26	P14.8	I/O0	B1/ PU	**Port 14 General Purpose I/O Line 8**
	AD24	I		**EBU Address/Data Bus Line 24**
	OUT104	O1		**OUT104 Line of GPTA0**
	OUT104	O2		**OUT104 Line of GPTA1**
	OUT104	O3		**OUT104 Line of LTCA2**
	AD24	O		**EBU Address/Data Bus Line 24**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AC25	P14.9	I/O0	B1/ PU	**Port 14 General Purpose I/O Line 9**
	AD25	I		**EBU Address/Data Bus Line 25**
	OUT105	O1		**OUT105 Line of GPTA0**
	OUT105	O2		**OUT105 Line of GPTA1**
	OUT105	O3		**OUT105 Line of LTCA2**
	AD25	O		**EBU Address/Data Bus Line 25**
AE26	P14.10	I/O0	B1/ PU	**Port 14 General Purpose I/O Line 10**
	AD26	I		**EBU Address/Data Bus Line 26**
	OUT106	O1		**OUT106 Line of GPTA0**
	OUT106	O2		**OUT106 Line of GPTA1**
	OUT106	O3		**OUT106 Line of LTCA2**
	AD26	O		**EBU Address/Data Bus Line 26**
AD25	P14.11	I/O0	B1/ PU	**Port 14 General Purpose I/O Line 11**
	AD27	I		**EBU Address/Data Bus Line 27**
	OUT107	O1		**OUT107 Line of GPTA0**
	OUT107	O2		**OUT107 Line of GPTA1**
	OUT107	O3		**OUT107 Line of LTCA2**
	AD27	O		**EBU Address/Data Bus Line 27**
AC24	P14.12	I/O0	B1/ PU	**Port 14 General Purpose I/O Line 12**
	AD28	I		**EBU Address/Data Bus Line 28**
	OUT108	O1		**OUT108 Line of GPTA0**
	OUT108	O2		**OUT108 Line of GPTA1**
	OUT108	O3		**OUT108 Line of LTCA2**
	AD28	O		**EBU Address/Data Bus Line 28**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AE25	P14.13	I/O0	B1/ PU	**Port 14 General Purpose I/O Line 13**
	AD29	I		**EBU Address/Data Bus Line 29**
	OUT109	O1		**OUT109 Line of GPTA0**
	OUT109	O2		**OUT109 Line of GPTA1**
	OUT109	O3		**OUT109 Line of LTCA2**
	AD29	O		**EBU Address/Data Bus Line 29**
AE24	P14.14	I/O0	B1/ PU	**Port 14 General Purpose I/O Line 14**
	AD30	I		**EBU Address/Data Bus Line 30**
	OUT110	O1		**OUT110 Line of GPTA0**
	OUT110	O2		**OUT110 Line of GPTA1**
	OUT110	O3		**OUT110 Line of LTCA2**
	AD30	O		**EBU Address/Data Bus Line 30**
AD24	P14.15	I/O0	B1/ PU	**Port 14 General Purpose I/O Line 15**
	AD31	I		**EBU Address/Data Bus Line 31**
	OUT111	O1		**OUT111 Line of GPTA0**
	OUT111	O2		**OUT111 Line of GPTA1**
	OUT111	O3		**OUT111 Line of LTCA2**
	AD31	O		**EBU Address/Data Bus Line 31**
Port 15				
AE21	P15.0	I/O0	B1/ PU	**Port 15 General Purpose I/O Line 0**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
	CS0	O		**Chip Select Output Line 0**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AD21	P15.1	I/O0	B1/ PU	**Port 15 General Purpose I/O Line 1**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	CS1	O		**Chip Select Output Line 1**
AD20	P15.2	I/O0	B1/ PU	**Port 15 General Purpose I/O Line 2**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	CS2	O		**Chip Select Output Line 2**
AD19	P15.3	I/O0	B1/ PU	**Port 15 General Purpose I/O Line 3**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	CS3	O		**Chip Select Output Line 3**
AE17	P15.4	I/O0	B1/ PU	**Port 15 General Purpose I/O Line 4**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	BC0	O		**Byte Control Line 0**
AD17	P15.5	I/O0	B1/ PU	**Port 15 General Purpose I/O Line 5**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	BC1	O		**Byte Control Line 1**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AF18	P15.6	I/O0	B1/ PU	**Port 15 General Purpose I/O Line 6**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	BC2	O		**Byte Control Line 2**
AE18	P15.7	I/O0	B1/ PU	**Port 15 General Purpose I/O Line 7**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	BC3	O		**Byte Control Line 3**
AF20	P15.8	I/O0	B1/ PU	**Port 15 General Purpose I/O Line 8**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	RD	O		**Read Control Line**
AF21	P15.9	I/O0	B1/ PU	**Port 15 General Purpose I/O Line 9**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	RD/WR	O		**Write Control Line**
AF22	P15.10	I/O0	B1/ PU	**Port 15 General Purpose I/O Line 10**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	ADV	O		**Address Valid Output**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AE20	P15.11	I/O0	B1/ PU	**Port 15 General Purpose I/O Line 11**
	WAIT	I		**Wait Input for inserting Wait-States**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
AF19	P15.12	I/O0	B1/ PU	**Port 15 General Purpose I/O Line 12**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
	MR/W	O		**Motorola-style Read/Write Control Signal**
AF23	P15.13	I/O0	B1/ PU	**Port 15 General Purpose I/O Line 13**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
	BAA	O		**Burst Address Advance Output**
AF24	P15.14	I/O0	B1/ PU	**Port 15 General Purpose I/O Line 14**
	BFCLKI	I		**Burst FLASH Clock Input (Clock Feedback).**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
AF25	P15.15	I/O0	B2/ PU	**Port 15 General Purpose I/O Line 15**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
	BFCLKO	O		**Burst Mode Flash Clock Output (Non-Differential)**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
Port 16				
AF17	P16.0	I/O0	B1/ PU	**Port 16 General Purpose I/O Line 0**
	HOLD	I		**Hold Request Input**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
AD18	P16.1	I/O0	B1/ PU	**Port 16 General Purpose I/O Line 1**
	HLDA	I		**Hold Acknowledge Output**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
	HLDA	O		**Hold Acknowledge Output**
AD22	P16.2	I/O0	B1/ PU	**Port 16 General Purpose I/O Line 2**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
	BREQ	O		**Bus Request Output**
AE19	P16.3	I/O0	B1/ PU	**Port 16 General Purpose I/O Line 3**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
	CSCOMB	O		**Combined Chip Select Output**
Analog Input Port				
AE1	AN0	I	D	**Analog Input 0**
AD2	AN1	I	D	**Analog Input 1**
AA4	AN2	I	D	**Analog Input 2**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AB3	AN3	I	D	**Analog Input 3**
AC2	AN4	I	D	**Analog Input 4**
AA3	AN5	I	D	**Analog Input 5**
AD1	AN6	I	D	**Analog Input 6**
AB4	AN7	I	D	**Analog Input 7**
AC1	AN8	I	D	**Analog Input 8**
AB2	AN9	I	D	**Analog Input 9**
Y3	AN10	I	D	**Analog Input 10**
AA2	AN11	I	D	**Analog Input 11**
AB1	AN12	I	D	**Analog Input 12**
W3	AN13	I	D	**Analog Input 13**
Y2	AN14	I	D	**Analog Input 14**
AA1	AN15	I	D	**Analog Input 15**
V4	AN16	I	D	**Analog Input 16**
W2	AN17	I	D	**Analog Input 17**
Y1	AN18	I	D	**Analog Input 18**
V3	AN19	I	D	**Analog Input 19**
W1	AN20	I	D	**Analog Input 20**
V2	AN21	I	D	**Analog Input 21**
V1	AN22	I	D	**Analog Input 22**
U1	AN23	I	D	**Analog Input 23**
AC8	AN24	I	D	**Analog Input 24**
AD8	AN25	I	D	**Analog Input 25**
AC7	AN26	I	D	**Analog Input 26**
AD7	AN27	I	D	**Analog Input 27**
AE6	AN28	I	D	**Analog Input 28**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AF6	AN29	I	D	**Analog Input 29**
AE7	AN30	I	D	**Analog Input 30**
AF7	AN31	I	D	**Analog Input 31**
AC3	AN32	I	D	**Analog Input 32**
AE2	AN33	I	D	**Analog Input 33**
AD3	AN34	I	D	**Analog Input 34**
AD5	AN35	I	D	**Analog Input 35**
AE3	AN36	I	D	**Analog Input 36**
AF2	AN37	I	D	**Analog Input 37**
AC4	AN38	I	D	**Analog Input 38**
AF3	AN39	I	D	**Analog Input 39**
AD4	AN40	I	D	**Analog Input 40**
AE4	AN41	I	D	**Analog Input 41**
AC5	AN42	I	D	**Analog Input 42**
AF4	AN43	I	D	**Analog Input 43**
System I/O				
B22	$\overline{\text{PORST}}$	I	Input only/ PD	**Power-on Reset Input** (input pad with input spike-filter)
A23	$\overline{\text{ESR0}}$	I/O	A2	**External System Request Reset Input 0** Default configuration during and after reset is open-drain Driver, corresponding to A2 strong Driver, sharp edge. The Driver drives low during power-on reset.
A22	$\overline{\text{ESR1}}$	I/O	A2/ PD	**External System Request Reset Input 1**
E24	TCK	I	Input only/ PD	**JTAG Module Clock Input**
	DAP0	I		**Device Access Port Line 0**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
E25	TDI	I	A2/ PU	**JTAG Module Serial Data Input**
	$\overline{\text{BRKIN}}$	I		**OCDS Break Input (Alternate Output)**
	$\overline{\text{BRKOUT}}$	O		**OCDS Break Output (Alternate Input)**
B23	$\overline{\text{TESTMODE}}$	I	Input only/ PU	**Test Mode Select Input**
F24	TMS	I	A2/ PD	**JTAG Module State Machine Control Input**
	DAP1	I/O		**Device Access Port Line 1**
F23	$\overline{\text{TRST}}$	I	Input only/ PD	**JTAG Module Reset/Enable Input**
G26	XTAL1	I		**Main Oscillator/PLL/Clock Generator Input**
G25	XTAL2	O		**Main Oscillator/PLL/Clock Generator Output**
D25	TDO	O	A2/ PU	**JTAG Module Serial Data Output**
	$\overline{\text{BRKIN}}$	I		**OCDS Break Input (Alternate Input)**
	$\overline{\text{BRKOUT}}$	O		**OCDS Break Output (Alternate Output)**
	DAP2	O		**Device Access Port Line 2**
A1, AF1, AF26, A24, C22, AC21, AD23, AE22, AE23	N.C.	-	-	**Not connected.** These pins are reserved for future extension and shall not be connected externally.
Power Supply				
W4	V_{DDM}	-	-	**ADC Analog Part Power Supply (3.3V - 5V)**
Y4	V_{SSM}	-	-	**ADC Analog Part Ground**
AE5	V_{AREF0}	-	-	**ADC0 Reference Voltage**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AF5	V_{AGND0}	-	-	**ADC0 Reference Ground**
	V_{AGND2}	-	-	**ADC2 Reference Ground**
AD6	V_{AREF1}	-	-	**ADC1 Reference Voltage**
AC6	V_{AGND1}	-	-	**ADC1 Reference Ground**
AD9	V_{AREF2}	-	-	**ADC2 Reference Voltage**
AF8	V_{FAREF}	-	-	**FADC Reference Voltage**
AE8	V_{FAGND}	-	-	**FADC Reference Ground**
AE9	V_{DDMF}	-	-	**FADC Analog Part Power Supply (3.3V)[1)]**
AC9	V_{DDAF}	-	-	**FADC Analog Part Logic Power Supply (1.5V)**
AF9	V_{SSMF}	-	-	**FADC Analog Part Ground**
	V_{SSAF}	-	-	**FADC Analog Part Logic Ground**
A18, B18, H3	V_{DDFL3}	-	-	**Flash Power Supply (3.3V)**
F25	V_{SSOSC}	-	-	**Main Oscillator Ground**
	V_{SS}	-	-	**Digital Ground**
F26	V_{DDOSC}	-	-	**Main Oscillator Power Supply (1.5V)**
E26	V_{DDOSC3}	-	-	**Main Oscillator Power Supply (3.3V)**
G23	V_{DDPF}	-	-	**E-Ray PLL Power Supply (1.5V)**
G24	V_{DDPF3}	-	-	**E-Ray PLL Power Supply (3.3V)**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AC11, AC20, AB23, V23, P23, E23, D24, C25, B26, D16, D9, H4, R4	V_{DD}	-	-	**Digital Core Power Supply (1.5V)**
AC16, AD16, AE16, AF16, D22, C23, B24, A25, D14, D7, K4	V_{DDP}	-	-	**Port Power Supply (3.3V)**
H23, H24, H25, H26, M23, T23, Y23, AC18, AC22	V_{DDEBU}	-	-	**EBU Port Power Supply (2.5V - 3.3V)**
R1	$V_{DDE(SB)}$	-	-	**Emulation Stand-by SRAM Power Supply (1.5V) (Emulation device only)** *Note: This pin is N.C. in a productive device.*

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AC10, AC17, AC19, AC23, W23, R23, L23, D23, C24, B25, A26, D15, D8, J4, T4	V_{SS}	-	-	**Digital Ground (outer balls)**
K10, K11, K12, K13, K14, K15, K16, K17	V_{SS}	-	-	**Digital Ground (center balls)**
L10, L11, L12, L13, L14, L15, L16, L17	V_{SS}	-	-	**Digital Ground (center balls cont'd)**
M10, M11, M12, M13, M14, M15, M16, M17	V_{SS}	-	-	**Digital Ground (center balls cont'd)**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
N10, N11, N12, N13, N14, N15, N16, N17	V_{SS}	-	-	**Digital Ground (center balls cont'd)**
P10, P11, P12, P13, P14, P15, P16, P17	V_{SS}	-	-	**Digital Ground (center balls cont'd)**
R10, R11, R12, R13, R14, R15, R16, R17	V_{SS}	-	-	**Digital Ground (center balls cont'd)**
T10, T11, T12, T13, T14, T15, T16, T17	V_{SS}	-	-	**Digital Ground (center balls cont'd)**

Table 4 Pin Definitions and Functions (BGA-416 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
U10, U11, U12, U13, U14, U15, U16, U17	V_{SS}	-	-	**Digital Ground (center balls cont'd)**

1) This pin is also connected to the analog power supply for comparator of the ADC module.

Legend for Table 4

Column "**Ctrl.**":

I = Input (for GPIO port Lines with IOCR bit field Selection PCx = $0XXX_B$)

O = Output
O0 = Output with IOCR bit field selection PCx = $1X00_B$
O1 = Output with IOCR bit field selection PCx = $1X01_B$ (ALT1)
O2 = Output with IOCR bit field selection PCx = $1X10_B$ (ALT2)
O3 = Output with IOCR bit field selection PCx = $1X11_B$ (ALT3)

Column "**Type**":

A1 = Pad class A1 (LVTTL)
A2 = Pad class A2 (LVTTL)
F = Pad class F (LVDS/CMOS)
D = Pad class D (ADC)

PU = with pull-up device connected during reset ($\overline{PORST}$ = 0)
PD = with pull-down device connected during reset ($\overline{PORST}$ = 0)
TR = tri-state during reset ($\overline{PORST}$ = 0)

3.1.2 Pull-Up/Pull-Down Reset Behavior of the Pins

Table 5 List of Pull-Up/Pull-Down Reset Behavior of the Pins

Pins	$\overline{PORST}$ = 0	$\overline{PORST}$ = 1
all GPIOs, TDI, $\overline{TESTMODE}$	Pull-up	
$\overline{PORST}$, $\overline{TRST}$, TCK, TMS	Pull-down	

Table 5 List of Pull-Up/Pull-Down Reset Behavior of the Pins

Pins	$\overline{\text{PORST}}$ = 0	$\overline{\text{PORST}}$ = 1
$\overline{\text{ESR0}}$	The open-drain driver is used to drive low.[1]	Pull-up[2]
$\overline{\text{ESR1}}$	Pull-down[2]	
TDO	Pull-up	High-impedance

1) Valid additionally after deactivation of $\overline{\text{PORST}}$ until the internal reset phase has finished. See the SCU chapter for details.

2) See the SCU_IOCR register description.

4 Identification Registers

The Identification Registers uniquely identify a module or the whole device.

Table 4-1 TC1797 Identification Registers [1)]

Short Name	Value	Address	Stepping
ADC0_ID	0059 C000$_H$	F010 1008$_H$	–
ADC1_ID	0059 C000$_H$	F010 1408$_H$	–
ADC2_ID	0059 C000$_H$	F010 1808$_H$	–
ASC0_ID	0000 4402$_H$	F000 0A08$_H$	–
ASC1_ID	0000 4402$_H$	F000 0B08$_H$	–
CAN_ID	002B C051$_H$	F000 4008$_H$	–
CBS_JDPID	0000 6350$_H$	F000 0408$_H$	–
CBS_JTAGID	1015 A083$_H$	F000 0464$_H$	–
CPS_ID	0015 C007$_H$	F7E0 FF08$_H$	–
CPU_ID	000A C006$_H$	F7E1 FE18$_H$	–
DMA_ID	001A C004$_H$	F000 3C08$_H$	–
DMI_ID	0008 C005$_H$	F87F FC08$_H$	–
EBU_ID	0014 C009$_H$	F800 0008$_H$	–
ERAY_ID	0044 C003$_H$	F001 0008$_H$	–
FADC_ID	0027 C003$_H$	F010 0408$_H$	–
FLASH0_ID	0053 C001$_H$	F800 2008$_H$	–
FLASH1_ID	0055 C001$_H$	F800 4008$_H$	–
FPU_ID	0054 C003$_H$	F7E1 A020$_H$	–
GPTA0_ID	0029 C005$_H$	F000 1808$_H$	–
GPTA1_ID	0029 C005$_H$	F000 2008$_H$	–
LBCU_ID	000F C005$_H$	F87F FE08$_H$	–
LFI_ID	000C C006$_H$	F87F FF08$_H$	–
LTCA2_ID	002A C005$_H$	F000 2808$_H$	–
MCHK_ID	001B C001$_H$	F010 C208$_H$	–
MLI0_ID	0025 C007$_H$	F010 C008$_H$	–
MLI1_ID	0025 C007$_H$	F010 C108$_H$	–
MSC0_ID	0028 C003$_H$	F000 0808$_H$	–

Table 4-1 TC1797 Identification Registers (cont'd)[1)]

Short Name	Value	Address	Stepping
MSC1_ID	0028 $C003_H$	F000 0908_H	–
PCP_ID	0020 $C006_H$	F004 $3F08_H$	–
PMI_ID	000B $C005_H$	F87F $FD08_H$	–
PMU0_ID	0050 $C001_H$	F800 0508_H	–
PMU1_ID	0051 $C001_H$	F800 6008_H	–
SBCU_ID	0000 $6A0C_H$	F000 0108_H	–
SCU_CHIPID	0000 9001_H	F000 0640_H	–
SCU_ID	0052 $C001_H$	F000 0508_H	–
SCU_MANID	0000 1820_H	F000 0644_H	–
SCU_RTID	0000 0003_H	F000 0648_H	AC only
SSC0_ID	0000 4511_H	F010 0108_H	–
SSC1_ID	0000 4511_H	F010 0208_H	–
STM_ID	0000 $C006_H$	F000 0208_H	–

1) Valid for all design steps except if explicitely defined.

5 Electrical Parameters

5.1 General Parameters

5.1.1 Parameter Interpretation

The parameters listed in this section partly represent the characteristics of the TC1797 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are marked with an two-letter abbreviation in column “Symbol”:

- **CC**
  Such parameters indicate **C**ontroller **C**haracteristics which are a distinctive feature of the TC1797 and must be regarded for a system design.
- **SR**
  Such parameters indicate **S**ystem **R**equirements which must provided by the microcontroller system in which the TC1797 designed in.

5.1.2 Pad Driver and Pad Classes Summary

This section gives an overview on the different pad driver classes and its basic characteristics. More details (mainly DC parameters) are defined in the **Section 5.2.1**.

Table 6 Pad Driver and Pad Classes Overview

Class	Power Supply	Type	Sub Class	Speed Grade	Load	Leakage[1]	Termination
A	3.3 V	LVTTL I/O, LVTTL outputs	**A1** (e.g. GPIO)	6 MHz	100 pF	500 nA	No
			A2 (e.g. serial I/Os)	40 MHz	50 pF	6 µA	Series termination recommended
B	2.375 - 3.6 V[2]	LVTTL I/O	**B1** (e.g. Ext. Bus Interface)	40 MHz	50 pF	6 µA	No
			B2 (e.g. Bus Clock)	75 MHz	35 pF		Series termination recommended (for f > 25 MHz)
F	3.3 V	LVDS/ CMOS	–	50 MHz	–	–	Parallel termination[3], 100 Ω ± 10%
DE	5 V	ADC	–	–	–	–	see **Table 11**

1) Values are for T_{Jmax} = 150 °C.

2) AC characteristics for EBU pins are valid for 2.5 V ± 5% and 3.3 V ± 5%.

3) In applications where the LVDS pins are not used (disabled), these pins must be either left unconnected, or properly terminated with the differential parallel termination of 100 Ω ± 10%.

5.1.3 Absolute Maximum Ratings

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
During absolute maximum rating overload conditions (V_{IN} > related V_{DD} or V_{IN} < V_{SS}) the voltage on the related V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Table 7 Absolute Maximum Rating Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Ambient temperature	T_A	SR	-40	–	125	°C	Under bias
Storage temperature	T_{ST}	SR	-65	–	150	°C	–
Junction temperature	T_J	SR	-40	–	150	°C	Under bias
Voltage at 1.5 V power supply pins with respect to V_{SS}[1)]	V_{DD}	SR	–	–	2.25	V	–
Voltage at 3.3 V power supply pins with respect to V_{SS}[2)]	V_{DDEBU} V_{DDP}	SR	–	–	3.75	V	–
Voltage at 5 V power supply pins with respect to V_{SS}	V_{DDM}	SR	–	–	5.5	V	–
Voltage on any Class A input pin and dedicated input pins with respect to V_{SS}	V_{IN}	SR	-0.5	–	V_{DDP} + 0.5 or max. 3.7	V	Whatever is lower
Voltage on any Class B input pin with respect to V_{SS}	V_{IN}	SR	-0.5	–	V_{DDEBU} + 0.5 or max. 3.7	V	Whatever is lower
Voltage on any Class D analog input pin with respect to V_{AGND}	V_{AIN} V_{AREFx}	SR	-0.5	–	V_{DDM} + 0.5	V	–
Voltage on any shared Class D analog input pin with respect to V_{SSAF}, if the FADC is switched through to the pin.	V_{AINF} V_{FAREF}	SR	-0.5	–	V_{DDM} + 0.5	V	–
CPU Frequency	f_{CPU}	SR	–	–	180 150	MHz	Derivative dependent

Table 7 Absolute Maximum Rating Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
PCP Frequency	f_{PCP} SR	–	–	180 150	MHz	Derivative dependent
E-Ray Sample Frequency	f_{SAMPLE} SR	–	–	80	MHz	

1) Applicable for V_{DD}, V_{DDOSC}, V_{DDPF}, and V_{DDAF}.

2) Applicable for V_{DDP}, V_{DDEBU}, V_{DDFL3}, V_{DPF3}, and V_{DDMF}.

5.1.4 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the TC1797. All parameters specified in the following table refer to these operating conditions, unless otherwise noticed.

The following operating conditions must not be exceeded in order to ensure correct operation of the TC1797. All parameters specified in the following table refer to these operating conditions, unless otherwise noted.

Table 8 Operating Condition Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital supply voltage[1)]	V_{DD} *SR* V_{DDOSC} SR	1.42	–	1.58[2)]	V	–
	V_{DDP} SR V_{DDOSC3} SR	3.13	–	3.47[3)]	V	For Class A pins (3.3 V ± 5%)
	V_{DDEBU} SR	3.13 2.375	–	3.47[3)] 2.625	V	For Class B (EBU) pins
	V_{DDFL3} SR	3.13	–	3.47[3)]	V	–
Analog supply voltages	V_{DDMF} SR	3.13	–	3.47[3)]	V	FADC
	V_{DDAF} SR	1.42	–	1.58[2)]	V	FADC
	V_{DDM} SR	4.75	–	5.25	V	For Class DE pins, ADC
Digital ground voltage	V_{SS} SR	0	–	–	V	–
Ambient temperature under bias	T_A SR	-40	–	+125	°C	–

Table 8 Operating Condition Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Analog supply voltages	–	–	–	–	–	See separate specification Page 138, Page 143
Overload current at class D pins	I_{OV}	-1	–	3	mA	4)
Sum of overload current at class D pins	$\Sigma\|I_{OV}\|$	–	–	10	mA	per single ADC
Overload coupling factor for analog inputs5)	K_{OVAP}	–	–	5×10-5		0 < I_{OV} < 3 mA
	K_{OVAN}	–	–	5×10-4		-1 mA< I_{OV} < 0
CPU & LMB Bus Frequency	f_{CPU} SR	–	–	180 150	MHz	Derivative dependent
PCP Frequency	f_{PCP} SR	–	–	180 150	MHz	Derivative dependent6)
FPI Bus Frequency	f_{SYS} SR	–	–	90	MHz	6)
Short circuit current	I_{SC} SR	-5	–	+5	mA	7)
Absolute sum of short circuit currents of a pin group (see Table 9)	$\Sigma\|I_{SC\_PG}\|$ SR	–	–	20	mA	See note
Inactive device pin current	I_{ID} SR	-1	–	1	mA	All power supply voltages V_{DDx} = 0
Absolute sum of short circuit currents of the device	$\Sigma\|I_{SC\_D}\|$ SR	–	–	100	mA	See note4)
External load capacitance	C_L SR	–	–	–	pF	Depending on pin class. See DC characteristics

1) Digital supply voltages applied to the TC1797 must be static regulated voltages which allow a typical voltage swing of ±5%.

2) Voltage overshoot up to 1.7 V is permissible at Power-Up and $\overline{\text{PORST}}$ low, provided the pulse duration is less than 100 µs and the cumulated summary of the pulses does not exceed 1 h.

3) Voltage overshoot to 4 V is permissible at Power-Up and $\overline{\text{PORST}}$ low, provided the pulse duration is less than 100 µs and the cumulated summary of the pulses does not exceed 1 h

4) See additional document “TC1767 Pin Reliability in Overload“ for definition of overload current on digital pins.
5) The overload coupling factor (kA) defines the worst case relation of an overload condition (IOV) at one pin to the resulting leakage current (IleakTOT) into an adjacent pin: IleakTOT = ±kA × |IOV| + IOZ1.
Thus under overload conditions an additional error leakage voltage (VAEL) will be induced onto an adjacent analog input pin due to the resistance of the analog input source (RAIN). That means VAEL = RAIN × |IleakTOT|.
The definition of adjacent pins is related to their order on the silicon.
The Injected leakage current always flows in the opposite direction from the causing overload current. Therefore, the total leakage current must be calculated as an algebraic sum of the both component leakage currents (the own leakage current IOZ1 and the optional injected leakage current).
6) The PLL jitter characteristics add to this value according to the application settings. See the PLL jitter parameters.
7) Applicable for digital outputs.

Table 9 Pin Groups for Overload / Short-Circuit Current Sum Parameter

Group	Pins
1	P4.[7:0]
2	P4.[15:8]
3	P10.[5:0]
4	P15.[0, 1, 7:4, 11, 12]
5	P15.[3:0, 8, 13], P16.3
6	P15.9, P16.2, P15.10, P15.[15:14]
7	P14.[15:10]
8	P14.[9:8]
9	P14.[7:2]
10	P14.[1:0], P13.[15:14]
11	P13.[13:12]
12	P13.[11:6]
13	P13.[5:2]
14	P13.[1:0], P12[5:4]
15	P12.[3:0]
16	P11.[15:12]
17	P11.[11:8]
18	P11.[7:4]
19	P11.[3:0]
20	P12.[7:6]

Table 9 Pin Groups for Overload / Short-Circuit Current Sum Parameter

Group	Pins
21	P9.[14:13, 10:9]
22	P9.[12:11, 8:7, 2]
23	P9.[6:5, 3, 1]
24	P9.[0, 4], P5.[10, 11]
25	P5.[15:14, 9:8]
26	P5.[13:12, 6, 4]
27	P5.[7:5, 3, 0]
28	P3.[7:0]
29	P3.[15:8]
30	P0.[7:0]
31	P0.[15:8]
32	P2.[15:9]
33	P2.[8:4]
34	P2.[3:2], P6[9:8]
35	P6[11, 6:4]
36	P6.[15:12, 10, 7]
37	P8.[7:0]
38	P1.[15:13, 11:8, 5]
39	P1.[12, 7, 6, 4, 3]
40	P1.[1:0], P7.0
41	P7.[5:1]
42	P7.[7:6]

5.2 DC Parameters

5.2.1 Input/Output Pins

Table 10 Input/Output DC-Characteristics (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
General Parameters						
Pull-up current[1]	$\lvert I_{PUH}\rvert$ CC	10	–	100	µA	$V_{IN} < V_{IHAmin}$; class A1/A2/F/Input pads.
		5	–	85	µA	$V_{IN} < V_{IHBmin}$; class B1/B2 pads.
Pull-down current[1]	$\lvert I_{PDL}\rvert$ CC	10	–	150	µA	$V_{IN} > V_{ILAmax}$; class A1/A2/F/Input pads. $V_{IN} > V_{ILBmax}$; class B1/B2 pads
Pin capacitance[1] (Digital I/O)	C_{IO} CC	–	–	10	pF	f = 1 MHz T_A = 25 °C
Input only Pads (V_{DDP} = 3.13 to 3.47 V = 3.3 V ± 5%)						
Input low voltage	V_{ILI} SR	-0.3	–	0.36 × V_{DDP}	V	–
Input high voltage	V_{IHI} SR	0.62 × V_{DDP}	–	V_{DDP}+ 0.3 or max. 3.6	V	Whatever is lower
Ratio V_{IL}/V_{IH}	CC	0.58	–	–	–	–
Input high voltage TRST, TCK	V_{IHJ} SR	0.64 × V_{DDP}	–	V_{DDP}+ 0.3 or max. 3.6	V	Whatever is lower
Input hysteresis	HYSI CC	0.1 × V_{DDP}	–	–	V	[4]
Input leakage current	I_{OZI} CC	–	–	±3000 ±6000	nA	((V_{DDP}/2)-1) < V_{IN} < ((V_{DDP}/2)+1) Otherwise[2]

Table 10 Input/Output DC-Characteristics (cont'd)(Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Spike filter always blocked pulse duration	t_{SF1} CC	–	–	10	ns	
Spike filter pass-through pulse duration	t_{SF2} CC	100	–	–	ns	
Class A Pads (V_{DDP} = 3.13 to 3.47 V = 3.3V ± 5%)						
Output low voltage [3]	V_{OLA} CC	–	–	0.4	V	I_{OL} = 2 mA for medium and strong driver mode, I_{OL} = 500 µA for weak driver mode
Output high voltage[2] [3]	V_{OHA} CC	2.4	–	–	V	I_{OH} = -2 mA for medium and strong driver mode, I_{OH} = -500 µA for weak driver mode
		V_{DDP} - 0.4	–	–	V	I_{OH} = -1.4 mA for medium and strong driver mode, I_{OH} = -400 µA for weak driver mode
Input low voltage Class A1/2 pins	V_{ILA} SR	-0.3	–	0.36 × V_{DDP}	V	–
Input high voltage Class A1 pins	V_{IHA1} SR	0.62 × V_{DDP}	–	V_{DDP}+ 0.3 or max. 3.6	V	Whatever is lower
Ratio V_{IL}/V_{IH} Class A1 pins	CC	0.58	–	–	–	–
Input high voltage Class A2 pins	V_{IHA2} SR	0.60 × V_{DDP}	–	V_{DDP}+ 0.3 or max. 3.6	V	Whatever is lower
Ratio V_{IL}/V_{IH} Class A2 pins	CC	0.6	–	–	–	–
Input hysteresis	HYSA CC	0.1 × V_{DDP}	–	–	V	[4]

Table 10 Input/Output DC-Characteristics (cont'd)(Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input leakage current Class A2 pins	I_{OZA2} CC	–	–	±3000 ±6000	nA	$((V_{DDP}/2)-1) < V_{IN} < ((V_{DDP}/2)+1)$ Otherwise[2]
Input leakage current Class A1 pins	I_{OZA1} CC	–	–	±500	nA	$0\ V < V_{IN} < V_{DDP}$
Class B Pads (V_{DDEBU} = 2.375 to 3.47 V)						
Output low voltage	V_{OLB} CC	–	–	0.4	V	I_{OL} = 2 mA
Output high voltage	V_{OHB} CC	V_{DDEBU} - 0.4	–	–	V	I_{OL} = 2 mA
Input low voltage	V_{ILB} SR	-0.3	–	$0.34 \times V_{DDEBU}$	V	–
Input high voltage	V_{IHB} SR	$0.64 \times V_{DDEBU}$	–	V_{DDEBU} + 0.3 or max. 3.6	V	Whatever is lower
Ratio V_{IL}/V_{IH}	CC	0.53	–	–	–	–
Input hysteresis	HYSB CC	$0.1 \times V_{DDEBU}$	–	–	V	[4]
Input leakage current Class B pins	I_{OZB} CC	–	–	±3000 ±6000	nA	$((V_{DDEBU}/2)-0.6) < V_{IN} < ((V_{DDEBU}/2)+0.6)$[5] Otherwise[2]
Class F Pads, LVDS Mode (V_{DDP} = 3.13 to 3.47 V = 3.3V ± 5%)						
Output low voltage	V_{OL} CC	875	–	–	mV	Parallel termination 100 Ω ± 1%
Output high voltage	V_{OH} CC		–	1525	mV	Parallel termination 100 Ω ± 1%
Output differential voltage	V_{OD} CC	150	–	400	mV	Parallel termination 100 Ω ± 1%
Output offset voltage	V_{OS} CC	1075	–	1325	mV	Parallel termination 100 Ω ± 1%
Output impedance	R_0 CC	40	–	140	Ω	–

Table 10 Input/Output DC-Characteristics (cont'd)(Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Class F Pads, CMOS Mode (V_{DDP} = 3.13 to 3.47 V = 3.3V ± 5%)						
Input low voltage Class F pins	V_{ILF} SR	-0.3	–	0.36 × V_{DDP}	V	–
Input high voltage Class F pins	V_{IHF} SR	0.60 × V_{DDP}	–	V_{DDP}+ 0.3 or max. 3.6	V	Whatever is lower
Input hysteresis Class F pins	HYSF CC	0.05 × V_{DDP}	–	–	V	
Input leakage current Class F pins	I_{OZF}	–	–	±3000 ±6000	nA	((V_{DDP}/2)-1) < V_{IN} < ((V_{DDP}/2)+1) Otherwise[2]
Output low voltage [6]	V_{OLF} CC	–	–	0.4	V	I_{OL} = 2 mA
Output high voltage[2] [6]	V_{OHF} CC	2.4	–	–	V	I_{OH} = -2 mA
		V_{DDP} - 0.4	–	–	V	I_{OH} = -1.4 mA
Class D Pads						
See ADC Characteristics		–	–	–	–	–

1) Not subject to production test, verified by design / characterization.

2) Only one of these parameters is tested, the other is verified by design characterization

3) Maximum resistance of the driver R_{DSON}, defined for P_MOS / N_MOS transistor separately:
25 / 20 Ω for strong driver mode, $I_{OH/L}$ < 2 mA,
200 / 150 Ω for medium driver mode, $I_{OH/L}$ < 400 uA,
600 / 400 Ω for weak driver mode, $I_{OH/L}$ < 100 uA,
verified by design / characterization.

4) Function verified by design, value verified by design characterization.
Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce.
It cannot be guaranteed that it suppresses switching due to external system noise.

5) V_{DDEBU} = 2.5 V ± 5%. For V_{DDEBU} = 3.3 ± 5% see class A2 pads.

6) The following constraint applies to an LVDS pair used in CMOS mode: only one pin of a pair should be used as output, the other should be used as input, or both pins should be used as inputs. Using both pins as outputs is not recommended because of the higher crosstalk between them.

5.2.2 Analog to Digital Converters (ADC0/ADC1/ADC2)

All ADC parameters are optimized for and valid in the range of V_{DDM} = 5V ± 5%.

Table 11 ADC Characteristics (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Analog supply voltage	V_{DDM}	SR	4.75	5	5.25 [1)]	V	–
			3.13	3.3	3.47	V	–
	V_{DD}	SR	1.42	1.5	1.58[2)]	V	Power supply for ADC digital part, internal supply
Analog ground voltage	V_{SSM}	SR	-0.1	–	0.1	V	–
Analog reference voltage[16)]	V_{AREFx}	SR	V_{AGNDx}+1 V	V_{DDM}	V_{DDM}+ 0.05 [1)3)4)]	V	–
Analog reference ground[16)]	V_{AGNDx}	SR	V_{SSMx} - 0.05V	0	V_{AREF} - 1V	V	–
Analog input voltage range	V_{AIN}	SR	V_{AGNDx}	–	V_{AREFx}	V	–
Analog reference voltage range[5)16)]	V_{AREFx}- V_{AGNDx}	SR	V_{DDM}/2	–	V_{DDM} + 0.05	V	–
Converter Clock	f_{ADC}	SR	1	–	90	MHz	–
Internal ADC clocks	f_{ADCI}	CC	0.5	–	10	MHz	–
Sample time	t_S	CC	2	–	257	TADCI	–
Total unadjusted error[5)]	TUE[6)]	CC	–	–	±4	LSB	12-bit conversion, without noise[7)8)]
			–	–	±2	LSB	10-bit conversion[8)]
			–	–	±1	LSB	8-bit conversion[8)]
DNL error[9) 5)]	EA_{DNL}	CC	–	±1.5	±3.0	LSB	12-bit conversion without noise[8)10)]
INL error[9)5)]	EA_{INL}	CC	–	±1.5	±3.0	LSB	12-bit convesion without noise[8)10)]

Table 11 ADC Characteristics (cont'd) (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gain error[9)5)]	EA_{GAIN} CC	–	±0.5	±3.5	LSB	12-bit conversion without noise[8)10)]
Offset error[9)5)]	EA_{OFF} CC	–	±1.0	±4.0	LSB	12-bit converson without noise[8)10)]
Input leakage current at analog inputs of ADC0/1 [11) 12) 13)]	I_{OZ1} CC	-300	–	100	nA	(0% V_{DDM}) < V_{IN} < (3% V_{DDM})
		-100	–	200	nA	(3% V_{DDM}) < V_{IN} < (97% V_{DDM})
		-100	–	300	nA	(97% V_{DDM}) < V_{IN} < (100% V_{DDM})
Input leakage current at $V_{AREF0/1/2,}$ per module	I_{OZ2} CC	–	–	±1.5	µA	0 V < V_{AREF} < $V_{DDM,}$ no conversion running
Input current at $V_{AREF0/1/2}$[16)], per module	I_{AREF} CC	–	35	75	µA rms	0 V < V_{AREF} < V_{DDM}[14)]
Total capacitance of the voltage reference inputs[15)16)]	$C_{AREFTOT}$ CC	–	20	40	pF	[8)]
Switched capacitance at the positive reference voltage input[16)]	C_{AREFSW} CC	–	15	30	pF	[8)17)]
Resistance of the reference voltage input path[15)]	R_{AREF} CC	–	500	1000	Ω	500 Ohm increased for AN[1:0] used as reference input[8)]
Total capacitance of the analog inputs[15)]	C_{AINTOT} CC	–	25	30	pF	[1)8)]

Table 11 ADC Characteristics (cont'd) (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Switched capacitance at the analog voltage inputs	C_{AINSW}	CC	–	7	20	pF	8)18)
ON resistance of the transmission gates in the analog voltage path	R_{AIN}	CC	–	700	1500	Ω	8)
ON resistance for the ADC test (pull-down for AIN7)	R_{AIN7T}	CC	180	550	900[19)]	Ω	Test feature available only for AIN7[8) 20)]
Current through resistance for the ADC test (pull-down for AIN7)	I_{AIN7T}	CC	–	15 rms	30 peak	mA	Test feature available only for AIN7[8)]

1) Voltage overshoot to tbd. V are permissible, provided the pulse duration is less than 100 µs and the cumulated summary of the pulses does not exceed 1 h.

2) Voltage overshoot to 1.7 V are permissible, provided the pulse duration is less than 100 µs and the cumulated summary of the pulses does not exceed 1 h.

3) A running conversion may become inexact in case of violating the normal operating conditions (voltage overshoot).

4) If the reference voltage V_{AREF} increases or the V_{DDM} decreases, so that V_{AREF} = (V_{DDM} + 0.05 V to V_{DDM} + 0.07V), then the accuracy of the ADC decreases by 4LSB12.

5) If a reduced reference voltage in a range of V_{DDM}/2 to V_{DDM} is used, then the ADC converter errors increase. If the reference voltage is reduced with the factor k (k<1), then TUE, DNL, INL Gain and Offset errors increase with the factor 1/k.
If a reduced reference voltage in a range of 1 V to V_{DDM}/2 is used, then there are additional decrease in the ADC speed and accuracy.

6) TUE is tested at V_{AREF} = 5.0 V, V_{AGND} = 0 V and V_{DDM} = 5.0 V

7) ADC module capability.

8) Not subject to production test, verified by design / characterization.

9) The sum of DNL/INL/Gain/Offset errors does not exceed the related TUE total unadjusted error.

10) For 10-bit conversions the DNL/INL/Gain/Offset error values must be multiplied with factor 0.25.
For 8-bit conversions the DNL/INL/Gain/Offset error values must be multiplied with 0.0625.

11) The leakage current definition is a continuous function, as shown in **Figure 21**. The numerical values defined determine the characteristic points of the given continuous linear approximation - they do not define step function.

12) Only one of these parameters is tested, the other is verified by design characterization.

13) The leakage current decreases typically 30% for junction temperature decrease of 10oC.

14) I_{AREF_MAX} is valid for the minimum specified conversion time. The current flowing during an ADC conversion with a duration of up to t_C = 25 µs can be calculated with the formula $I_{AREF\_MAX} = Q_{CONV} / t_C$. Every conversion needs a total charge of Q_{CONV} = 150 pC from V_{AREF}.
All ADC conversions with a duration longer than t_C = 25µs consume an I_{AREF_MAX} = 6µA.

15) For the definition of the parameters see also **Figure 20**.

16) Applies to AINx, when used as auxiliary reference inputs.

17) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead of this smaller capacitances are successively switched to the reference voltage.

18) The sampling capacity of the conversion C-Network is pre-charged to V_{AREF} / 2 before the sampling moment. Because of the parasitic elements the voltage measured at AINx deviates from V_{AREF}/2, and is typically 1.35 V.

19) RAIN7T = 1400 Ohm maximum and 830 Ohm typical in the V_{DDM} = 3.3 V ± 5% range.

20) The DC current at the pin is limited to 3 mA for the operational lifetime.

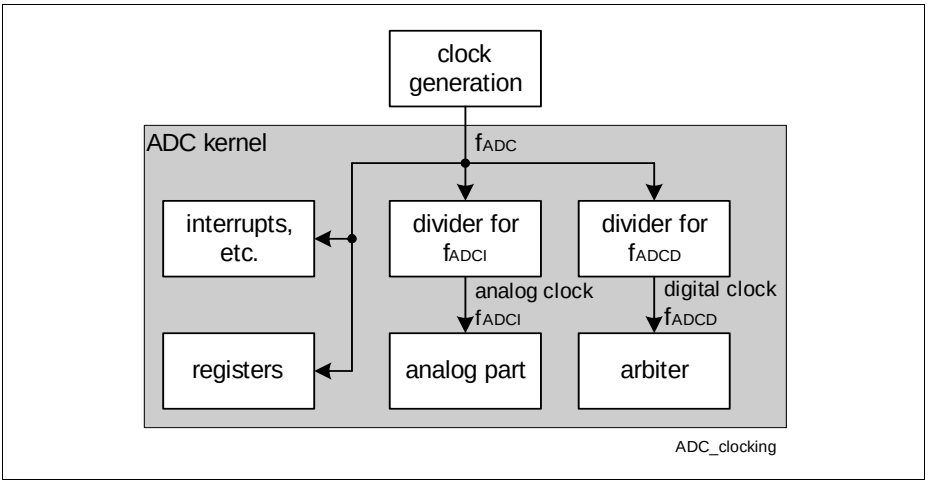


Figure 19 ADC0/ADC1 Clock Circuit

Table 12 Conversion Time (Operating Conditions apply)

Parameter	Symbol	Value	Unit	Note
Conversion time with post-calibration	t_C CC	$2 \times T_{ADC} + (4 + STC + n) \times T_{ADCI}$	µs	n = 8, 10, 12 for n - bit conversion $T_{ADC} = 1 / f_{ADC}$ $T_{ADCI} = 1 / f_{ADCI}$
Conversion time without post-calibration		$2 \times T_{ADC} + (2 + STC + n) \times T_{ADCI}$		

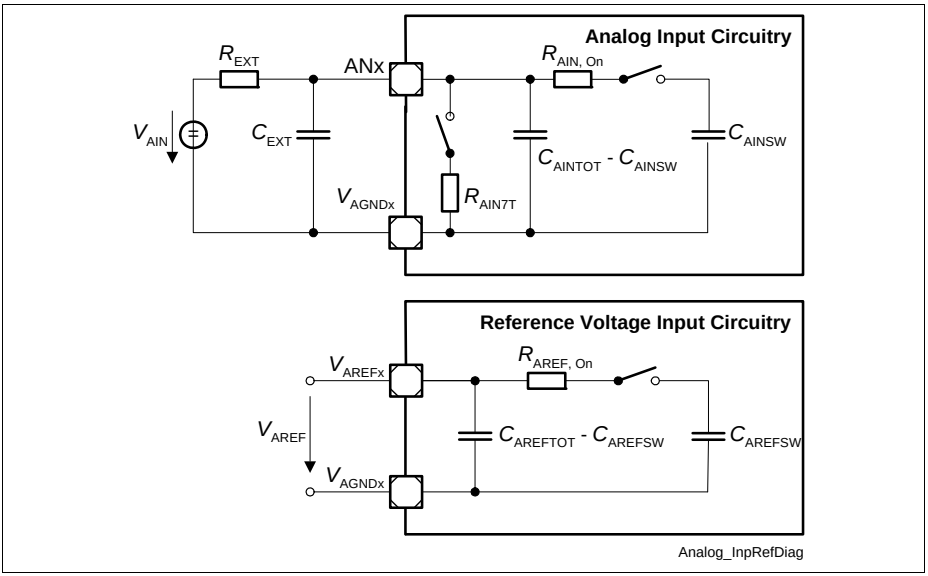


Figure 20 ADC0/ADC1 Input Circuits

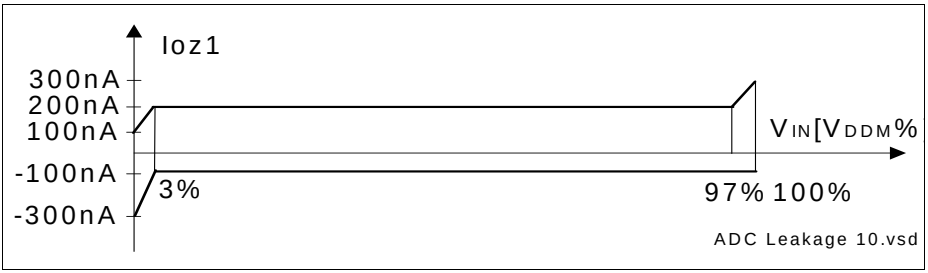


Figure 21 ADC0/ADC1Analog Inputs Leakage

5.2.3 Fast Analog to Digital Converter (FADC)

All parameters apply to FADC used in differential mode, which is the default and the intended mode of operation, and which takes advantage of many error cancelation effects inherent to differential measurements in general.

Table 13 FADC Characteristics (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DNL error	EF_{DNL} CC	–	–	±1	LSB	9)
INL error	EF_{INL} CC	–	–	±4	LSB	9)
Gradient error9)	EF_{GRAD} CC	–	–	±5	%	Without calibration gain 1, 2, 4
		–	–	±6	%	Without calibration gain 8
Offset error9)1)	EF_{OFF} 2) CC	–	–	±20 3)	mV	With calibration1)
		–	–	±90 3)	mV	Without calibration
Reference error of internal V_{FAREF}/2	EF_{REF} CC	–	–	±60	mV	–
Analog supply voltages	V_{DDMF} SR	3.13	–	3.47 4)	V	–
	V_{DDAF} SR	1.42	–	1.58 5)	V	–
Analog ground voltage	V_{SSAF} SR	-0.1	–	0.1	V	–
Analog reference voltage	V_{FAREF} SR	3.13	–	3.47 4)6)	V	Nominal 3.3 V
Analog reference ground	V_{FAGND} SR	V_{SSAF} - 0.05 V	–	V_{SSAF} + 0.05 V	V	–
Analog input voltage range	V_{AINF} SR	V_{FAGND}	–	V_{DDMF}	V	–
Analog supply currents	I_{DDMF} SR	–	–	15	mA	–
	I_{DDAF} SR	–	–	12	mA	7)
Input current at V_{FAREF}	I_{FAREF} CC	–	–	120	µA rms	Independent of conversion
Input leakage current at V_{FAREF} 8)	I_{FOZ2} CC	–	–	±500	nA	0 V < V_{IN} < V_{DDMF}
Input leakage current at V_{FAGND} 8)	I_{FOZ3} CC	–	–	±8	µA	0 V < V_{IN} < V_{DDMF}

Table 13 FADC Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Conversion time	t_C	CC	–	–	21	CLK of f_{ADC}	For 10-bit conv.
Converter Clock	f_{FADC}	SR	–	–	90	MHz	–
Input resistance of the analog voltage path (Rn, Rp)	R_{FAIN}	CC	100	–	200	kΩ	9)
Channel Amplifier Cutoff Frequency9)	f_{COFF}	CC	2	–	–	MHz	–
Settling Time of a Channel Amplifier after changing ENN or ENP9)	t_{SET}	CC	–	–	5	µs	–

1) Calibration should be performed at each power-up. In case of continuous operation, calibration should be performed minimum once per week, or on regular basis in order to compensate for temperature changes.

2) The offset error voltage drifts over the whole temperature range maximum ±6 LSB.

3) Applies when the gain of the channel equals one. For the other gain settings, the offset error increases; it must be multiplied with the applied gain.

4) Voltage overshoots up to 4 V are permissible, provided the pulse duration is less than 100 µs and the cumulated summary of the pulses does not exceed 1 h.

5) Voltage overshoots up to 1.7 V are permissible, provided the pulse duration is less than 100 µs and the cumulated sum of the pulses does not exceed 1 h.

6) A running conversion may become inexact in case of violating the normal operating conditions (voltage overshoots).

7) Current peaks of up to 40 mA with a duration of max. 2 ns may occur

8) This value applies in power-down mode.

9) Not subject to production test, verified by design / characterization.

The calibration procedure should run after each power-up, when all power supply voltages and the reference voltage have stabilized. The offset calibration must run first, followed by the gain calibration.

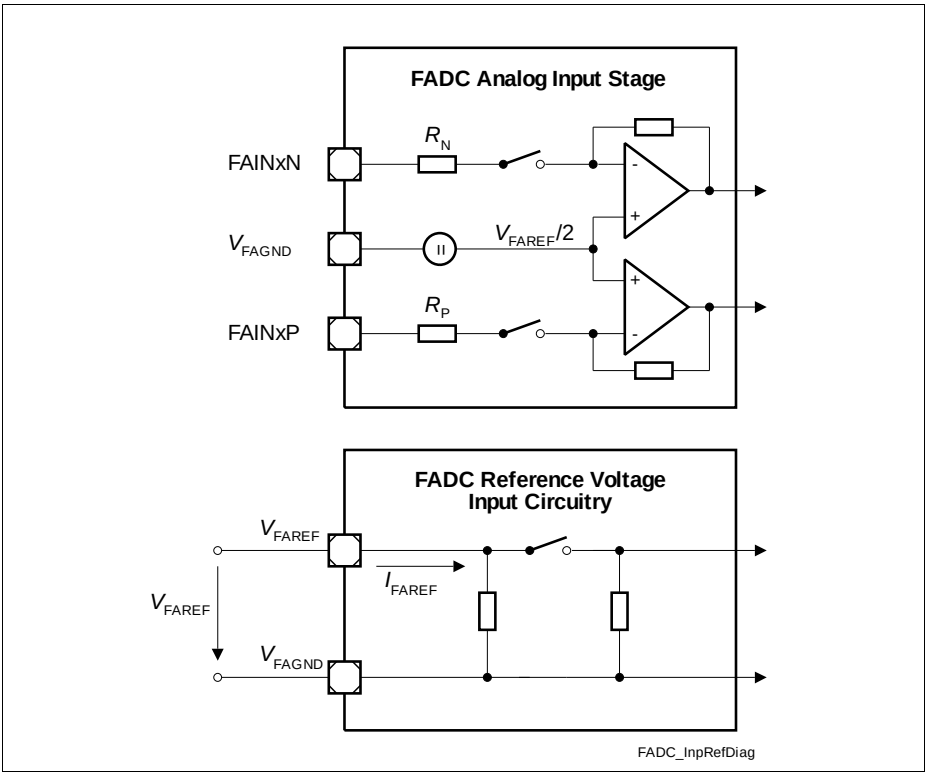


Figure 22 FADC Input Circuits

5.2.4 Oscillator Pins

Table 14 Oscillator Pins Characteristics (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Frequency Range	f_{OSC}	CC	4	–	40	MHz	Direct Input Mode selected
			8	–	25	MHz	External Crystal Mode selected
Input low voltage at XTAL1[1]	V_{ILX}	SR	-0.2	–	$0.3 \times V_{DDOSC3}$	V	–
Input high voltage at XTAL1[1]	V_{IHX}	SR	$0.7 \times V_{DDOSC3}$	–	$V_{DDOSC3} + 0.2$	V	–
Input current at XTAL1	I_{IX1}	CC	–	–	±25	µA	$0\ V < V_{IN} < V_{DDOSC3}$

1) If the XTAL1 pin is driven by a crystal, reaching a minimum amplitude (peak-to-peak) of $0.3 \times V_{DDOSC3}$ is necessary.

Note: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal supplier.

5.2.5 Temperature Sensor

Table 15 Temperature Sensor Characteristics (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Temperature sensor range	T_{SR}	SR	-40		150	°C	Junction temperature
Temperature sensor measurement time	t_{TSMT}	SR	–	–	100	µs	–
Start-up time after reset	t_{TSST}	SR	–	–	10	µs	–
Sensor accuracy	T_{TSA}	CC	–	–	±6[1]	°C	Calibrated

1) Not subject to production test, verified by design / characterization.

The following formula calculates the temperature measured by the DTS in [^{o}C] from the RESULT bitfield of the DTSSTAT register.

(1)

$$Tj = \frac{DTSSTAT_{RESULT} - 619}{2,28}$$

5.2.6 Power Supply Current

The default test conditions (differences explicitly specified) are:
VDD=1.58 V, VDD=3.47 V, fCPU=180 MHz, Tj=150oC

Table 16 Power Supply Currents (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Core active mode supply current[1)2) 3)]	I_{DD}	CC	–	–	600	mA	f_{CPU}=180 MHz f_{CPU}/f_{SYS} = 2:1
Realistic core active mode supply current [4) 5)]			–	–	430	mA	V_{DD} = 1.53 V, T_J = 150°C
E-Ray PLL 1.5 V supply	I_{DDPF}	CC	–	–	4	mA	–
E-Ray PLL 3.3 V supply	I_{DDPF3}	CC	–	–	5	mA	– [5)]
FADC 3.3 V analog supply current	I_{DDMF}	CC	–	–	15	mA	–
FADC 1.5 V analog supply current	I_{DDAF}	CC	–	–	12	mA	– [5)]
Flash memory 3.3 V supply current	I_{DDFL3R}	CC	–	–	125	mA	continuously reading the Flash memory [6)]
	I_{DDFL3E}	CC	–	–	120	mA	Flash memory erase-verify [7)]
Oscillator 1.5 V supply	I_{DDOSC}	CC	–	–	3	mA	– [5)]
Oscillator 3.3 V supply	I_{DDOSC3}	CC	–	–	10	mA	– [5)]
LVDS 3.3 V supply	I_{LVDS}		–	–	30	mA	in total for four pairs
Pad currents, sum of V_{DDP} 3.3 V supplies	I_{DDP}	CC	–	–	30	mA	– [5) 8)]
	I_{DDP_FP}	CC	–	–	54	mA	I_{DDP} including Data Flash programming current [8) 9)]
ADC 5 V power supply	I_{DDM}	CC	–	–	6	mA	ADC0/1/2
Maximum Average Power Dissipation[1)]	P_D	SR	–	–	1800	mW	worst case T_A = 125°C, $P_D \times R_{\Theta JA}$ < 25°C

1) Infineon Power Loop: CPU and PCP running, all peripherals active. The power consumption of each custom application will most probably be lower than this value, but must be evaluated separately.

2) The I_{DD} maximum value is 530 mA at f_{CPU} = 150 MHz, constant T_J = 150°C, for the Infineon Max Power Loop. The dependency in this range is, at constant junction temperature, linear.
f_{CPU}/f_{SYS} = 2:1 mode.

3) Not using the E-Ray module, E-Ray PLL in an application lowers the current consumption for typically 9mA.
4) The I_{DD} maximum value is 390 mA at f_{CPU} = 150 MHz, constant T_J = 150°C, for the Realistic Pattern.
The dependency in this range is, at constant junction temperature, linear.
f_{CPU}/f_{SYS} = 2:1 mode.
5) Not tested in production separately, verified by design / characterization.
6) This value assumes worst case of reading flash line with all cells erased. In case of 50% cells written with “1” and 50% cells written with “0”, the maximum current drops down to 95 mA.
7) Relevant for the power supply dimensioning, not for thermal considerations.
In case of erase of Data Flash, internal flash array loading effects may generate transient current spikes of up to 15 mA for maximum 5 ms.
8) No GPIO and EBU activity, LVDS off
9) This value is relevant for the power supply dimensioning. The currents caused by the GPIO and EBU activity depend on the particular application and should be added separately. If two Flash modules are programmed in parallel, the current increase is 2 × 24 mA.

5.3 AC Parameters

All AC parameters are defined with the temperature compensation disabled. That means, keeping the pads constantly at maximum strength.

5.3.1 Testing Waveforms

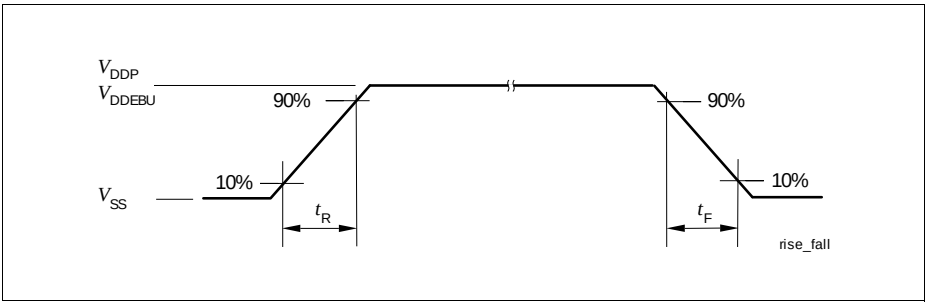


Figure 23 Rise/Fall Time Parameters

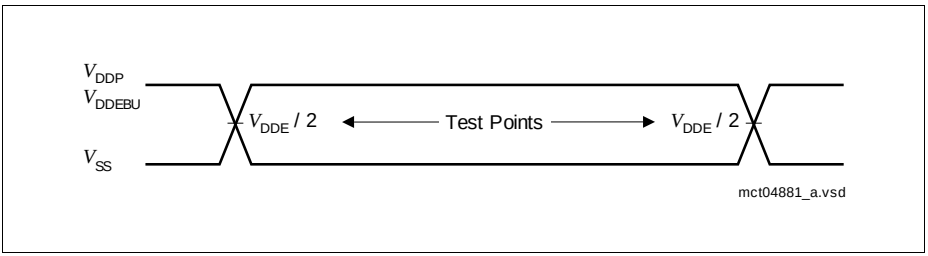


Figure 24 Testing Waveform, Output Delay

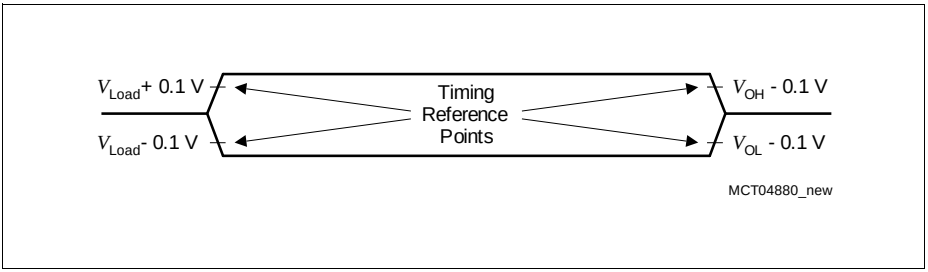


Figure 25 Testing Waveform, Output High Impedance

5.3.2 Output Rise/Fall Times

Table 17 Output Rise/Fall Times (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Class A1 Pads						
Rise/fall times[1)]	t_{RA1}, t_{FA1}	–	–	50 140 18000 150 550 65000	ns	Regular (medium) driver, 50 pF Regular (medium) driver, 150 pF Regular (medium) driver, 20 nF Weak driver, 20 pF Weak driver, 150 pF Weak driver, 20 000 pF
Class A2 Pads						
Rise/fall times[1)]	t_{RA2}, t_{FA2}	–	–	3.7 7.5 7 18 50 140 18000 150 550 65000	ns	Strong driver, sharp edge, 50 pF Strong driver, sharp edge, 100pF Strong driver, med. edge, 50 pF Strong driver, soft edge, 50 pF Medium driver, 50 pF Medium driver, 150 pF Medium driver, 20 000 pF Weak driver, 20 pF Weak driver, 150 pF Weak driver, 20 000 pF
Class B Pads 3.3V ± 5%						
Rise/fall times[1)2)]	t_{RB}, t_{FB}	–	–	3.0 3.7 7.5	ns	35 pF 50 pF 100 pF
Class B Pads 2.5V ± 5%						
Rise/fall times[1)3)]	t_{RB}, t_{FB}	–	–	3.7 4.6 9.0	ns	35 pF 50 pF 100 pF
Class F Pads						
Rise/fall times	t_{RF1}, t_{RF1}	–	–	2	ns	LVDS Mode
Rise/fall times	t_{RF2}, t_{RF2}	–	–	60	ns	CMOS Mode, 50 pF

1) Not all parameters are subject to production test, but verified by design/characterization and test correlation.

2) Parameter test correlation for V_{DDEBU} = 2.5 V ± 5%

3) Parameter test correlation for V_{DDEBU} = 2.5 V ± 5%

5.3.3 Power Sequencing

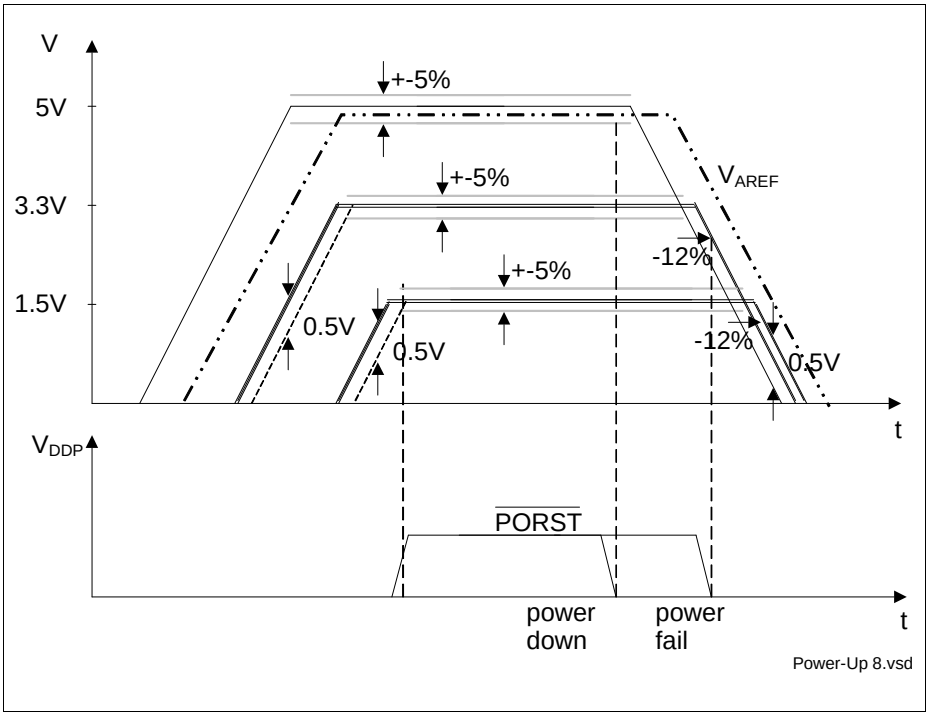


Figure 26 5 V / 3.3 V / 1.5 V Power-Up/Down Sequence

The following list of rules applies to the power-up/down sequence:

- All ground pins V_{SS} must be externally connected to one single star point in the system. Regarding the DC current component, all ground pins are internally directly connected.
- At any moment,
  each power supply must be higher than any lower_power_supply - 0.5 V, or:
  VDD5 > VDD3.3 - 0.5 V; VDD5 > VDD1.5 - 0.5 V;VDD3.3 > VDD1.5 - 0.5 V, see **Figure 26**.
- During power-up and power-down, the voltage difference between the power supply pins of the same voltage (3.3 V, 1.5 V, and 5 V) with different names (for example VDDP, VDDFL3 ...), that are internally connected via diodes, must be lower than 100 mV. On the other hand, all power supply pins with the same name (for example

all VDDP), are internally directly connected. It is recommended that the power pins of the same voltage are driven by a single power supply.

- The PORST signal may be deactivated after all VDD5, VDD3.3, VDD1.5, and VAREF power-supplies and the oscillator have reached stable operation, within the normal operating conditions.
- At normal power down the PORST signal should be activated within the normal operating range, and then the power supplies may be switched off. Care must be taken that all Flash write or delete sequences have been completed.
- At power fail the PORST signal must be activated at latest when any 3.3 V or 1.5 V power supply voltage falls 12% below the nominal level. The same limit of 3.3 V-12% applies to the 5 V power supply too. If, under these conditions, the PORST is activated during a Flash write, only the memory row that was the target of the write at the moment of the power loss will contain unreliable content. In order to ensure clean power-down behavior, the PORST signal should be activated as close as possible to the normal operating voltage range.
- In case of a power-loss at any power-supply, all power supplies must be powered-down, conforming at the same time to the rules number 2 and 4.
- Although not necessary, it is additionally recommended that all power supplies are powered-up/down together in a controlled way, as tight to each other as possible.
- Aditionally, regarding the ADC reference voltage VAREF:
  - VAREF must power-up at the same time or later than VDDM, and
  - VAREF must power-down eather earlier or at latest to satisfy the condition VAREF < VDDM + 0.5 V. This is required in order to prevent discharge of VAREF filter capacitance through the ESD diodes through the VDDM power supply. In case of discharging the reference capacitance through the ESD diodes, the current must be lower than 5 mA.

5.3.4 Power, Pad and Reset Timing

Table 18 Power, Pad and Reset Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Min. V_{DDP} voltage to ensure defined pad states[1]	V_{DDPPA}	CC	0.6	–	–	V	–
Oscillator start-up time[2]	t_{OSCS}	CC	–	–	10	ms	–
Minimum $\overline{\text{PORST}}$ active time after power supplies are stable at operating levels	t_{POA}	SR	10	–	–	ms	–
$\overline{\text{ESR0}}$ pulse width	t_{HD}	CC	Programmable[3][5]	–	–	f_{SYS}	–
$\overline{\text{PORST}}$ rise time	t_{POR}	SR	–	–	50	ms	–
Setup time to $\overline{\text{PORST}}$ rising edge[4]	t_{POS}	SR	0	–	–	ns	–
Hold time from $\overline{\text{PORST}}$ rising edge	t_{POH}	SR	100	–	–	ns	$\overline{\text{TESTMODE}}$ $\overline{\text{TRST}}$
Setup time to $\overline{\text{ESR0}}$ rising edge	t_{HDS}	SR	0	–	–	ns	–
Hold time from $\overline{\text{ESR0}}$ rising edge	t_{HDH}	SR	$16 \times 1/f_{SYS}$[5]	–	–	ns	HWCFG
Ports inactive after $\overline{\text{PORST}}$ reset active[6][7]	t_{PIP}	CC	–	–	150	ns	–
Ports inactive after $\overline{\text{ESR0}}$ reset active (and for all logic)	t_{PI}	CC	–	–	$8 \times 1/f_{SYS}$	ns	–
Power on Reset Boot Time[8]	t_{BP}	CC	–	–	2.5	ms	–
Application Reset Boot Time at f_{CPU}=180MHz[9][10]	t_B	CC	125	–	575	µs	–

1) This parameter is valid under assumption that $\overline{\text{PORST}}$ signal is constantly at low level during the power-up/power-down of the V_{DDP}.

2) t_{OSCS} is defined from the moment when V_{DDOSC3} = 3.13 V until the oscillations reach an amplitude at XTAL1 of 0,3 × V_{DDOSC3}. This parameter is verified by device characterization. The external oscillator circuitry must be optimized by the customer and checked for negative resistance as recommended and specified by crystal suppliers.

3) Any $\overline{\text{ESR0}}$ activation is internally prolonged to SCU_RSTCNTCON.RELSA FPI bus clock (f_{FPI}) cycles.

4) Applicable for input pins $\overline{\text{TESTMODE}}$ and $\overline{\text{TRST}}$.
5) $f_{FPI} = f_{CPU}/2$
6) Not subject to production test, verified by design / characterization.
7) This parameter includes the delay of the analog spike filter in the $\overline{\text{PORST}}$ pad.
8) The duration of the boot-time is defined between the rising edge of the $\overline{\text{PORST}}$ and the moment when the first user instruction has entered the CPU and its processing starts.
9) The duration of the boot time is defined between the rising edge of the internal application reset and the clock cycle when the first user instruction has entered the CPU pipeline and its processing starts.
10) The given time includes the time of the internal reset extension for a configured value of SCU_RSTCNTCON.RELSA = 0x05BE.

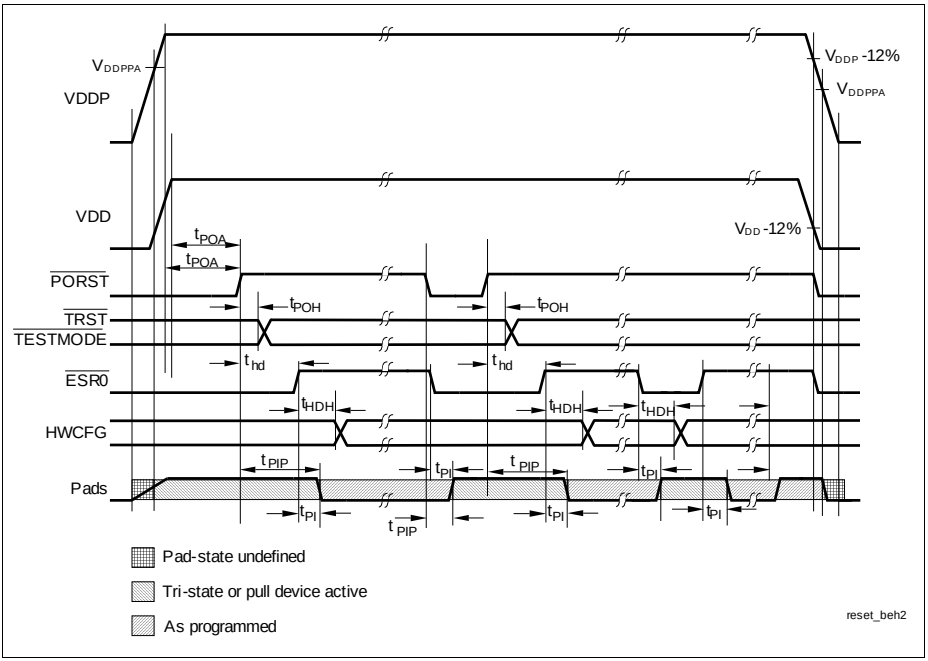


Figure 27 Power, Pad and Reset Timing

5.3.5 Phase Locked Loop (PLL)

Note: All PLL characteristics defined on this and the next page are not subject to production test, but verified by design characterization.

Table 19 PLL Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Accumulated jitter	$\|D_m\|$	–	–	7	ns	–
VCO frequency range	f_{VCO}	400	–	800	MHz	–
VCO input frequency range	f_{REF}	8	–	16	MHz	–
PLL base frequency[1)]	$f_{PLLBASE}$	50	200	320	MHz	–
PLL lock-in time	t_L	–	–	200	µs	–

1) The CPU base frequency with which the application software starts after PORST is calculated by dividing the limit values by 16 (this is the K2 factor after reset).

Phase Locked Loop Operation

When PLL operation is enabled and configured, the PLL clock f_{VCO} (and with it the LMB-Bus clock f_{LMB}) is constantly adjusted to the selected frequency. The PLL is constantly adjusting its output frequency to correspond to the input frequency (from crystal or clock source), resulting in an accumulated jitter that is limited. This means that the relative deviation for periods of more than one clock cycle is lower than for a single clock cycle.

This is especially important for bus cycles using waitstates and for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is negligible.

Two formulas are defined for the (absolute) approximate maximum value of jitter D_m in [ns] dependent on the K2 - factor, the LMB clock frequency f_{LMB} in [MHz], and the number m of consecutive f_{LMB} clock periods.

$$\text{for} \quad (K2 \le 100) \quad \text{and} \quad (m \le (f_{LMB}[MHz])/2)$$

$$|Dm[ns]| = \left(\frac{740}{K2 \times f_{LMB}[MHz]} + 5\right) \times \left(\frac{(1 - 0,01 \times K2) \times (m - 1)}{0,5 \times f_{LMB}[MHz] - 1} + 0,01 \times K2\right) \quad (2)$$

$$\text{else} \quad |Dm[ns]| = \frac{740}{K2 \times f_{LMB}[MHz]} + 5 \quad (3)$$

With rising number *m* of clock cycles the maximum jitter increases linearly up to a value of *m* that is defined by the K2-factor of the PLL. Beyond this value of *m* the maximum accumulated jitter remains at a constant value. Further, a lower LMB-Bus clock frequency f_{LMB} results in a higher absolute maximum jitter value.

Figure 28 gives the jitter curves for several K2 / f_{LMB} combinations.

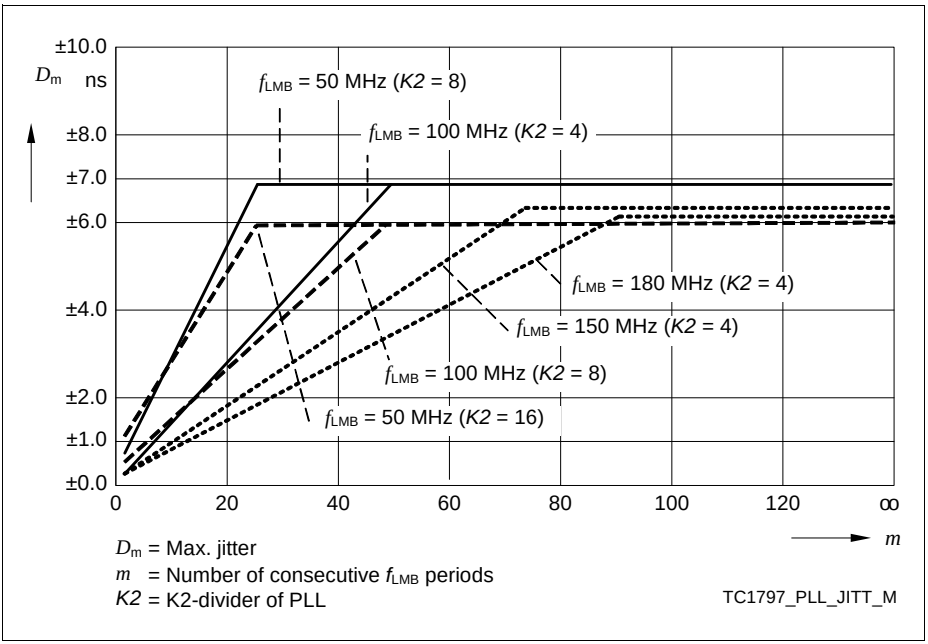


Figure 28 Approximated Maximum Accumulated PLL Jitter for Typical LMB-Bus Clock Frequencies f_{LMB}

Note: The specified PLL jitter values are valid if the capacitive load per output pin does not exceed C_L = 20 pF with the maximum driver and sharp edge, except the E-Ray output pins, which can be loaded with C_L = 25 pF. In case of applications with many pins with high loads, driver strengths and toggle rates the specified jitter values could be exceeded.

Note: The maximum peak-to-peak noise on the pad supply voltage, measured between V_{DDOSC3} at pin E26 and V_{SSOSC} at pin F25, is limited to a peak-to-peak voltage of V_{PP} = 100 mV for noise frequencies below 300 KHz and V_{PP} = 40 mV for noise frequencies above 300 KHz.
The maximum peak-to peak noise on the pad supply votage, measured between V_{DDOSC} at pin F26 and V_{SSOSC} at pin F25, is limited to a peak-to-peak voltage of V_{PP} = 100 mV for noise frequencies below 300 KHz and V_{PP} = 40 mV for noise

frequencies above 300 KHz.
These conditions can be achieved by appropriate blocking of the supply voltage as near as possible to the supply pins and using PCB supply and ground planes.

5.3.6 E-Ray Phase Locked Loop (E-Ray PLL)

Note: All PLL characteristics defined on this and the next page are not subject to production test, but verified by design characterization.

Table 20 PLL Parameters of the System PLL(Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Accumulated jitter at E_Ray module clock input[1]	$D_{P\_ERAY\_I}$	–	–	0.5	ns	–
Accumulated jitter at SYSCLK pin[2]	$D_{P\_ERAY\_E}$	–	–	0.8	ns	–
VCO frequency range	f_{VCO_ERAY}	400	–	500	MHz	–
VCO input frequency range	f_{REF_ERAY}	20	–	40	MHz	–
PLL base frequency[3]	$f_{PLLBASE\_ERAY}$	140	–	320	MHz	–
PLL lock-in time	t_{L_ERAY}	–	–	200	µs	–

1) Short term jitter and long term jitter for all numbers P of sample clocks (P ≥ 1), with f_{OSC} = 20MHz, K = 6, and f_{SAMPLE} = 80 MHz.

2) Short term jitter and long term jitter for all numbers P of sample clocks (P ≥ 1), with f_{OSC} = 20MHz, K = 6, and f_{SAMPLE} = 80 MHz.

3) The CPU base frequency which is selected after reset is calculated by dividing the limit values by 16 (this is the K factor after reset).

Note: The specified PLL jitter values are valid if the capacitive load per output pin does not exceed C_L = 20 pF with the maximum driver and sharp edge, except the E-Ray output pins, which can be loaded with C_L = 25 pF. In case of applications with many pins with high loads, driver strengths and toggle rates the specified jitter values could be exceeded.

Note: The maximum peak-to-peak noise on the pad supply voltage, measured between V_{DDPF3} at pin G24 and V_{SSOSC} at pin F25, is limited to a peak-to-peak voltage of V_{PP} = 100 mV for noise frequencies below 300 KHz and V_{PP} = 40 mV for noise frequencies above 300 KHz.

The maximum peak-to peak noise on the pad supply voltage, measured between V_{DDPF} at pin G23 and V_{SSOSC} at pin F25, is limited to a peak-to-peak voltage of V_{PP} = 100 mV for noise frequencies below 300 KHz and V_{PP} = 40 mV for noise frequencies above 300 KHz.

These conditions can be achieved by appropriate blocking of the supply voltage as near as possible to the supply pins and using PCB supply and ground planes.

5.3.7 BFCLKO Output Clock Timing

V_{SS} = 0 V;V_{DD} = 1.5 V ± 5%; V_{DDEBU} = 2.5 V ± 5% and 3.3 V ± 5%,;
T_A = -40 °C to +125 °C; C_L = 35 pF

Table 21 BFCLK0 Output Clock Timing Parameters[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
BFCLKO clock period	t_{BFCLKO} CC	13.33[2)]	–	–	ns	–
BFCLKO high time	t_5 CC	3	–	–	ns	–
BFCLKO low time	t_6 CC	3	–	–	ns	–
BFCLKO rise time	t_7 CC	–	–	3	ns	–
BFCLKO fall time	t_8 CC	–	–	3	ns	–
BFCLKO duty cycle $t_5/(t_5 + t_6)$[3)]	DC	45	50	55	%	–

1) Not subject to production test, verified by design/characterization.

2) The PLL jitter characteristics add to this value according to the application settings. See the PLL jitter parameters.

3) The PLL jitter is not included in this parameter. If the BFCLKO frequency is equal to f_{CPU}, the K divider has to be regarded.

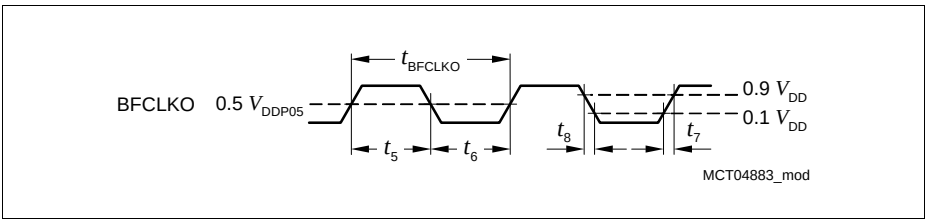


Figure 29 BFCLKO Output Clock Timing

5.3.8 JTAG Interface Timing

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Table 22 JTAG Interface Timing Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK clock period	t_1 SR	25	–	–	ns	–
TCK high time	t_2 SR	12	–	–	ns	–
TCK low time	t_3 SR	10	–	–	ns	–
TCK clock rise time	t_4 SR	–	–	4	ns	–
TCK clock fall time	t_5 SR	–	–	4	ns	–
TDI/TMS setup to TCK rising edge	t_6 SR	6	–	–	ns	–
TDI/TMS hold after TCK rising edge	t_7 SR	6	–	–	ns	–
TDO valid after TCK falling edge[1] (propagation delay)	t_8 CC	–	–	13	ns	C_L = 50 pF
	t_8 CC	–	–	3	ns	C_L = 20 pF
TDO hold after TCK falling edge[1]	t_{18} CC	2	–	–	ns	
TDO high imped. to valid from TCK falling edge[1)2)]	t_9 CC	–	–	14	ns	C_L = 50 pF
TDO valid to high imped. from TCK falling edge[1]	t_{10} CC	–	–	13.5	ns	C_L = 50 pF

1) The falling edge on TCK is used to generate the TDO timing.

2) The setup time for TDO is given implicitly by the TCK cycle time.

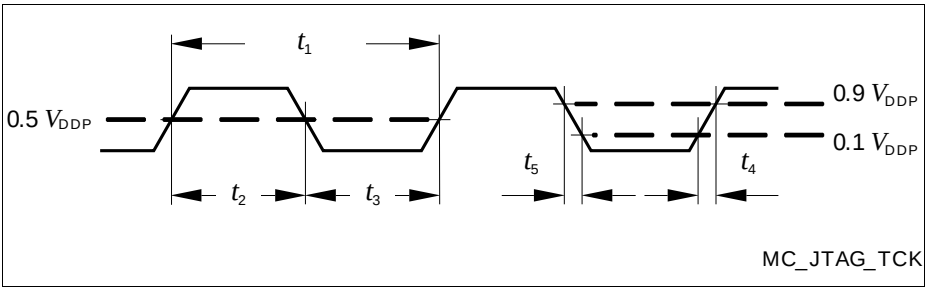


Figure 30 Test Clock Timing (TCK)

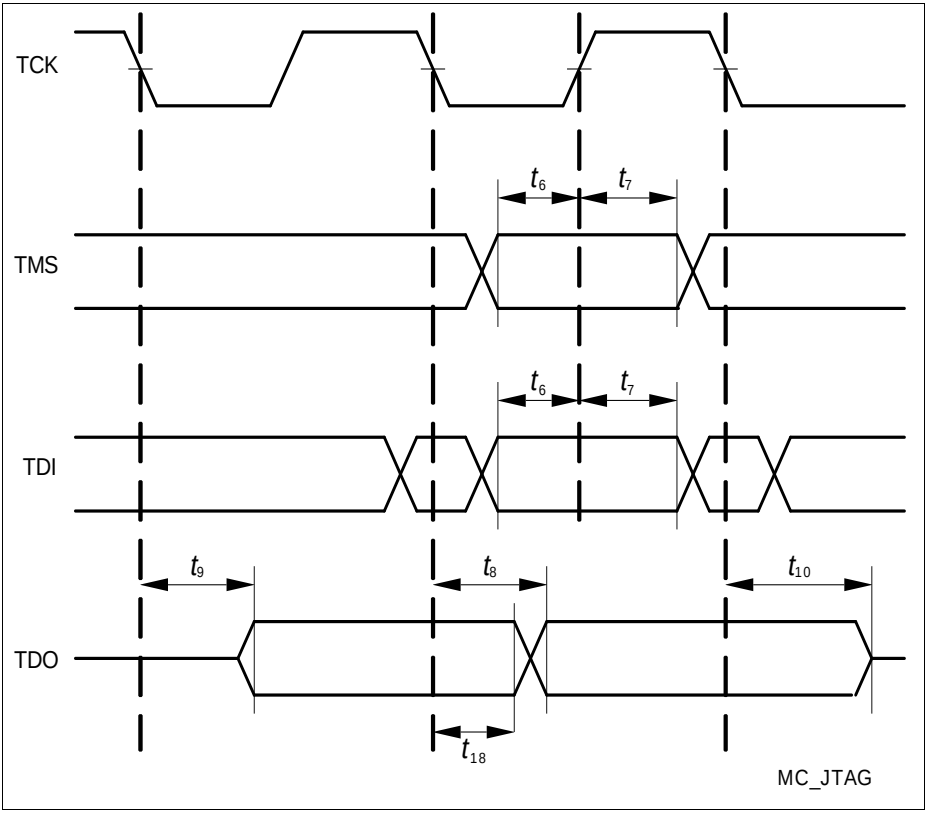


Figure 31 JTAG Timing

5.3.9 DAP Interface Timing

The following parameters are applicable for communication through the DAP debug interface.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Table 23 DAP Interface Timing Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAP0 clock period	t_{11} SR	12.5	–	–	ns	–
DAP0 high time	t_{12} SR	4	–	–	ns	–
DAP0 low time	t_{13} SR	4	–	–	ns	–
DAP0 clock rise time	t_{14} SR	–	–	2	ns	–
DAP0 clock fall time	t_{15} SR	–	–	2	ns	–
DAP1 setup to DAP0 rising edge	t_{16} SR	6	–	–	ns	–
DAP1 hold after DAP0 rising edge	t_{17} SR	6	–	–	ns	–
DAP1 valid per DAP0 clock period[1)]	t_{19} SR	8	–	–	ns	80 MHz, C_L = 20 pF
	t_{19} SR	10	–	–	ns	40 MHz, C_L = 50 pF

1) The Host has to find a suitable sampling point by analyzing the sync telegram response.

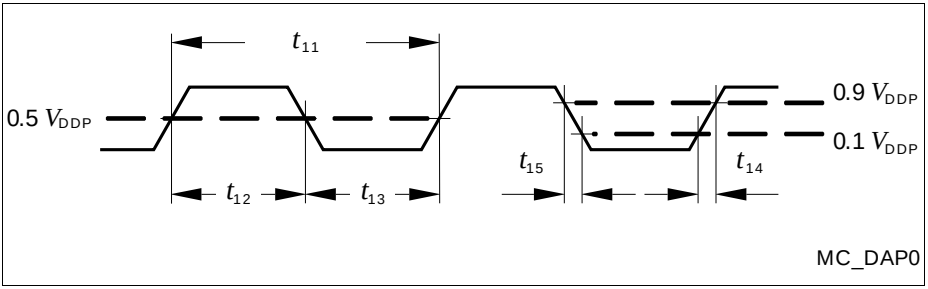


Figure 32 Test Clock Timing (DAP0)

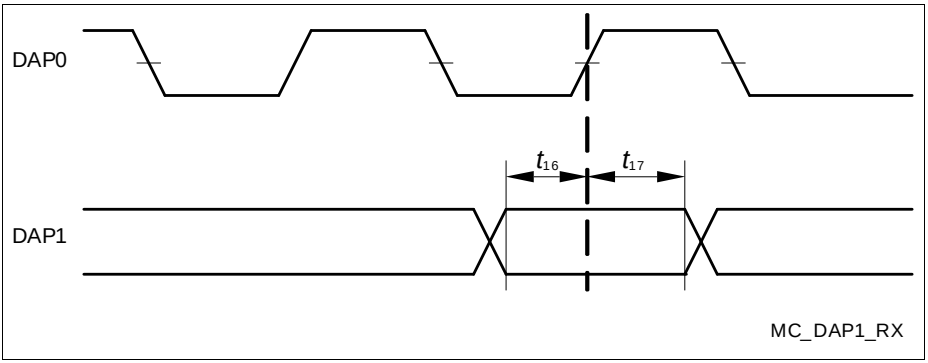


Figure 33 DAP Timing Host to Device

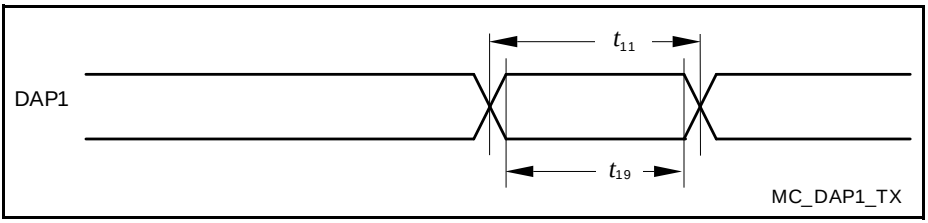


Figure 34 DAP Timing Device to Host

5.3.10 EBU Timings

V_{SS} = 0 V;V_{DD} = 1.5 V ± 5%; V_{DDEBU} = 2.5 V ± 5% and 3.3 V ± 5%, Class B pins;
T_A = -40 °C to +125 °C; C_L = 35 pF for address/data; C_L = 40pF for the control lines.

5.3.10.1 EBU Asynchronous Timings

For each timing, the accumulated PLL jitter of the programed duration in number of clock periods must be added separately. Operating conditions apply and C_L = 35 pF.

Table 24 Common timing parameters for all asynchronous timings[1)]

Parameter		Symbol		Limit Values		Unit	Edge Setting
				min	max		
Pulse width deviation from the ideal programmed width due to the A2 pad asymmetry, strong driver mode, rise delay - fall delay. C_L = 35 pF.		t_a	CC	-1	1.5	ns	sharp
				-2	1		medium
AD(31:0) output delay	to $\overline{ADV}$ rising edge, multiplexed read / write	t_{13}	CC	-5.5	2		–
AD(31:0) output delay		t_{14}	CC	-5.5	2		–

1) Not subject to production test, verified by design/characterization.

Read Timings

Table 25 Asynchronous read timings, multiplexed and demultiplexed[1)]

Parameter		Symbol		Limit Values		Unit
				min	max	
A(23:0) output delay	to $\overline{RD}$ rising edge, deviation from the ideal programmed value.	t_0	CC	-2.5	2.5	ns
A(23:0) output delay		t_1	CC	-2.5	2.5	
$\overline{CS}$ rising edge		t_2	CC	-2	2.5	
$\overline{ADV}$ rising edge		t_3	CC	-1.5	4.5	
$\overline{BC}$ rising edge		t_4	CC	-2.5	2.5	
$\overline{WAIT}$ input setup		t_5	SR	12	–	
$\overline{WAIT}$ input hold		t_6	SR	0	–	
Data input setup		t_7	SR	12	–	
Data input hold		t_8	SR	0	–	
MR / $\overline{W}$ output delay		t_9	CC	-2.5	1.5	

1) Not subject to production test, verified by design/characterization.

Multiplexed Read Timing

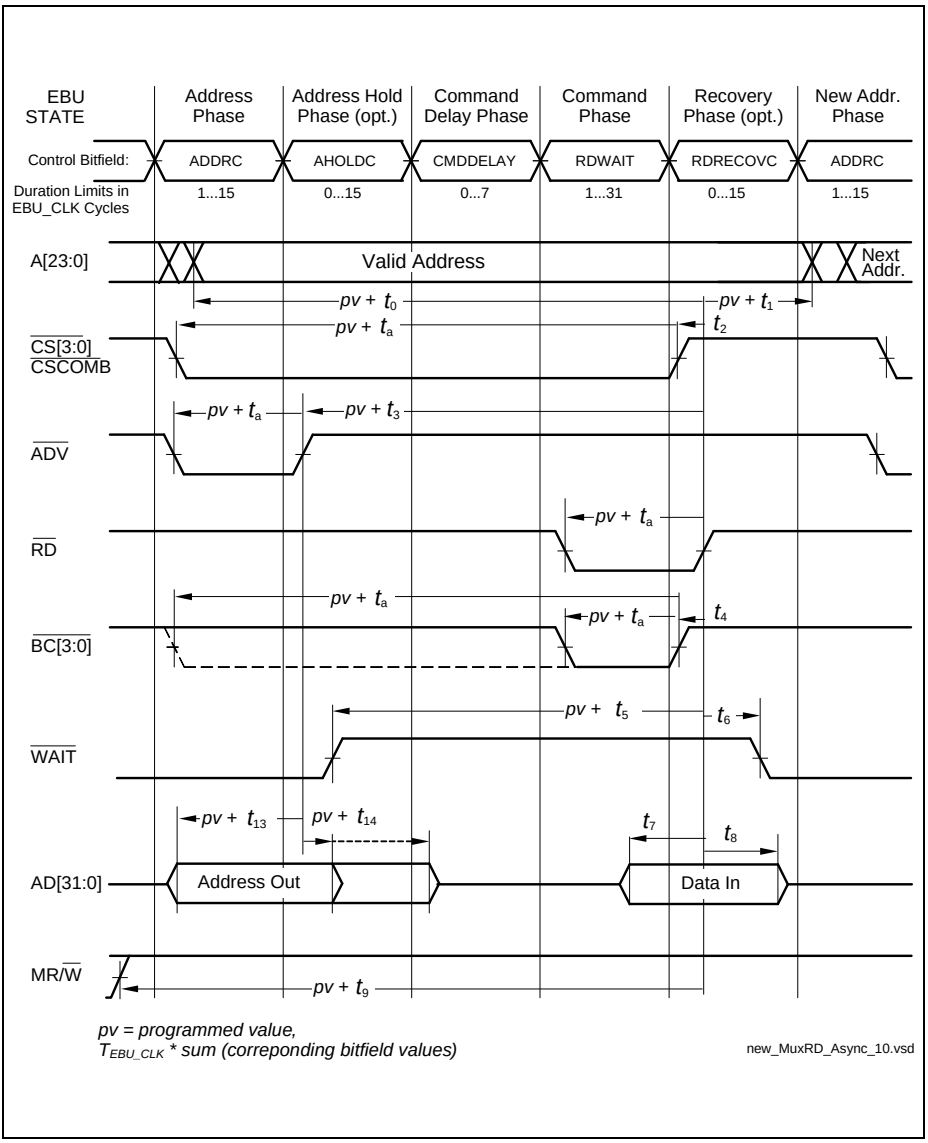


Figure 35 Multiplexed Read Access

Demultiplexed Read Timing

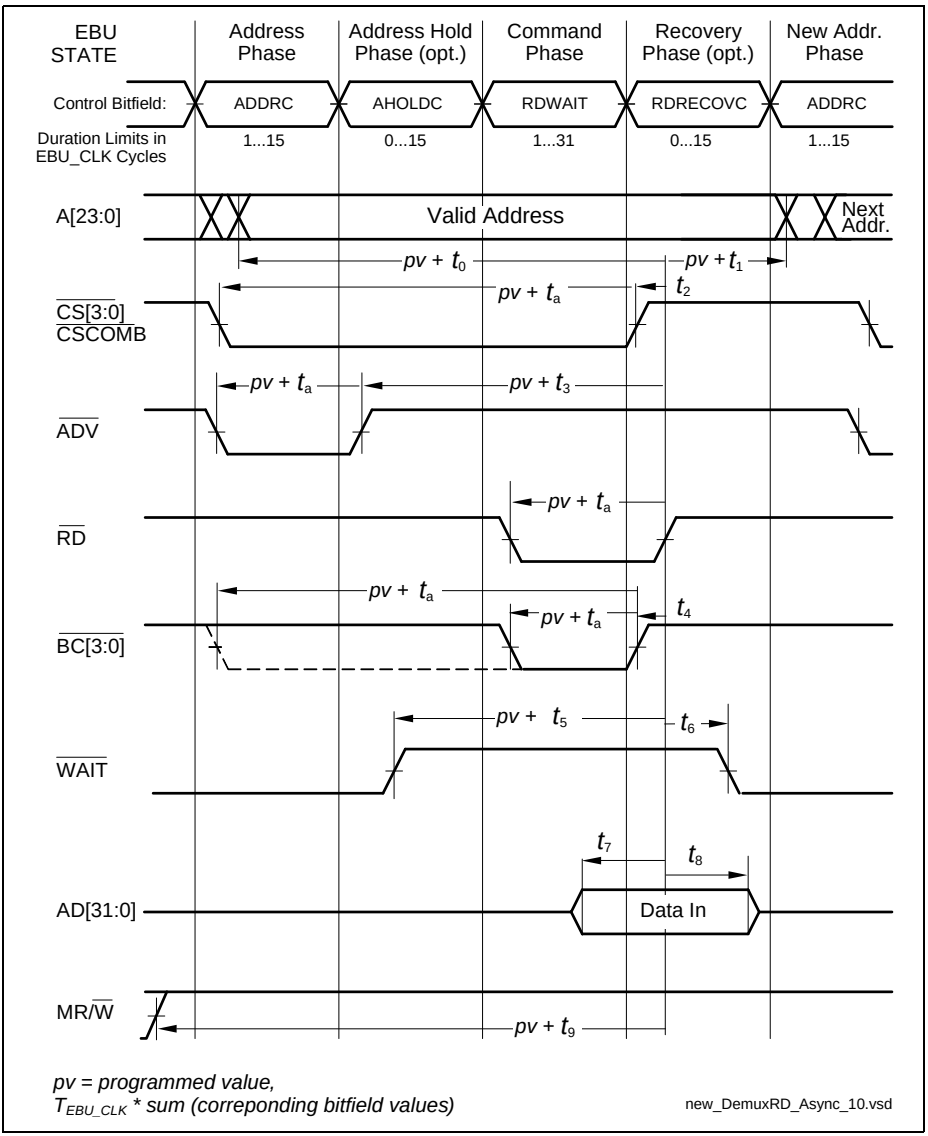


Figure 36 Demultiplexed Read Access

Write Timings

Table 26 Asynchronous write timings, multiplexed and demultiplexed[1)]

Parameter		Symbol		Limit Values		Unit
				min	max	
A(23:0) output delay	to RD/$\overline{WR}$ rising edge, deviation from the ideal programmed value.	t_{30}	CC	-2.5	2.5	ns
A(23:0) output delay		t_{31}	CC	-2.5	2.5	
$\overline{CS}$ rising edge		t_{32}	CC	-2	2	
$\overline{ADV}$ rising edge		t_{33}	CC	-2	4.5	
$\overline{BC}$ rising edge		t_{34}	CC	-2.5	2	
$\overline{WAIT}$ input setup		t_{35}	SR	12	–	
$\overline{WAIT}$ input hold		t_{36}	SR	0	–	
Data output delay		t_{37}	CC	-5.5	2	
Data output delay		t_{38}	CC	-5.5	2	
MR / $\overline{W}$ output delay		t_{39}	CC	-2.5	1.5	

1) Not subject to production test, verified by design/characterization.

Multiplexed Write Timing

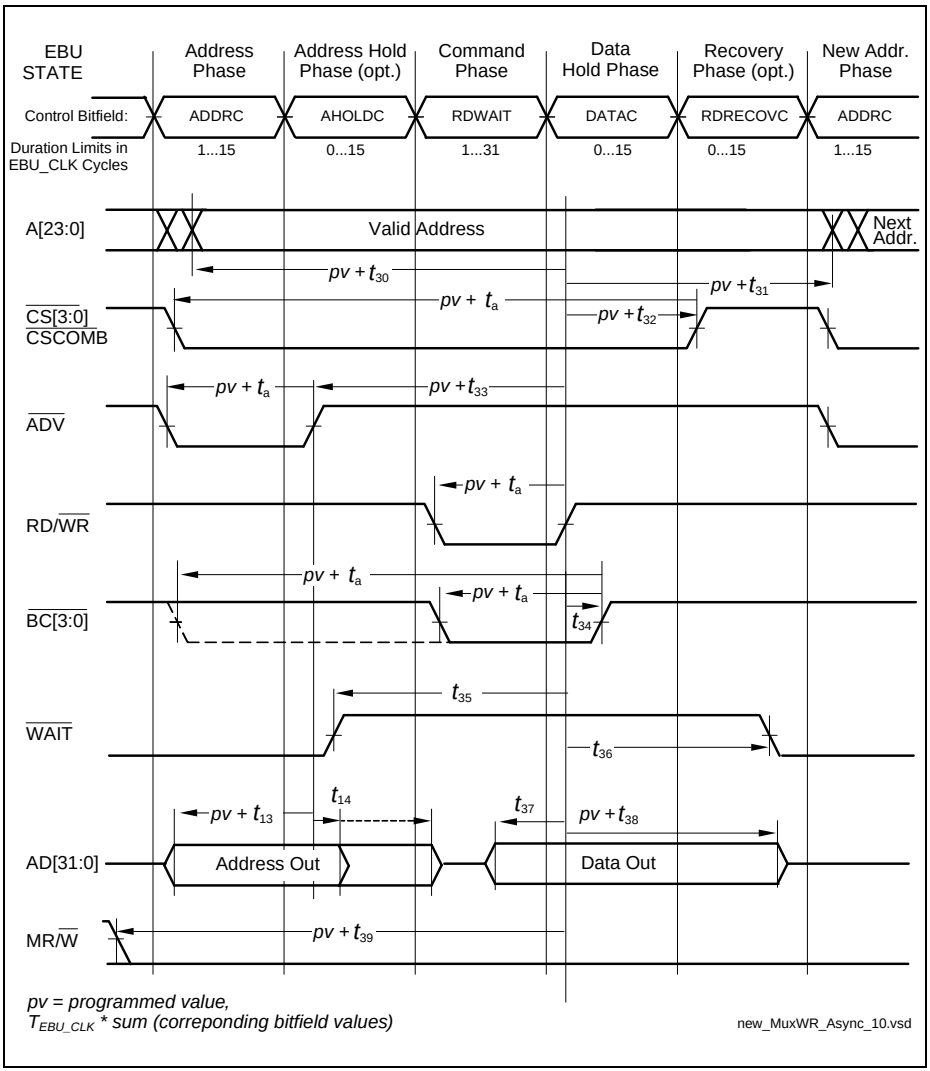


Figure 37 Multiplexed Write Access

Demultiplexed Write Timing

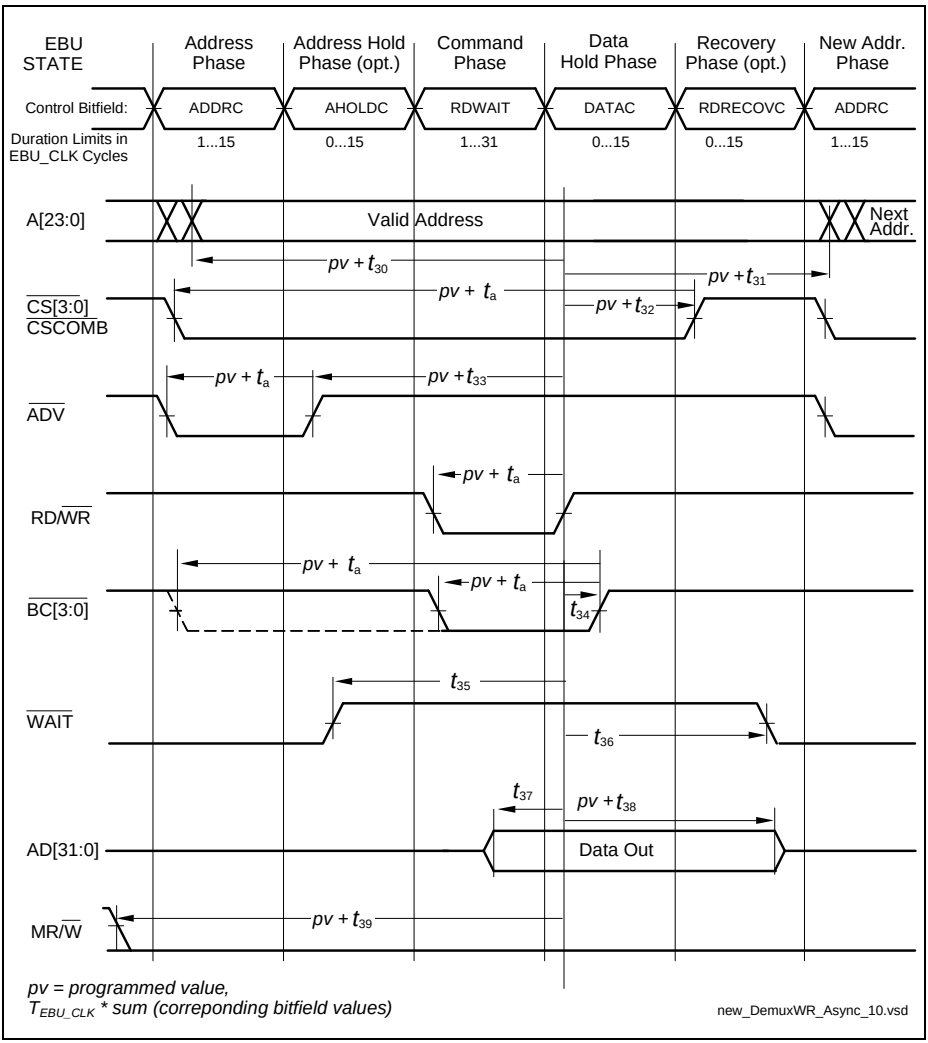


Figure 38 Demultiplexed Write Access

5.3.10.2 EBU Burst Mode Access Timing

V_{SS} = 0 V;V_{DD} = 1.5 V ± 5%; V_{DDEBU} = 2.5 V ± 5% and 3.3 V ± 5%, Class B pins;
T_A = -40 °C to +125 °C; C_L = 35 pF;

Table 27 EBU Burst Mode Read / Write Access Timing Parameters[1)]

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Output delay from BFCLKO active edge[2)]	t_{10}	CC	-2	–	2	ns	–
$\overline{RD}$ and RD/$\overline{WR}$ active/inactive after BFCLKO active edge[3)]	t_{12}	CC	-2	–	2	ns	–
$\overline{CS}$x output delay from BFCLKO active edge[3)]	t_{21}	CC	-2.5	–	1.5	ns	–
$\overline{ADV}$ active/inactive after BFCLKO active edge[4)]	t_{22}	CC	-2	–	2	ns	–
$\overline{BAA}$ active/inactive after BFCLKO active edge[4)]	t_{22a}	CC	-2.5	–	1.5	ns	–
Data setup to BFCLKI rising edge[5)]	t_{23}	SR	3	–	–	ns	–
Data hold from BFCLKI rising edge[5)]	t_{24}	SR	0	–	–	ns	–
$\overline{WAIT}$ setup (low or high) to BFCLKI rising edge[5)]	t_{25}	SR	3	–	–	ns	–
$\overline{WAIT}$ hold (low or high) from BFCLKI rising edge[5)]	t_{26}	SR	0	–	–	ns	–

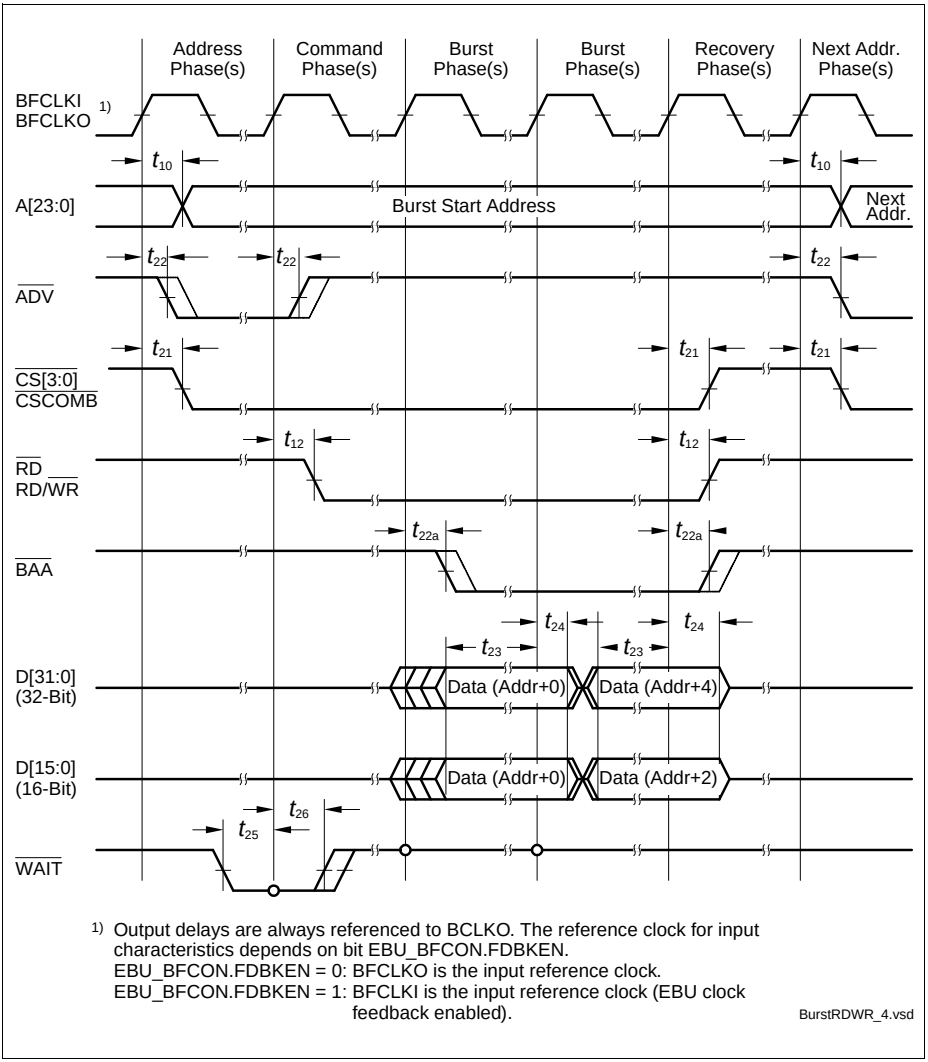
1) Not subject to production test, verified by design/characterization.

2) This is a default parameter which are applicable to all timings which are not explicitly covered by the other parameters.

3) An active edge can be rising or falling edge, depending on the settings of bits BFCON.EBSE / ECSE and clock divider ratio.
Negative minimum values for these parameters mean that the last data read during a burst may be corrupted. However, with clock feedback enabled, this value is oversampling not required for the LMB transaction and will be discarded.

4) This parameter is valid for BUSCONx.EBSE = 1 and BUSAPx.EXTCLK = 00_B.
For BUSCONx.EBSE = 1 and other values of BUSAPx.EXTCLK, ADV and BAA will be delayed by 1 / 2 of the LMB bus clock period $T_{CPU} = 1 / f_{CPU}$.
For BUSCONx. EBSE = 0 and BUSAPx.EXTCLK = 11_B, add 2 LMB clock periods.
For BUSCONx. EBSE = 0 and other values of BUSAPx.EXTCLK add 1 LMB clock period.

5) If the clock feedback is not enabled, the input signals are latched using the internal clock in the same way as at asynchronous access. So t5, t6, t7 and t8 from the asynchronous timings apply.



1) Output delays are always referenced to BCLKO. The reference clock for input characteristics depends on bit EBU_BFCON.FDBKEN.
EBU_BFCON.FDBKEN = 0: BFCLKO is the input reference clock.
EBU_BFCON.FDBKEN = 1: BFCLKI is the input reference clock (EBU clock feedback enabled).

BurstRDWR_4.vsd

Figure 39 EBU Burst Mode Read / Write Access Timing

5.3.10.3 EBU Arbitration Signal Timing

V_{SS} = 0 V;V_{DD} = 1.5 V ± 5%; V_{DDEBU} = 2.5 V ± 5% and 3.3 V ± 5%, Class B pins;
T_A = -40°C to +125 °C; C_L = 35 pF;

Table 28 EBU Arbitration Signal Timing Parameters[1)]

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Output delay from BFCLKO rising edge	t_{27}	CC	–	–	3	ns	–
Data setup to BFCLKO falling edge	t_{28}	SR	11	–	–	ns	–
Data hold from BFCLKO falling edge	t_{29}	SR	2	–	–	ns	–

1) Not subject to production test, verified by design/characterization.

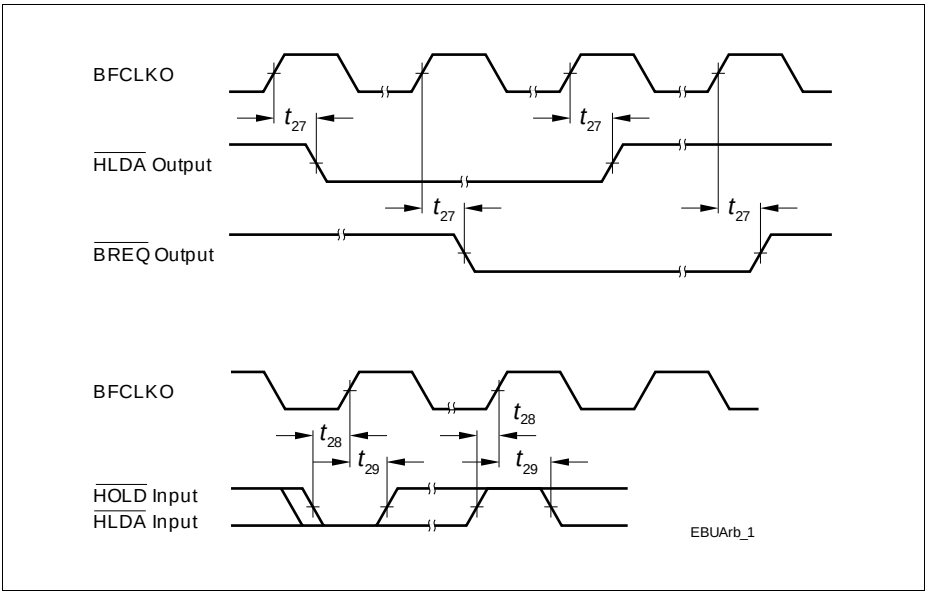


Figure 40 EBU Arbitration Signal Timing

5.3.11 Peripheral Timings

Note: Peripheral timing parameters are not subject to production test. They are verified by design/characterization.

5.3.11.1 Micro Link Interface (MLI) Timing

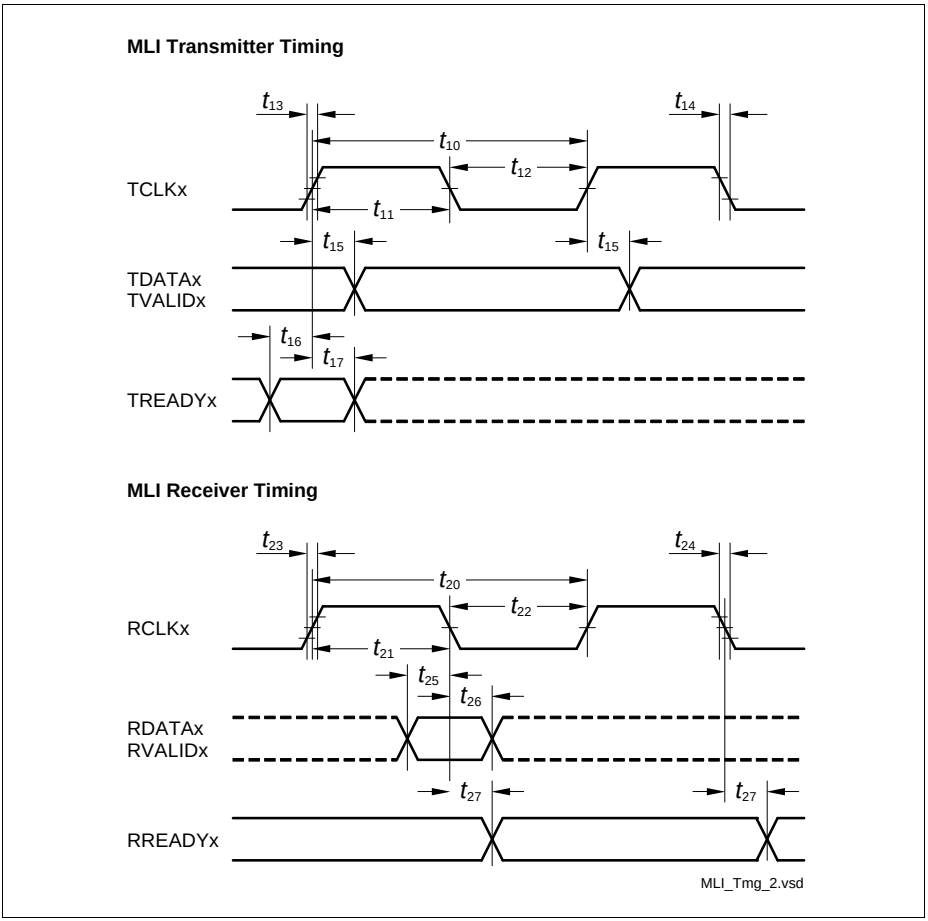


Figure 41 MLI Interface Timing

Note: The generation of RREADYx is in the input clock domain of the receiver. The reception of TREADYx is asynchronous to TCLKx.

Table 29 MLI Timings (Operating Conditions apply), C_L = 50 pF

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
MLI Transmitter Timing							
TCLK clock period	t_{10}	CC	$2 \times T_{MLI}$	–	–	ns	1)
TCLK high time	t_{11}	CC	$0.45 \times t_{10}$	$0.5 \times t_{10}$	$0.55 \times t_{10}$	ns	2)3)
TCLK low time	t_{12}	CC	$0.45 \times t_{10}$	$0.5 \times t_{10}$	$0.55 \times t_{10}$	ns	2)3)
TCLK rise time	t_{13}	CC	–	–	4)	ns	–
TCLK fall time	t_{14}	CC	–	–	4)	ns	–
TDATA/TVALID output delay time	t_{15}	CC	-3	–	4.4	ns	–
TREADY setup time to TCLK rising edge	t_{16}	SR	18	–	–	ns	–
TREADY hold time from TCLK rising edge	t_{17}	SR	0	–	–	ns	–
MLI Receiver Timing							
RCLK clock period	t_{20}	SR	$1 \times T_{MLI}$	–	–	ns	1)
RCLK high time	t_{21}	SR	–	$0.5 \times t_{20}$	–	ns	5)6)
RCLK low time	t_{22}	SR	–	$0.5 \times t20$	–	ns	5)6)
RCLK rise time	$t23R$	S	–	–	4	ns	7)
RCLK fall time	$t24R$	S	–	–	4	ns	7)
RDATA/RVALID setup time to RCLK falling edge	$t25R$	S	4.2	–	–	ns	–
RDATA/RVALID hold time from RCLK rising edge	$t26R$	S	2.2	–	–	ns	–
RREADY output delay time	$t27C$	C	0	–	16	ns	–

1) $T_{MLImin.} = T_{SYS} = 1/f_{SYS}$. When f_{SYS} = 90 MHz, t_{10} = 22.22 ns and t_{20} = 11.11 ns.

2) The following formula is valid: $t_{11} + t_{12} = t_{10}$

3) The min./max. TCLK low/high times t_{11}/t_{12} include the PLL jitter of f_{SYS}. Fractional divider settings must be regarded additionally to t_{11} / t_{12}.
4) For high-speed MLI interface, strong driver sharp or medium edge selection (class A2 pad) is recommended for TCLK.
5) The following formula is valid: $t_{21} + t_{22} = t_{20}$
6) The min. and max. value of is parameter can be adjusted by considering the other receiver timing parameters.
7) The RCLK max. input rise/fall times are best case parameters for f_{SYS} = 90 MHz. For reduction of EMI, slower input signal rise/fall times can be used for longer RCLK clock periods.

5.3.11.2 Micro Second Channel (MSC) Interface Timing

Table 30 MSC Interface Timing (Operating Conditions apply), C_L = 50 pF

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
FCLP clock period[1)2)]	t_{40}	CC	2 × T_{MSC}[3)]	–	–	ns	–
SOP/ENx outputs delay from FCLP rising edge	t_{45}	CC	-10		10	ns	–
SDI bit time	t_{46}	CC	8 × T_{MSC}		–	ns	–
SDI rise time	t_{48}	SR			100	ns	–
SDI fall time	t_{49}	SR			100	ns	–

1) FCLP signal rise/fall times are the same as the A2 Pads rise/fall times.

2) FCLP signal high and low can be minimum 1 × T_{MSC}.

3) T_{MSCmin} = T_{SYS} = 1 / f_{SYS}. When f_{SYS} = 90 MHz, t_{40} = 22,2ns

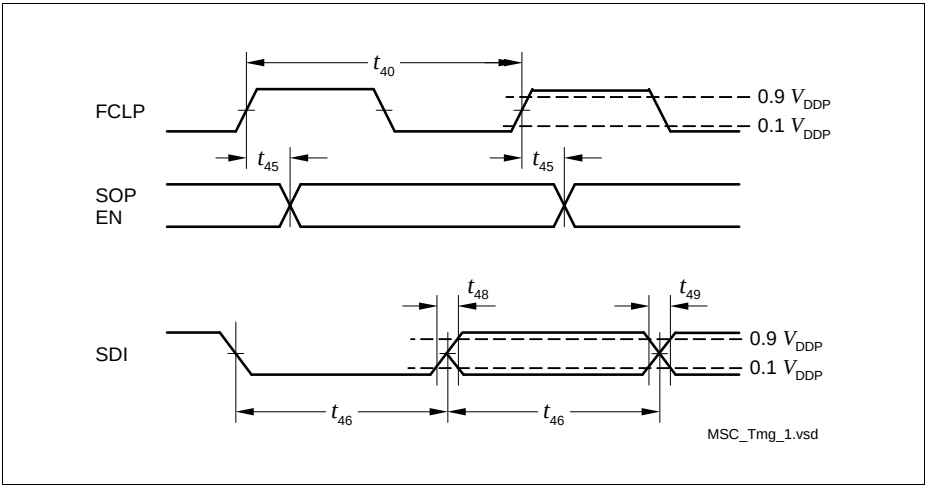


Figure 42 MSC Interface Timing

Note: The data at SOP should be sampled with the falling edge of FCLP in the target device.

5.3.11.3 SSC Master/Slave Mode Timing

Table 31 SSC Master/Slave Mode Timing
(Operating Conditions apply), C_L = 50 pF

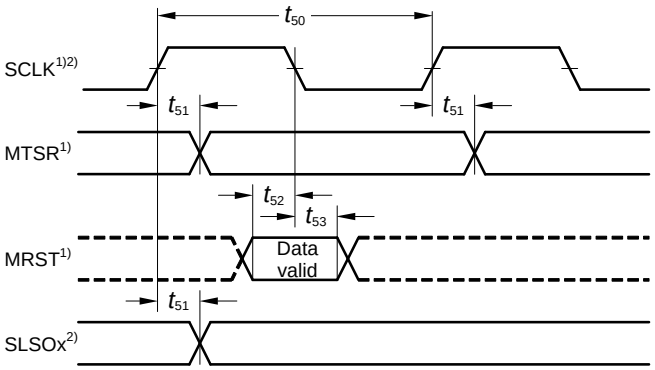
Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Master Mode Timing							
SCLK clock period	t_{50}	CC	$2 \times T_{SSC}$	–	–	ns	1)2)3)
MTSR/SLSOx delay from SCLK rising edge	t_{51}	CC	0	–	8	ns	–
MRST setup to SCLK falling edge	t_{52}	SR	13	–	–	ns	3)
MRST hold from SCLK falling edge	t_{53}	SR	0	–	–	ns	3)
Slave Mode Timing							
SCLK clock period	t_{54}	SR	$4 \times T_{SSC}$	–	–	ns	1)3)
SCLK duty cycle	t_{55}/t_{54}	SR	45	–	55	%	–
MTSR setup to SCLK latching edge	t_{56}	SR	$T_{SSC} + 5$	–	–	ns	3)4)
MTSR hold from SCLK latching edge	t_{57}	SR	$T_{SSC} + 5$	–	–	ns	3)4)
SLSI setup to first SCLK shift edge	t_{58}	SR	$T_{SSC} + 5$	–	–	ns	3)
SLSI hold from last SCLK latching edge	t_{59}	SR	7	–	–	ns	–
MRST delay from SCLK shift edge	t_{60}	CC	0	–	15	ns	–
SLSI to valid data on MRST	t_{61}	CC	–	–	12	ns	–

1) SCLK signal rise/fall times are the same as the A2 Pads rise/fall times.

2) SCLK signal high and low times can be minimum $1 \times T_{SSC}$.

3) $T_{SSCmin} = T_{SYS} = 1/f_{SYS}$. When f_{SYS} = 90 MHz, t_{50} = 22.2 ns.

4) Fractional divider switched off, SSC internal baud rate generation used.

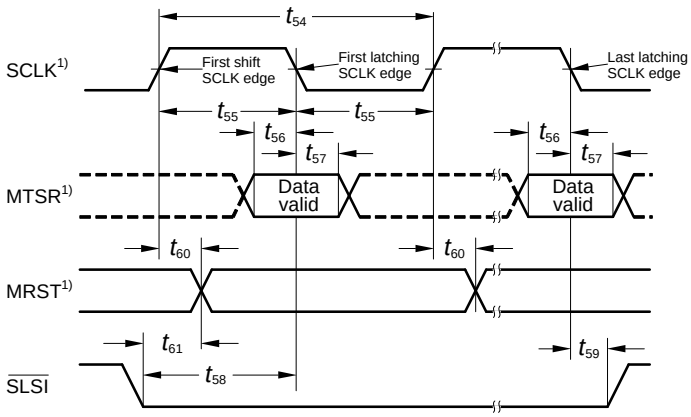


1) This timing is based on the following setup: CON.PH = CON.PO = 0.

2) The transition at SLSOx is based on the following setup: SSOTC.TRAIL = 0 and the first SCLK high pulse is in the first one of a transmission.

SSC_TmgMM

Figure 43 SSC Master Mode Timing



1) This timing is based on the following setup: CON.PH = CON.PO = 0.

SSC_TmgSM

Figure 44 SSC Slave Mode Timing

5.3.11.4 E-Ray Interface Timing

The timings in this section are valid for the strong / sharp and strong / medium settings of the output drivers, and for both A1 or A2 input pads. The timing parameters are not subject to production test, but verified by design / characterization.

Table 32 E-Ray Interface Timing (Operating Conditions apply)**, C_L = 25 pF**

Parameter	Symbol		Limit Values			Unit	Notes Conditions
			Min.	Typ.	Max.		
TxDA / TxDB Signal Timing at end of frame							
Time span from last BSS to FES without the influence of quartz tolerances d10Bit_Tx [1]	t_{60}	CC	997.75	–	1002.25	ns	f_{oscdd} = 20MHz; f_{oscdd} = 40MHz; C_L = 25 pF (TxDA, TXDB)
TxD data valid, from f_{sample} flip-flop txd_reg ⇒ TxDA, TxDB, (dTxAsym) [2] [3]	$\lvert t_{61} - t_{62} \rvert$	CC	–	–	1.5	ns	Asymmetrical delay of rising and falling edge (TxDA, TxDB)
RxDA / RxDB Signal Timing at end of frame							
Time span between last BSS and FES that is properly decoded, without influence of quartz tolerances d10Bit_Rx [1] [4] [5]	t_{63}	SR	966	–	1046.1	ns	f_{oscdd} = 20MHz; f_{oscdd} = 40MHz; C_L = 25 pF (TxDA, TXDB)
RxD capture by f_{sample}, RxDA / RxDB ⇒ sampling flip-flop, (dRxAsym) [5]	$\lvert t_{64} - t_{65} \rvert$	CC	–	–	3.0	ns	Asymmetrical delay of rising and falling edge (RxDA, RxDB)

1) PLL jitter included.

2) Refers to delays caused by the asymmetries of the output drivers of the digital logic and the GPIO pad drivers. Quartz tolerance and PLL jitter are not included.

3) E-Ray TxD output drivers have an asymmetry of rising and falling edges of $|t_F - t_R| \leq 1$ ns.

4) Limits of 966.5 ns and 1046 ns correspond to (30%, 70%) × V_{DDP} FlexRay standard input thresholds. Due to different input thresholds of the TC1797, a correcton of -0.5 ns and +0.1 ns has been applied.

5) Valid for output slopes of the Bus Driver of dRxSlope ≤ 5 ns, 20% × V_{DDP} to 80% × V_{DDP}, according to the FlexRay Electrical Physical Layer Specification V2.1 B. For A1 pads, the rise and fall times of the incoming signal have to satisfy the following inequality: $-1.6 \text{ ns} \leq t_F - t_R \leq 1.3 \text{ ns}$.

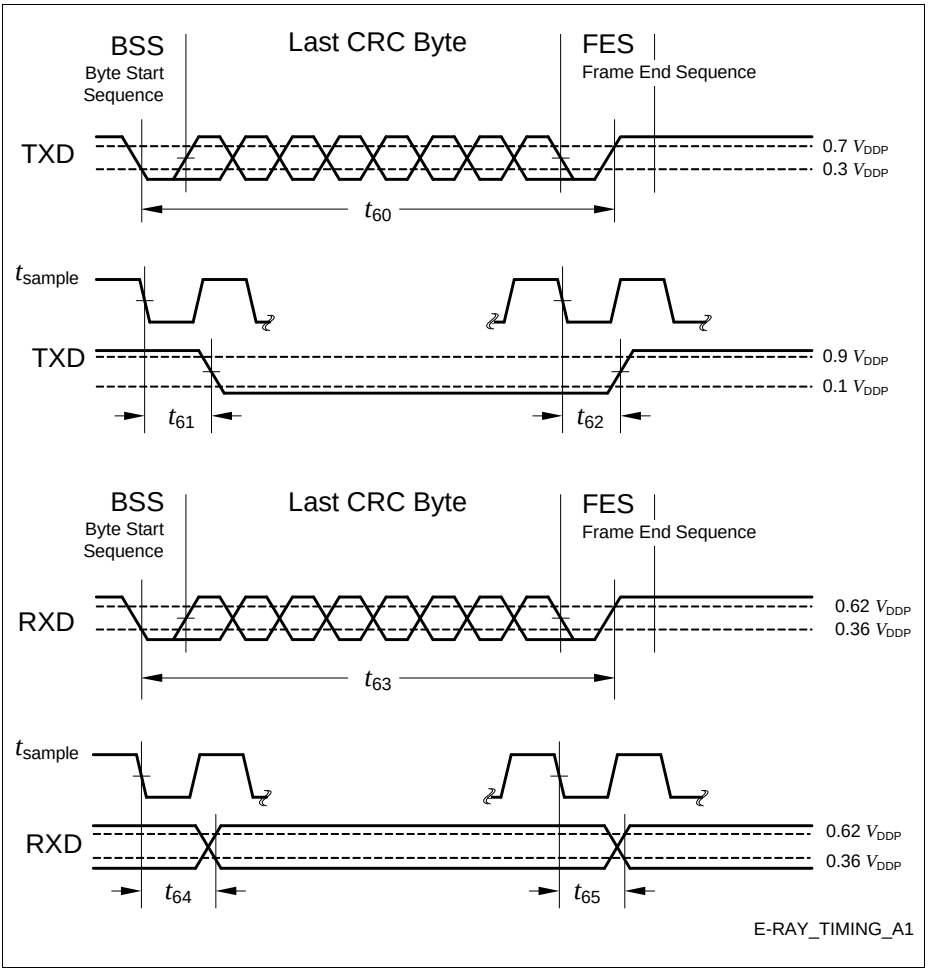


Figure 45 E-Ray Timing

5.4 Package and Reliability

5.4.1 Package Parameters

Table 33 Thermal Characteristics of the Package

Device	Package	RΘJCT[1)]	RΘJCB[1)]	Unit	Note
TC1797	P/PG-BGA-416-10 / P/PG-BGA-416-27	4	6	K/W	

1) The top and bottom thermal resistances between the case and the ambient (R_{TCAT}, R_{TCAB}) are to be combined with the thermal resistances between the junction and the case given above (R_{TJCT}, R_{TJCB}), in order to calculate the total thermal resistance between the junction and the ambient (R_{TJA}). The thermal resistances between the case and the ambient (R_{TCAT}, R_{TCAB}) depend on the external system (PCB, case) characteristics, and are under user responsibility.
The junction temperature can be calculated using the following equation: $T_J = T_A + R_{TJA} \times P_D$, where the R_{TJA} is the total thermal resistance between the junction and the ambient. This total junction ambient resistance R_{TJA} can be obtained from the upper four partial thermal resistances.
Thermal resistances as measured by the ‘cold plate method’ (MIL SPEC-883 Method 1012.1).

5.4.2 Package Outline

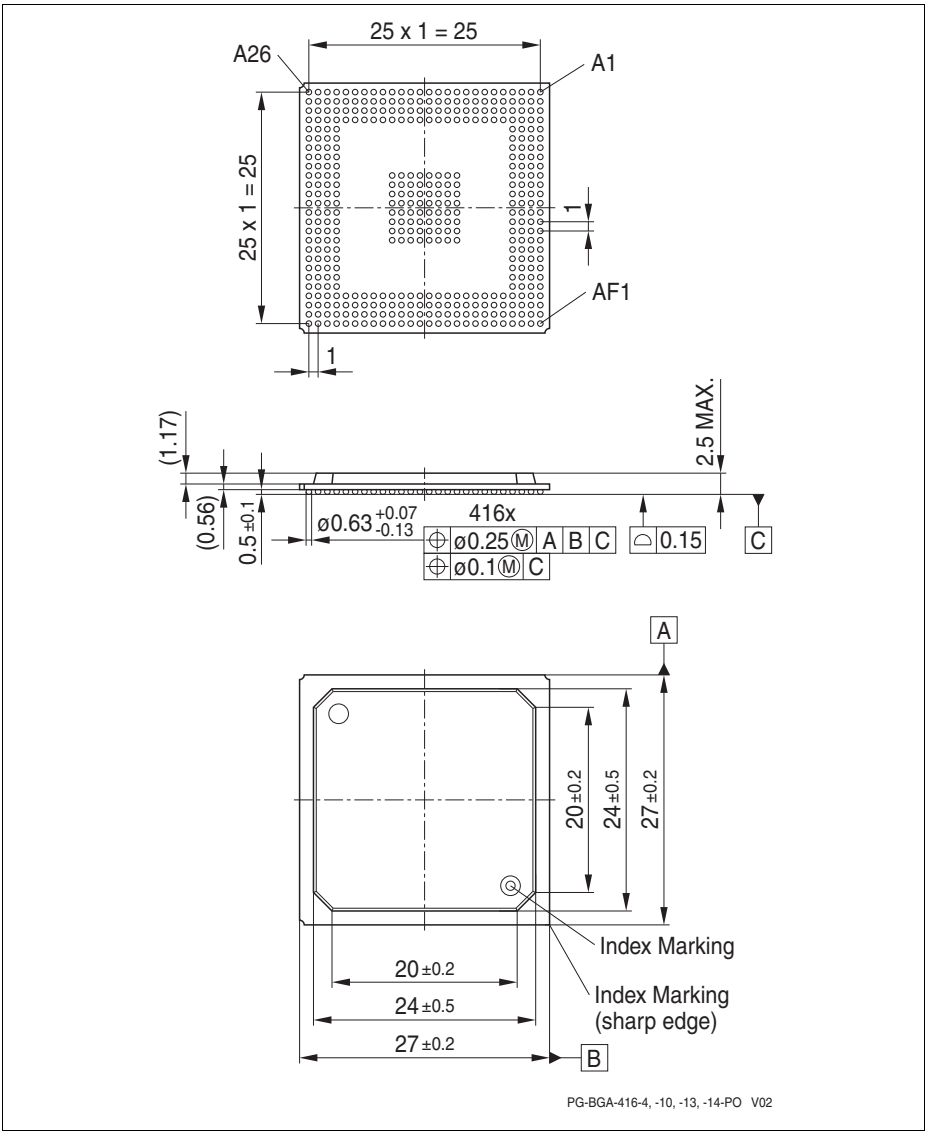


Figure 46 Package Outlines P/PG-BGA-416-10, Plastic (Green) Ball Grid Array

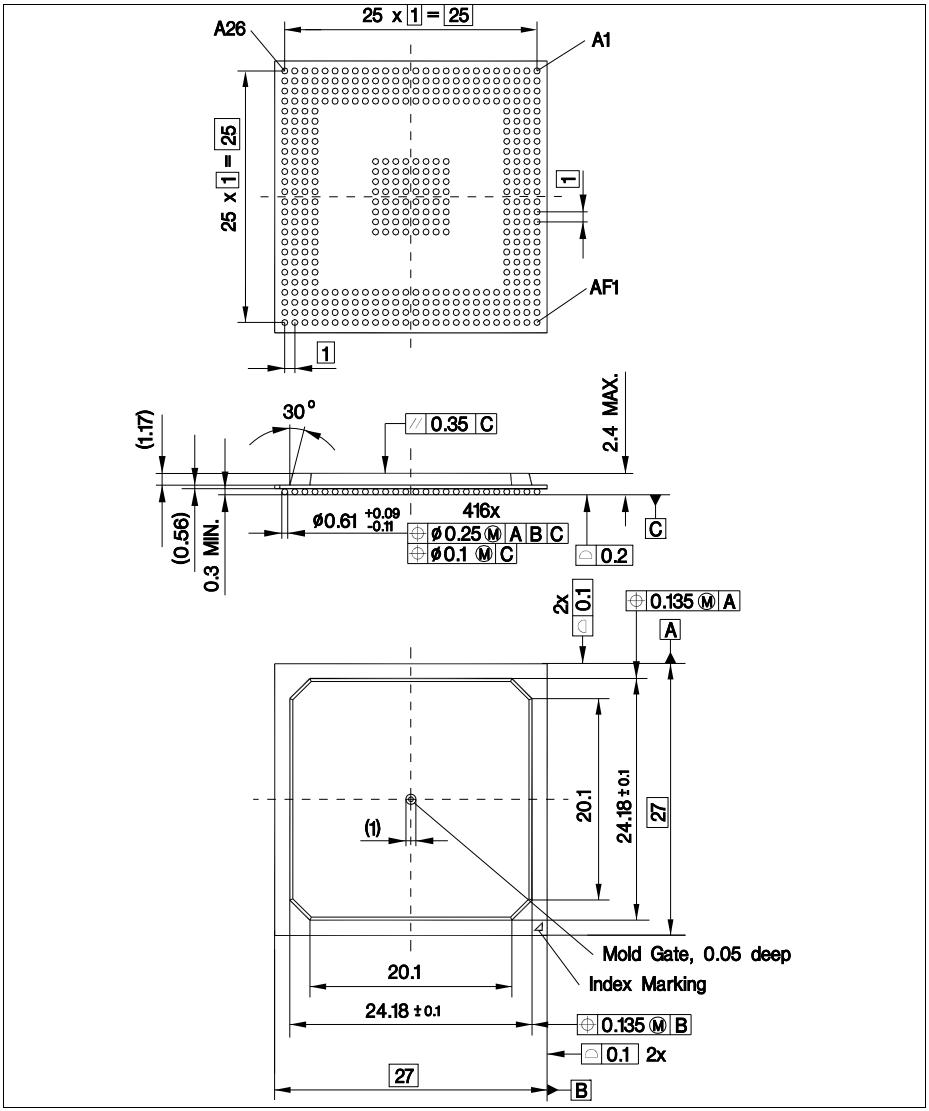


Figure 47 Package Outlines P/PG-BGA-416-27, Plastic (Green) Ball Grid Array

You can find all of our packages, sorts of packing and others in Infineon Internet Page.

5.4.3 Flash Memory Parameters

The data retention time of the TC1797's Flash memory (i.e. the time after which stored data can still be retrieved) depends on the number of times the Flash memory has been erased and programmed.

Table 34 Flash Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Program Flash Retention Time, Physical Sector[1)2)]	t_{RET} CC	20	–	–	years	Max. 1000 erase/program cycles
Program Flash Retention Time Logical Sector[1)2)]	t_{RETL} CC	20	–	–	years	Max. 100 erase/program cycles
Data Flash Endurance (64 KB)	N_E CC	30 000	–	–	cycles	Max. data retention time 5 years
Data Flash Endurance, EEPROM Emulation (4 × 16 KB)	N_{E8} CC	120000	–	–	cycles	Max. data retention time 5 years
Programming Time per Page[3)]	t_{PR} CC	–	–	5	ms	–
Program Flash Erase Time per 256-KB Sector	t_{ERP} CC	–	–	5	s	f_{CPU} = 180 MHz
Data Flash Erase Time for 2 × 32-KB Sectors	t_{ERD} CC	–	–	2.5	s	f_{CPU} = 180 MHz
Wake-up time	t_{WU} CC	–	–	4000/f_{CPU} + 180	µs	–

1) Storage and inactive time included.

2) At average weighted junction temperature T_j = 100°C, or
the retention time at average weighted temperature of T_j = 110°C is minimum 10 years, or
the retention time at average weighted temperature of T_j = 150°C is minimum 0.7 years.

3) In case the Program Verify feature detects weak bits, these bits will be programmed once more. The reprogramming takes additional 5 ms.

5.4.4 Quality Declarations

Table 35 Quality Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Operation Lifetime[1]	t_{OP}	–	–	24000	hours	–[2) 3)]
ESD susceptibility according to Human Body Model (HBM)	V_{HBM}	–	–	2000	V	Conforming to JESD22-A114-B
ESD susceptibility of the LVDS pins	V_{HBM1}	–	–	500	V	–
ESD susceptibility according to Charged Device Model (CDM)	V_{CDM}	–	–	500	V	Conforming to JESD22-C101-C
Moisture Sensitivity Level	MSL	–	–	3	–	Conforming to Jedec J-STD-020C for 240°C

1) This lifetime refers only to the time when the device is powered on.

2) For worst-case temperature profile equivalent to:
2000 hours at T_j = 150°C
16000 hours at T_j = 125°C
6000 hours at T_j = 110°C

3) This 30000 hours worst-case temperature profile is also covered:
300 hours at T_j = 150°C
1000 hours at T_j = 140°C
1700 hours at T_j = 130°C
24000 hours at T_j = 120°C
3000 hours at T_j = 110°C

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