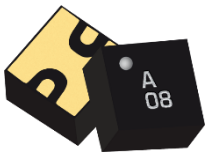
Chip Scale Package MMIC 50 GHz 10dB Attenuator ATN10-0050CSP1

1 Device Overview



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1.1 General Description

The ATN10-0050CSP1 is a surface mount GaAs MMIC 10dB attenuator in a chip scale package (CSP). This attenuator is an ideal solution for attenuating a signal and can be used in a wide range of applications. The CSP allows for extreme miniaturization of SMT footprint while providing die-like performance. GaAs MMIC technology provides consistent unit-to-unit performance in a small, low-cost form factor. Compensates for high frequency board losses with a positive gain slope. A 50-ohm match is maintained over the entire operating frequency range.

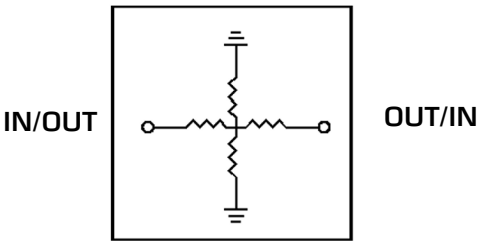
1.2 Features

- Small 1.5 x 1.5 mm package size
- 10dB attenuation from DC to 50 GHz
- 22dB typical return loss over operating band
- 1W Power Handling
- Low SWaP
- S2P data: ATN10-0050CSP1.s2p

1.3 Applications

- 5G
- Airborne Applications
- Test Equipment
- Amplitude Matching
- Precision Characterization
- High Channel Count Systems

1.4 Functional Block Diagram



1.5 Part Ordering Options[1]

Part Number	Attenuation (dB)	Description	Package	Green Status	Product Lifecycle	Export Classification
ATN10-0050CSP1	10	1.5 x 1.5 mm CSP	CSP1	RoHS	Active	EAR99
EVB-ATN10-0050	10	Connectorized Eval Module	Module			

[1] Refer to our website for a list of definitions for terminology presented in this table.

Table of Contents

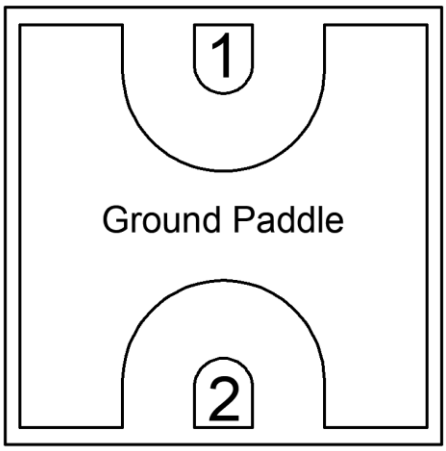
Revision History

Revision Code	Revision Date	Comment
-	April 2022	Datasheet Initial Release
A	June 2022	Outline Drawings Updated

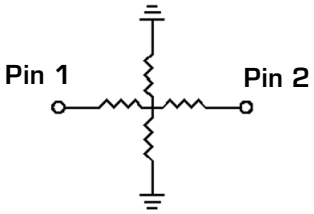
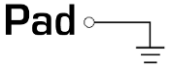
2 Port Configurations and Functions

2.1 Port Diagram

An x-ray view of the ATN10-0050CSP1 package outline drawing is shown below. The ATN attenuators are symmetrical allowing Port 1 or Port 2 to be used as the input.



2.2 Port Functions

Port	Function	Description	Equivalent Circuit
Pin 1	Input/Output	Pin 1 and pin 2 are DC connected to each other and ground through a T-network of resistors.	
Pin 2	Input/Output		
GND	Ground	SM package ground path is provided through the ground paddle.	

3 Specifications

3.1 Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If these limits are exceeded, the device may be inoperable or have a reduced lifetime.

Parameter	Maximum Rating	Units
Power Handling, at any Port	1	W
Operating Temperature	-55 to +100	°C
Storage Temperature	-65 to +125	°C

3.2 Package Information

Parameter	Details	Rating
ESD	Human Body Model (HBM), per MIL-STD-750, Method 1020	TBD

3.3 Electrical Specifications[2]

The electrical specifications apply at T_A=+25°C in a 50Ω system. Typical data shown is for the equalizer in a SM package with a sine wave input applied to port 1.

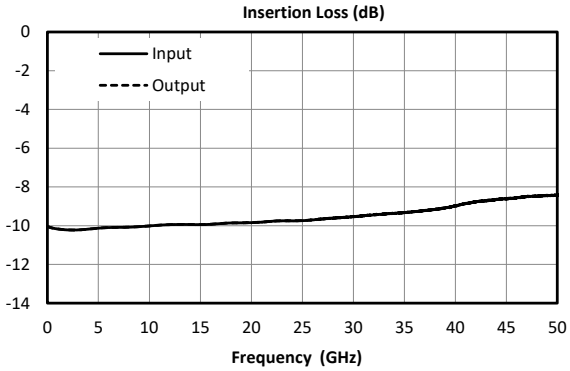
Min and Max limits are guaranteed at T_A=+25°C. All bare die are 100% DC tested and visually inspected.

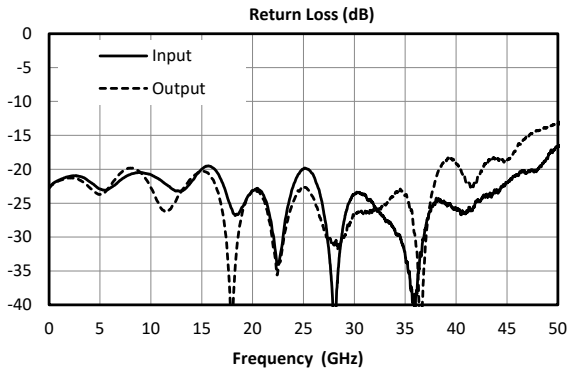
Parameter	Frequency Range (GHz)	Min	Typ	Max
Insertion Loss (dB)	DC to 30		10	
	30 to 50		9	
Return Loss (dB)	DC to 40	15	24	
	40 to 50		18	
Impedance (Ω)	DC to 50		50	

[2] Attenuator is symmetrical. Reverse measurement is equivalent to forward measurement. All measurements taken in eval and de-embedded to the CSP1 pad interface.

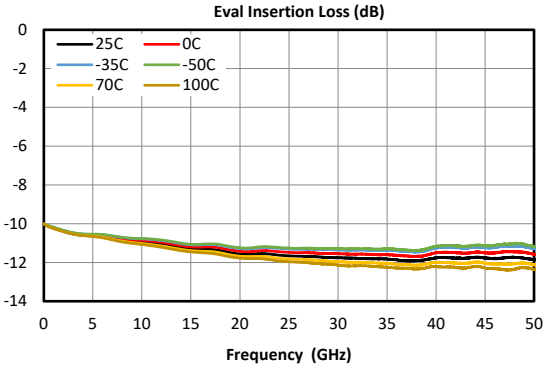
3.4 Typical Performance Plots

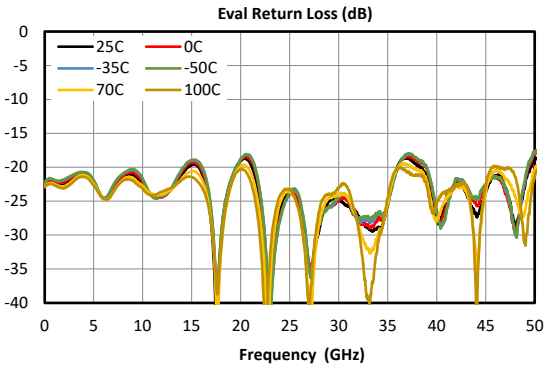
3.4.1 Electrical Performance[3]





3.4.2 Electrical Performance Over Temperature[4]

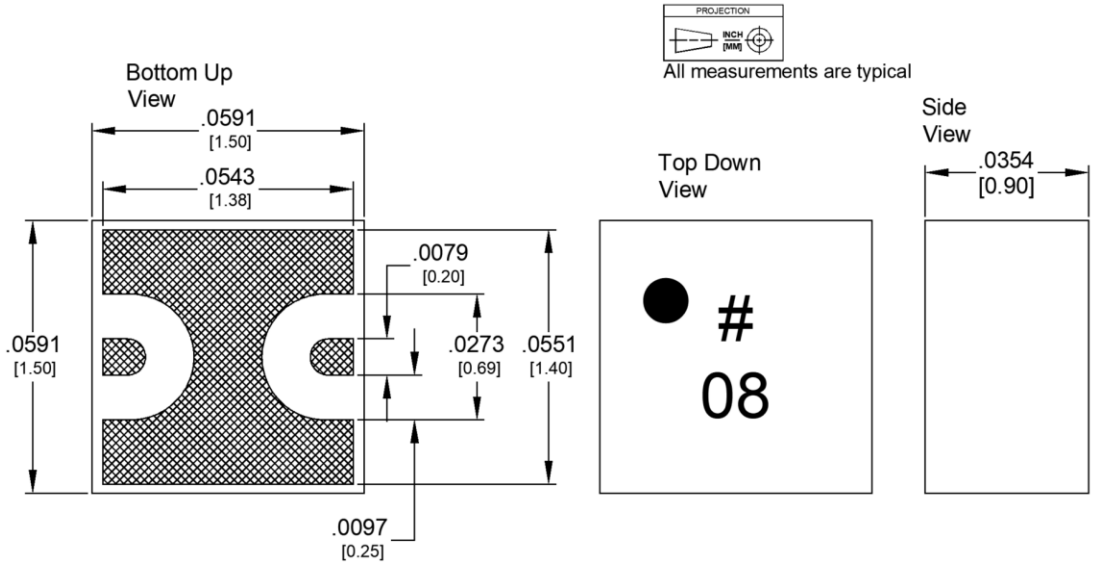




[3] Electrical Performance Data is de-embedded to the CSP package ports
[4] Evaluation board performance is shown as a proxy for device performance due to fixturing variability over temperature

4 Mechanical Data

4.1 CSP1 Package Outline Drawing

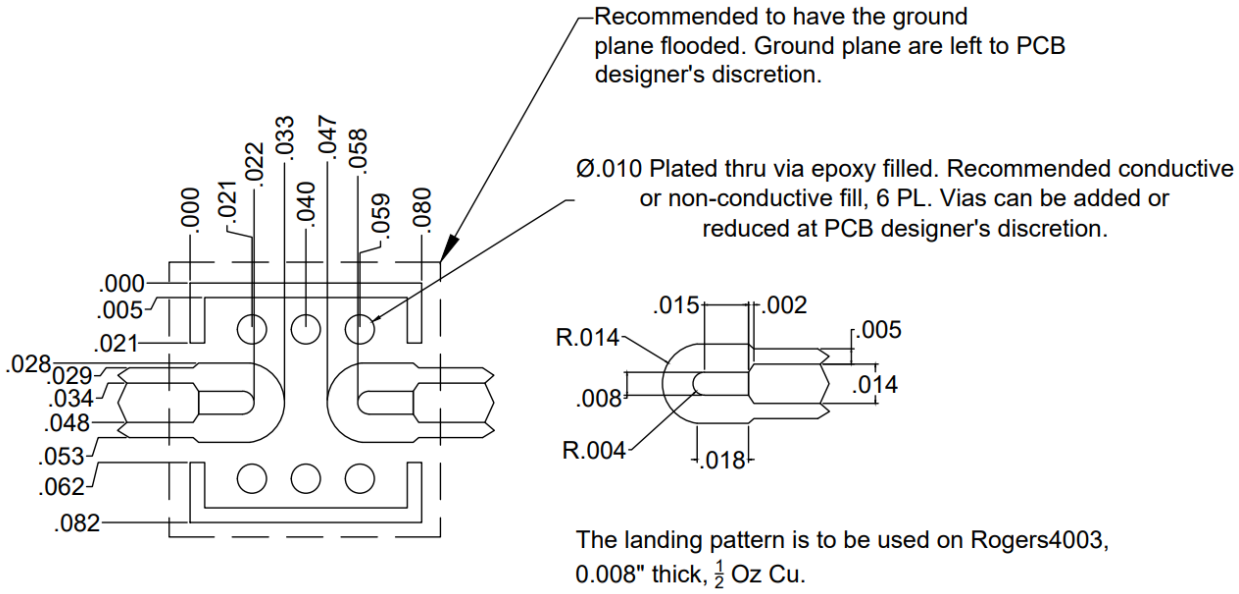


Unless otherwise specified, dimensions are in inches. Tolerances are:

.X ±.1
.XXX ±.004

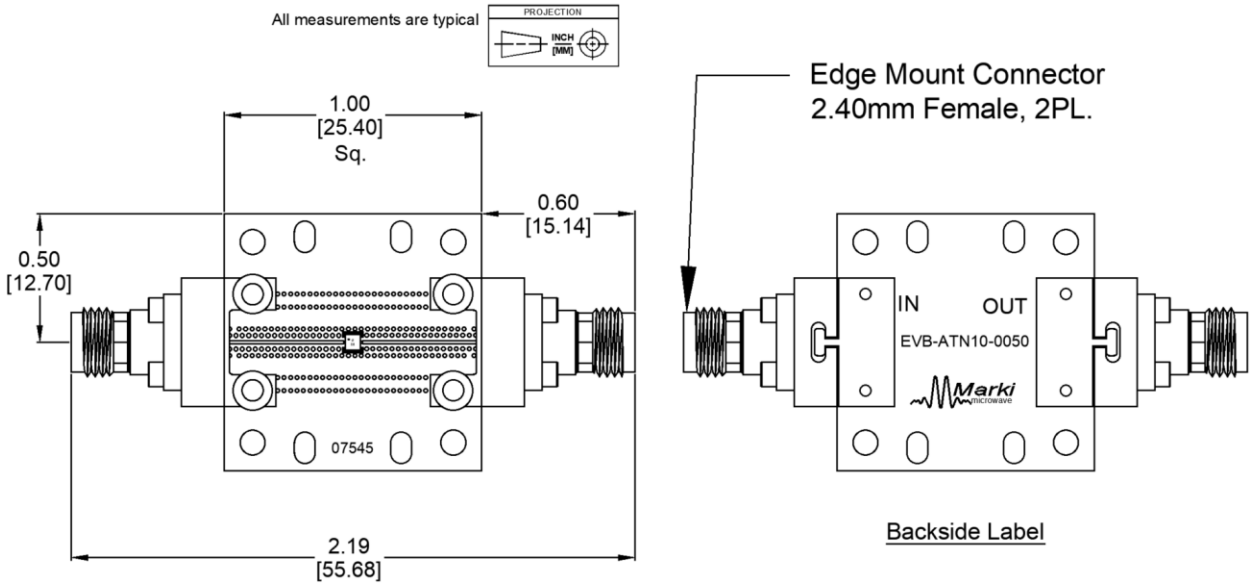
1. Front to back registration to be 50.8µm max.
2. Circuits to be shipped individually.
3. Shaded areas are metalized.
4. Finish: Ni: 0.5 - 2.5 µm
   Pd: 0.02 - 0.15 µm
   Au: 0.003 - 0.015 µm

4.2 CSP1 Package Footprint



SM-Package Surface-Mount Landing Pattern
Click here for a DXF of the above layout.
Click here for leaded solder reflow. Click here for lead-free solder reflow

4.3 EVB Package Outline Drawing



Unless otherwise specified, dimensions are in inches. Tolerances are:

.XX	±.02
.XXX	±.005