

September 2013

## GENERAL DESCRIPTION

The HI-8382 and HI-8383 bus interface products are silicon gate CMOS devices designed as a line driver in accordance with the ARINC 429 bus specifications.

Inputs are provided for clocking and synchronization. These signals are AND'd with the DATA inputs to enhance system performance and allow the HI-8382 to be used in a variety of applications. Both logic and synchronization inputs feature built-in 2,000V minimum ESD input protection as well as TTL and CMOS compatibility.

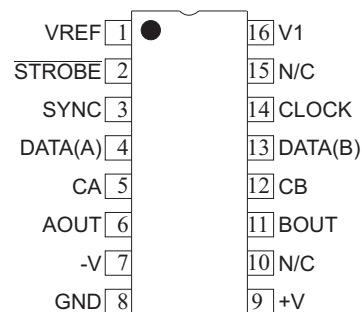
The differential outputs of the HI-8382 are independently programmable to either the high speed or low speed ARINC 429 output rise and fall time specifications through the use of two external capacitors. The output voltage swing is also adjustable by the application of an external voltage to the VREF input. The HI-8382 has on-chip Zener diodes in series with a fuse to each differential output protecting the ARINC bus from an overvoltage failure. The outputs each have a series resistance of 37.5 ohms. The HI-8383 is identical to the HI-8382 except that the series resistors are 13 ohms and the overvoltage protection circuitry has been eliminated.

The updated HI-318X and HI-8585 ARINC 429 line drivers are recommended for all new designs where logic signals must be converted to ARINC 429 levels such as a user ASIC, the HI-3282 or HI-8282A ARINC 429 Serial Transmitter/Dual Receiver, the HI-6010 ARINC 429 Transmitter/Receiver or the HI-8783 ARINC interface device. Holt products are readily available for both industrial and extended temperature ranges. Please contact the Holt Sales Department for additional information, including data sheets for any of the Holt products mentioned above.

## FEATURES

- Low power CMOS
- TTL and CMOS compatible inputs
- Programmable output voltage swing
- Adjustable ARINC rise and fall times
- Operates at data rates up to 100 Kbits
- Overvoltage protection
- Industrial and extended temperature ranges
- DSCC SMD part number

## PIN CONFIGURATION (Top View)

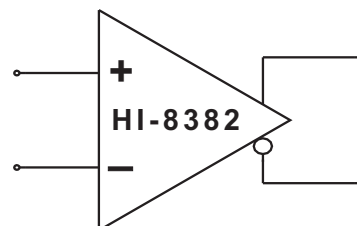


**HI-8382C / CT / CM-01 / CM-03**  
**SMD # 5962-8687901EA**

**16 - PIN CERAMIC SIDE-BRAZED DIP**

*(See Page 6 for additional package pin configurations)*

## FUNCTION



**ARINC 429 DIFFERENTIAL LINE DRIVER**

## TRUTH TABLE

| SYNC | CLOCK | DATA(A) | DATA(B) | AOUT  | BOUT  | COMMENTS |
|------|-------|---------|---------|-------|-------|----------|
| X    | L     | X       | X       | 0V    | 0V    | NULL     |
| L    | X     | X       | X       | 0V    | 0V    | NULL     |
| H    | H     | L       | L       | 0V    | 0V    | NULL     |
| H    | H     | L       | H       | -VREF | +VREF | LOW      |
| H    | H     | H       | L       | +VREF | -VREF | HIGH     |
| H    | H     | H       | H       | 0V    | 0V    | NULL     |

## FUNCTIONAL DESCRIPTION

The SYNC and CLOCK inputs establish data synchronization utilizing two AND gates, one for each data input. Each logic input, including the power enable (STROBE) input, are TTL/CMOS compatible. Besides reducing chip current drain, STROBE also floats each output. However the overvoltage fuses and diodes of the HI-8382 are not switched out.

Figure 1 illustrates a typical ARINC 429 bus application. Three power supplies are necessary to operate the HI-8382; typically +15V, -15V and +5V. The chip also works with  $\pm 12V$  supplies. The +5V supply can also provide a reference voltage that determines the output voltage swing. The differential output voltage swing will equal  $2V_{REF}$ . If a value of  $V_{REF}$  other than +5V is needed, a separate +5V power supply is required for pin V1.

With the DATA (A) input at a logic high and DATA (B) input at a logic low, AOUT will switch to the +VREF rail and BOUT will switch to the -VREF rail (ARINC HIGH state). With both data input signals at a logic low state, the outputs will both switch to 0V (ARINC NULL state).

The driver output impedance,  $R_{OUT}$ , is nominally 75 ohms. The rise and fall times of the outputs can be calibrated through the selection of two external capacitor values that are connected to the CA and CB input pins. Typical values for high-speed operation (100KBPS) are  $C_A = C_B = 75pF$  and for low-speed operation (12.5 to 14KBPS)  $C_A = C_B = 500pF$ . The driver can be externally powered down by applying a logic high to the STROBE input pin. If this feature is not being used, the pin should be tied to ground.

The CA and CB pins are inputs to unity gain amplifiers. Therefore they must be allowed to swing to -5V. Provision to

switch capacitors must be done with analog switches that allow voltages below their ground.

Both ARINC outputs of the HI-8382 are protected by internal fuses capable of sinking between 800 - 900 mA for short periods of time (125 $\mu$ s).

### POWER SUPPLY SEQUENCING

The power supplies should be controlled to prevent large currents during supply turn-on and turn-off. The recommended sequence is +V followed by V1, always ensuring that +V is the most positive supply. The -V supply is not critical and can be asserted at any time.

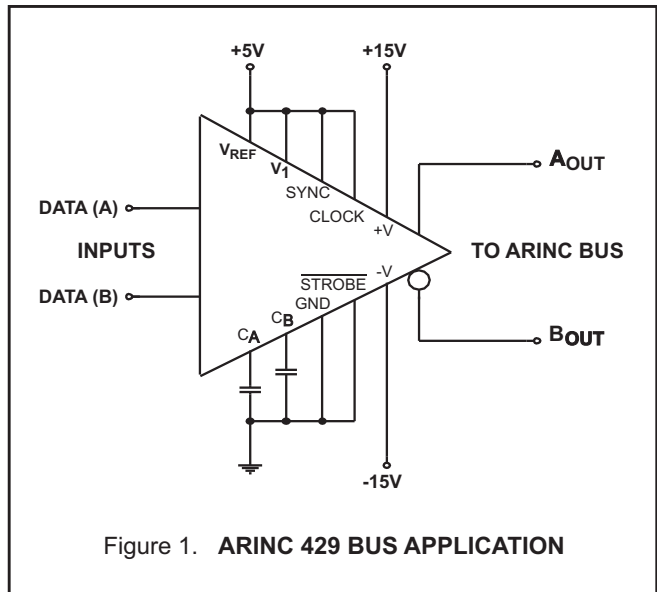


Figure 1. ARINC 429 BUS APPLICATION

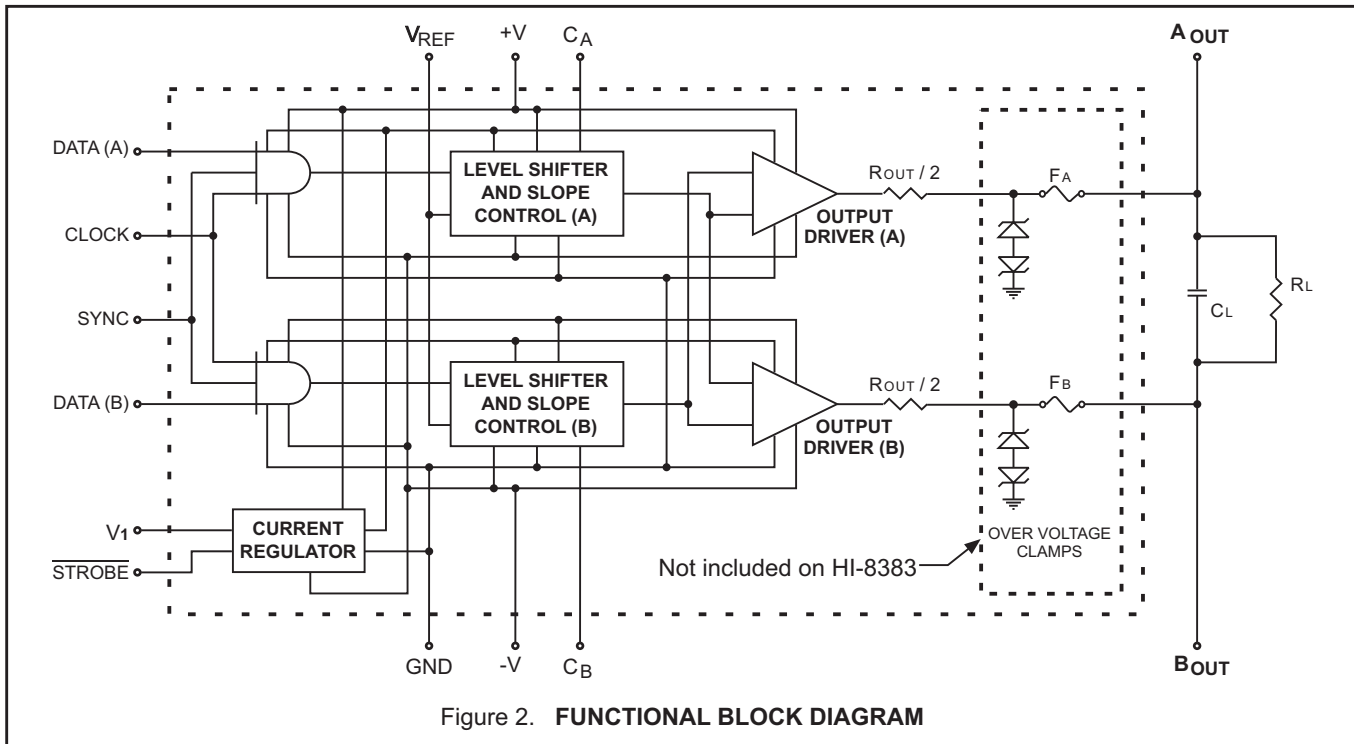


Figure 2. FUNCTIONAL BLOCK DIAGRAM

## PIN DESCRIPTIONS

| SYMBOL   | FUNCTION | DESCRIPTION  |
|----------|----------|--|
| VREF     | POWER    | THE REFERENCE VOLTAGE USED TO DETERMINE THE OUTPUT VOLTAGE SWING |
| STROBE   | INPUT    | A LOGIC HIGH ON THIS INPUT PLACES THE DRIVER IN POWER DOWN MODE  |
| SYNC     | INPUT    | SYNCHRONIZES DATA INPUTS   |
| DATA (A) | INPUT    | DATA INPUT TERMINAL A  |
| CA       | INPUT    | CONNECTION FOR DATA (A) SLEW-RATE CAPACITOR                      |
| AOUT     | OUTPUT   | ARINC OUTPUT TERMINAL A  |
| -V       | POWER    | -12V to -15V   |
| GND      | POWER    | 0.0V   |
| +V       | POWER    | +12V to +15V   |
| BOUT     | OUTPUT   | ARINC OUTPUT TERMINAL B  |
| Cb       | INPUT    | CONNECTION FOR DATA (B) SLEW-RATE CAPACITOR                      |
| DATA (B) | INPUT    | DATA INPUT TERMINAL B  |
| CLOCK    | INPUT    | SYNCHRONIZES DATA INPUTS   |
| V1       | POWER    | +5V ±5%  |

## ABSOLUTE MAXIMUM RATINGS

All Voltages referenced to GND, TA = Operating Temperature Range (unless otherwise specified)

| PARAMETER                                    | SYMBOL         | CONDITIONS  | OPERATING RANGE  | MAXIMUM                          | UNIT                         |
|--|----------------|---|--|----------------------------------|------------------------------|
| Differential Voltage                         | VDIF           | Voltage between +V and -V terminals   |  | 40                               | V                            |
| Supply Voltage                               | +V<br>-V<br>V1 |   | +10.8 to +16.5<br>-10.8 to -16.5<br>+5 ±5%               | +7                               | V<br>V<br>V                  |
| Voltage Reference                            | VREF           | For ARINC 429<br>For Applications other than ARINC                                | +5 ±5%<br>0 to 6   | 6<br>6                           | V<br>V                       |
| Input Voltage Range                          | VIN            |   |  | ≥ GND -0.3<br>≤ V1 +0.3          | V<br>V                       |
| Output Short-Circuit Duration                |                | See Note: 1   |  |                                  |                              |
| Output Overvoltage Protection                |                | See Note: 2   |  |                                  |                              |
| Operating Temperature Range                  | TA             | Extended<br>Industrial  | -55 to +125<br>-40 to +85                                |                                  | °C<br>°C                     |
| Storage Temperature Range                    | TSTG           | Ceramic & Plastic   | -65 to +150  |                                  | °C                           |
| Lead Temperature                             |                | Soldering, 10 seconds   |  | +275                             | °C                           |
| Junction Temperature                         | TJ             |   |  | +175                             | °C                           |
| Power Dissipation                            | PD             | 16-Pin Ceramic DIP<br>28-Pin Ceramic LCC<br>28-Pin Plastic PLCC<br>32-Pin CERQUAD | See Note: 3<br>See Note: 3<br>See Note: 3<br>See Note: 3 | 1.725<br>1.120<br>2.143<br>1.725 | W<br>W<br>W<br>W             |
| Thermal Resistance,<br>(Junction-to-Ambient) | ØJA            | 16-Pin Ceramic DIP<br>28-Pin Ceramic LCC<br>28-Pin Plastic PLCC<br>32-Pin CERQUAD |  | 86.5<br>133.7<br>70.0<br>86.5    | °C/W<br>°C/W<br>°C/W<br>°C/W |

Note 1. Heatsinking may be required for Output Short Circuit at +125°C and for 100KBPS at +125°C.

Note 2. The fuses used for Output Overvoltage Protection may be blown by the presence of a voltage at either output that is greater than ±12.0V with respect to GND. (HI-8382 only)

Note 3. Derate above +25°C, 11.5mW/°C for 16-PIN DIP and 32-PIN CERQUAD, 7.5 mW/°C for 28-PIN LCC, 14.2 mW/°C for 28-PIN PLCC

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

+V = +15V, -V = -15V, V<sub>1</sub> = V<sub>REF</sub> = +5.0V, T<sub>A</sub> = Operating Temperature Range (unless otherwise specified).

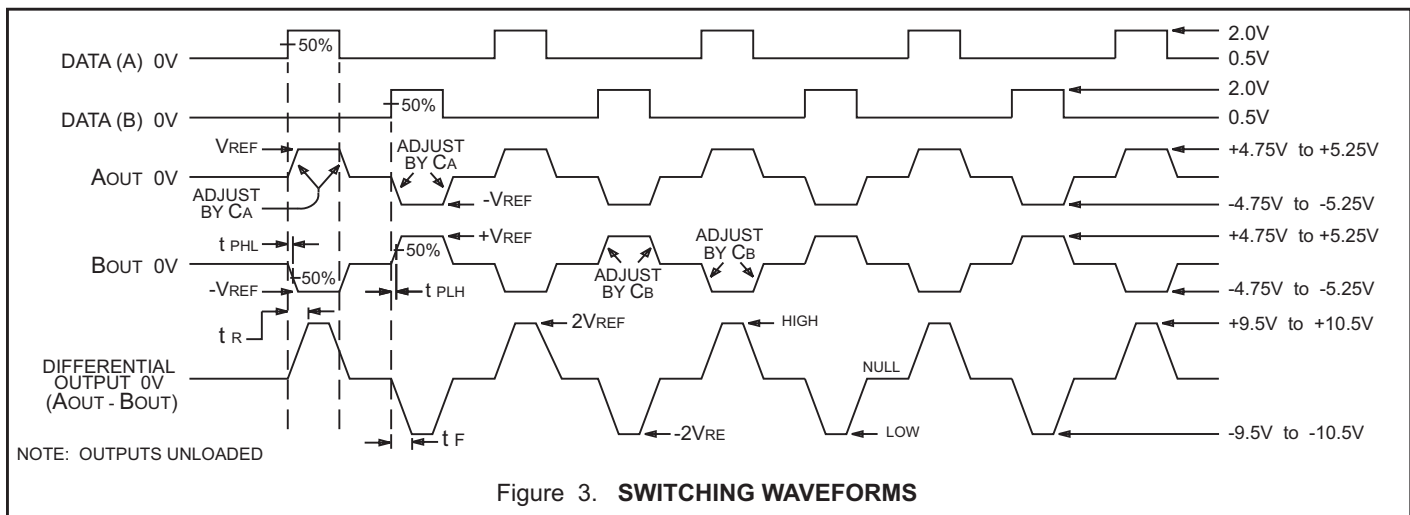
| PARAMETER                                     | SYMBOL                    | CONDITION   | MIN                     | TYP | MAX                     | UNITS |
|---|---------------------------|---|-------------------------|-----|-------------------------|-------|
| Supply Current +V (Operating)                 | ICCOP (+V)                | No Load (0 - 100KBPS)                             |                         |     | +11                     | mA    |
| Supply Current -V (Operating)                 | ICCOP (-V)                | No Load (0 - 100KBPS)                             | -11                     |     |                         | mA    |
| Supply Current V <sub>1</sub> (Operating)     | ICCOP (V <sub>1</sub> )   | No Load (0 - 100KBPS)                             |                         |     | 500                     | μA    |
| Supply Current V <sub>REF</sub> (Operating)   | ICCOP (V <sub>REF</sub> ) | No Load (0 - 100KBPS)                             |                         |     | 500                     | μA    |
| Supply Current +V (Power Down)                | ICCPD (+V)                | STROBE = HIGH                                     |                         |     | 475                     | uA    |
| Supply Current -V (Power Down)                | ICCPD (-V)                | STROBE = HIGH                                     | -475                    |     |                         | uA    |
| Supply Current +V (During Short Circuit Test) | I <sub>SC</sub> (+V)      | Short to Ground (See Note: 1)                     |                         |     | 150                     | mA    |
| Supply Current -V (During Short Circuit Test) | I <sub>SC</sub> (-V)      | Short to Ground (See Note: 1)                     | -150                    |     |                         | mA    |
| Output Short Circuit Current (Output High)    | I <sub>OHSC</sub>         | Short to Ground V <sub>MIN</sub> =0 (See Note: 2) |                         |     | -80                     | mA    |
| Output Short Circuit Current (Output Low)     | I <sub>OLSC</sub>         | Short to Ground V <sub>MIN</sub> =0 (See Note: 2) | +80                     |     |                         | mA    |
| Input Current (Input High)                    | I <sub>IH</sub>           |   |                         |     | 1.0                     | μA    |
| Input Current (Input Low)                     | I <sub>IL</sub>           |   |                         |     | -1.0                    | μA    |
| Input Voltage High                            | V <sub>IH</sub>           |   | 2.0                     |     |                         | V     |
| Input Voltage Low                             | V <sub>IL</sub>           |   |                         |     | 0.5                     | V     |
| Output Voltage High (Output to Ground)        | V <sub>OH</sub>           | No Load (0 - 100KBPS)                             | +V <sub>REF</sub> - .25 |     | +V <sub>REF</sub> + .25 | V     |
| Output Voltage Low (Output to Ground)         | V <sub>OL</sub>           | No Load (0 - 100KBPS)                             | -V <sub>REF</sub> - .25 |     | -V <sub>REF</sub> + .25 | V     |
| Output Voltage Null                           | V <sub>NULL</sub>         | No Load (0-100KBPS)                               | -250                    |     | +250                    | mV    |
| Input Capacitance                             | C <sub>IN</sub>           | See Note 1  |                         | 15  |                         | pF    |

Note 1. Not tested, but characterized at initial device design and after major process and/or design change which affects this parameter.  
 Note 2. Interchangeability of force and sense is acceptable.

## AC ELECTRICAL CHARACTERISTICS

+V = +15V, -V = -15V, V<sub>1</sub> = V<sub>REF</sub> = +5.0V, T<sub>A</sub> = Operating Temperature Range (unless otherwise specified).

| PARAMETER                         | SYMBOL           | CONDITION                    | MIN | TYP | MAX | UNITS |
|-----------------------------------|------------------|------------------------------|-----|-----|-----|-------|
| Rise Time (AOUT, BOUT)            | t <sub>R</sub>   | CA = CB = 75pF See Figure 3. | 1.0 |     | 2.0 | μs    |
| Fall Time (AOUT, BOUT)            | t <sub>F</sub>   | CA = CB = 75pF See Figure 3. | 1.0 |     | 2.0 | μs    |
| Propagation Delay Input to Output | t <sub>PLH</sub> | CA = CB = 75pF See Figure 3. |     |     | 3.0 | μs    |
| Propagation Delay Input to Output | t <sub>PHL</sub> | CA = CB = 75pF See Figure 3. |     |     | 3.0 | μs    |



# HI-8382 PACKAGE THERMAL CHARACTERISTICS

## MAXIMUM ARINC LOAD <sup>7</sup>

| PACKAGE STYLE <sup>1</sup> | ARINC 429 DATA RATE     | SUPPLY CURRENT (mA) <sup>2</sup> |                       |                        | JUNCTION TEMP, T <sub>j</sub> (°C) |                       |                        |
|----------------------------|-------------------------|----------------------------------|-----------------------|------------------------|------------------------------------|-----------------------|------------------------|
|                            |                         | T <sub>a</sub> = 25°C            | T <sub>a</sub> = 85°C | T <sub>a</sub> = 125°C | T <sub>a</sub> = 25°C              | T <sub>a</sub> = 85°C | T <sub>a</sub> = 125°C |
| 28 Lead PLCC               | Low Speed <sup>3</sup>  | 17.6                             | 17.2                  | 17.0                   | 48                                 | 107                   | 142                    |
|                            | High Speed <sup>4</sup> | 25.4                             | 24.5                  | 24.2                   | 56                                 | 110                   | 150                    |
| 16 Lead Ceramic SB DIP     | Low Speed               | 17.9                             | 17.4                  | 17.1                   | 41                                 | 103                   | 145                    |
|                            | High Speed              | 25.8                             | 24.8                  | 24.4                   | 47                                 | 112                   | 147                    |

## AOUT and BOUT Shorted To Ground <sup>5, 6, 7</sup>

| PACKAGE STYLE <sup>1</sup> | ARINC 429 DATA RATE     | SUPPLY CURRENT (mA) <sup>2</sup> |                       |                        | JUNCTION TEMP, T <sub>j</sub> (°C) |                       |                        |
|----------------------------|-------------------------|----------------------------------|-----------------------|------------------------|------------------------------------|-----------------------|------------------------|
|                            |                         | T <sub>a</sub> = 25°C            | T <sub>a</sub> = 85°C | T <sub>a</sub> = 125°C | T <sub>a</sub> = 25°C              | T <sub>a</sub> = 85°C | T <sub>a</sub> = 125°C |
| 28 Lead PLCC               | Low Speed <sup>3</sup>  | 60.1                             | 55.7                  | 52.4                   | 110                                | 157                   | 194                    |
|                            | High Speed <sup>4</sup> | 63.1                             | 56.3                  | 52.3                   | 100                                | 150                   | 182                    |
| 16 Lead Ceramic SB DIP     | Low Speed               | 62.1                             | 56.2                  | 53.0                   | 90                                 | 145                   | 180                    |
|                            | High Speed              | 64.0                             | 56.2                  | 52.2                   | 86                                 | 144                   | 176                    |

Notes:

- All data taken in still air on devices soldered to a single layer copper PCB (3" X 4.5" X .062").
- At 100% duty cycle, 15V power supplies. For 12V power supplies multiply all tabulated values by 0.8.
- Low Speed: Data Rate = 12.5 Kbps, Load: R = 400 Ohms, C = 30 nF.
- High Speed: Data Rate = 100 Kbps, Load: R = 400 Ohms, C = 10 nF. Data not presented for C = 30 nF as this is considered unrealistic for high speed operation.
- Similar results would be obtained with AOUT shorted to BOUT.
- For applications requiring survival with continuous short circuit, operation above T<sub>j</sub> = 175°C is not recommended.
- Data will vary depending on air flow and the method of heat sinking employed.

## ORDERING INFORMATION

### HI - 838x x x - xx (Ceramic)

| PART NUMBER | TEMPERATURE RANGE | FLOW | BURN IN | NOTES     |
|-------------|-------------------|------|---------|-----------|
| Blank       | -40°C to +85°C    | I    | No      |           |
| T           | -55°C to +125°C   | T    | No      |           |
| M-01        | -55°C to +125°C   | M    | Yes     | (1)       |
| M-03        | -55°C to +125°C   | DSCC | Yes     | (1) & (2) |

| PART NUMBER | PACKAGE DESCRIPTION                              | LEAD FINISH     | NOTES     |
|-------------|--|-----------------|-----------|
| C           | 16 PIN CERAMIC SIDE BRAZED DIP (16C)             | Gold            | (3) & (1) |
| S           | 28 PIN CERAMIC LEADLESS CHIP CARRIER (28S)       | Gold            | (3) & (1) |
| U           | 32 PIN CERQUAD (32U) not available with 'M' flow | Tin/Lead Solder |           |

| PART NUMBER | OUTPUT SERIES |      |
|-------------|---------------|------|
|             | RESISTANCE    | FUSE |
| 8382        | 37.5 Ohms     | Yes  |
| 8383        | 13 Ohms       | No   |

- Process Flows M and DSCC always have Tin/Lead (Sn/Pb) solder lead finish.
- DSCC SMD# 5962-8687901EA. Only available in "C" package with Sn/Pb solder lead finish.
- Gold terminal finish is Pb-Free, RoHS compliant.

## HI-8382, HI-8383

### HI - 838xJ x x (Plastic)

| PART NUMBER | LEAD FINISH                              |
|-------------|--|
| Blank       | Tin / Lead (Sn / Pb) Solder              |
| F           | 100% Matte Tin (Pb-free, RoHS compliant) |

| PART NUMBER | TEMPERATURE RANGE | FLOW | BURN IN |
|-------------|-------------------|------|---------|
| Blank       | -40°C to +85°C    | I    | No      |
| T           | -55°C to +125°C   | T    | No      |

| PART NUMBER | PACKAGE DESCRIPTION           | OUTPUT SERIES |      |
|-------------|-------------------------------|---------------|------|
|             |                               | RESISTANCE    | FUSE |
| 8382J       | 28 PIN PLASTIC PLCC (28J) (1) | 37.5 Ohms     | Yes  |
| 8383J       | 28 PIN PLASTIC PLCC (28J) (1) | 13 Ohms       | No   |

(1) NOT RECOMMENDED FOR NEW DESIGNS. The newer HI-3182PJxx and HI-3183PJxx are drop-in replacements for the older HI-8382Jxx and HI-8383Jxx respectively.

### HI - 838x PDx x (Plastic DIP)

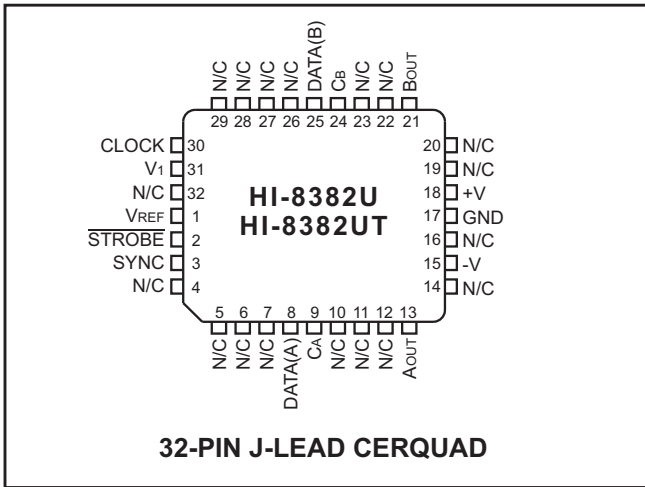
| PART NUMBER | LEAD FINISH                              |
|-------------|--|
| Blank       | Tin / Lead (Sn / Pb) Solder              |
| F           | 100% Matte Tin (Pb-free, RoHS compliant) |

| PART NUMBER | TEMPERATURE RANGE | FLOW | BURN IN |
|-------------|-------------------|------|---------|
| I           | -40°C to +85°C    | I    | No      |
| T           | -55°C to +125°C   | T    | No      |
| M           | -55°C to +125°C   | M    | Yes     |

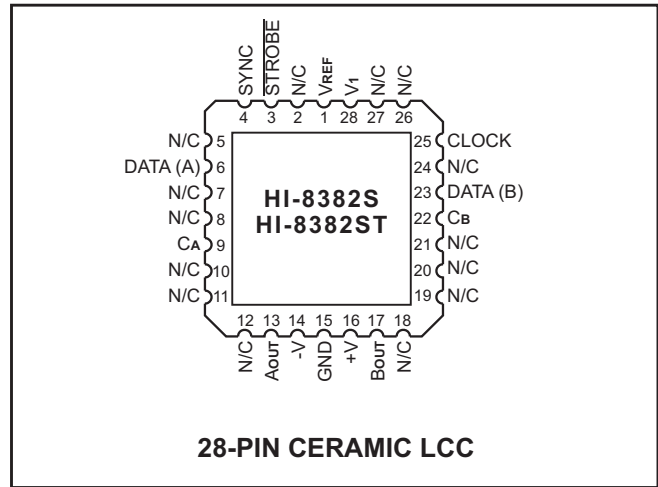
| PART NUMBER | PACKAGE DESCRIPTION | OUTPUT SERIES |      |
|-------------|---------------------|---------------|------|
|             |                     | RESISTANCE    | FUSE |
| 8382        | 16 PIN PLASTIC DIP  | 37.5 Ohms     | Yes  |
| 8383        | 16 PIN PLASTIC DIP  | 13 Ohms       | No   |

## ADDITIONAL PIN CONFIGURATIONS

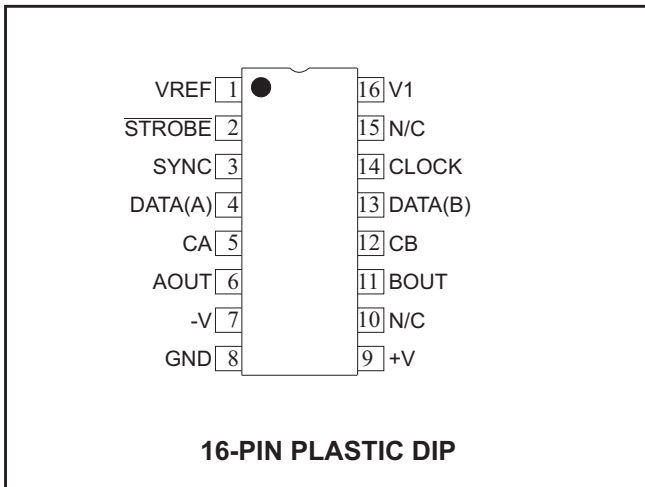
(See page 1 for the 16-pin Ceramic Side-Braced DIP Package )



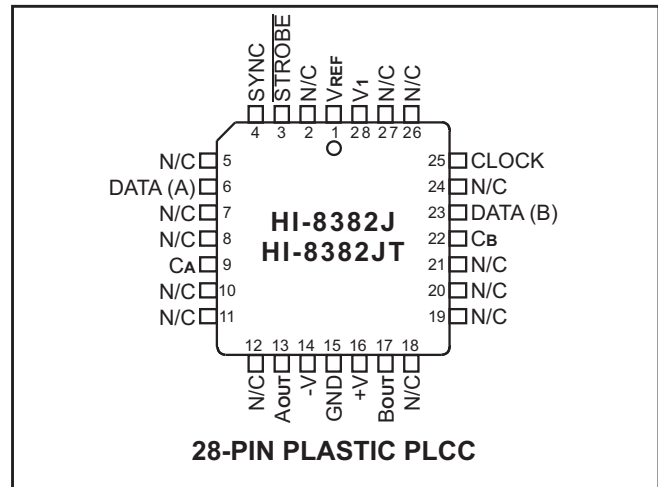
32-PIN J-LEAD CERQUAD



28-PIN CERAMIC LCC



16-PIN PLASTIC DIP



28-PIN PLASTIC PLCC

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## REVISION HISTORY

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| P/N    | Rev | Date     | Description of Change  |
|--------|-----|----------|--|
| DS8382 | E   | 02/26/09 | Clarified the temperature ranges, and Note (1) in the Ordering Information.                          |
|        | F   | 09/16/11 | Realigned pin names and numbers with package pin locations in Additional Pin Configuration drawings. |
|        | G   | 09/10/13 | Added Plastic DIP package option.  |

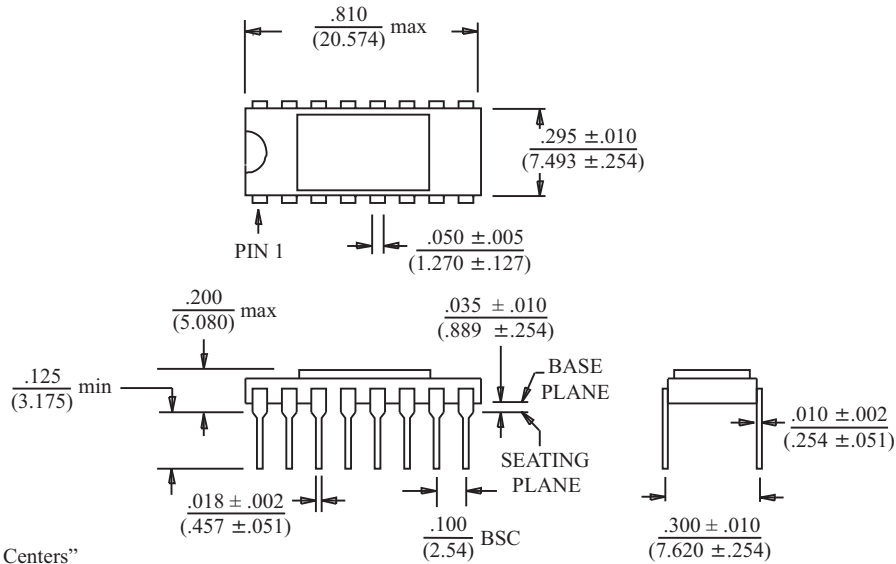
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**16-PIN CERAMIC SIDE-BRAZED DIP**

*inches (millimeters)*

Package Type: 16C

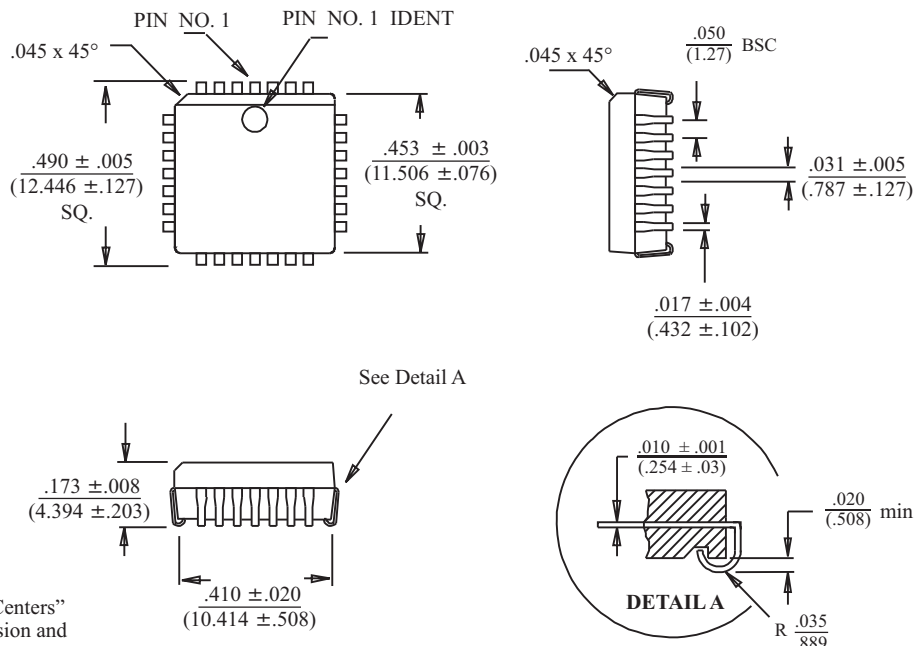


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

**28-PIN PLASTIC PLCC**

*inches (millimeters)*

Package Type: 28J

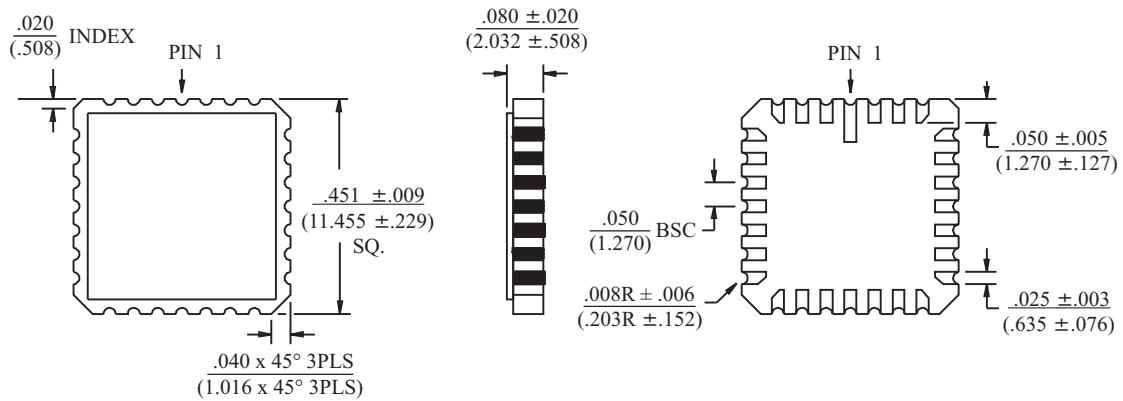


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

**28-PIN CERAMIC LEADLESS CHIP CARRIER**

*inches (millimeters)*

Package Type: 28S

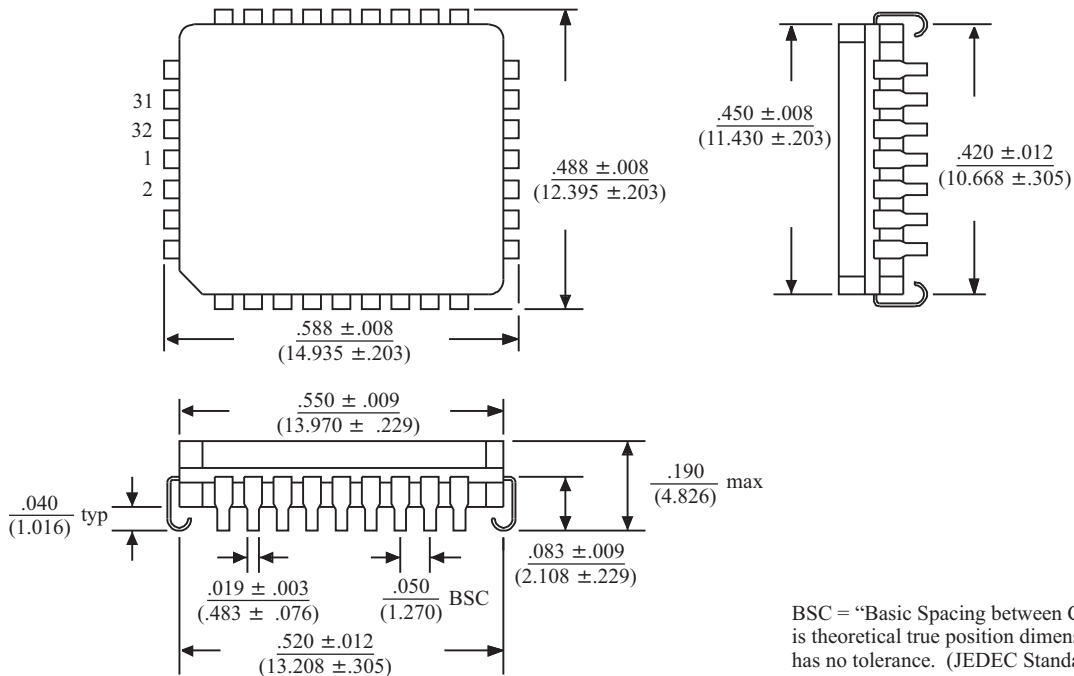


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

**32-PIN J-LEAD CERQUAD**

*inches (millimeters)*

Package Type: 32U

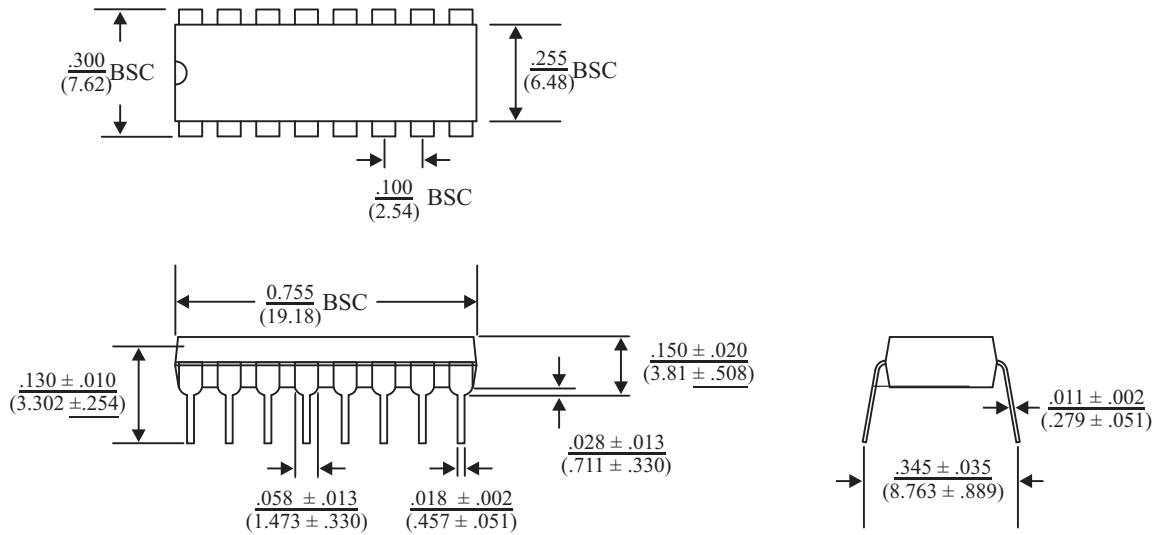


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

**16-PIN PLASTIC DUAL IN-LINE PACKAGE (PDIP)  
(300mil Body)**

*inches (millimeters)*

Package Type: 16PDIP



BSC = "Basic Spacing between Centers"  
is theoretical true position dimension and  
has no tolerance. (JEDEC Standard 95)