CDx4HC73 CD74HCT73 Dual J-K Flip-Flop with Reset Negative-Edge Trigger

1 Features

- Hysteresis on clock inputs for improved noise immunity and increased input rise and fall times
- Asynchronous reset
- Complementary outputs
- Buffered inputs
- Typical f_{MAX} = 60 MHz at V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C
- Fanout (over temperature range)
  - Standard outputs: 10 LSTTL loads
  - Bus driver outputs: 15 LSTTL loads
- Wide operating temperature range: –55°C to 125°C
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL Logic ICs
- HC types
  - 2 V to 6V operation
  - High noise immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5 V
- HCT types
  - 4.5 V to 5.5 V operation
  - Direct LSTTL input logic compatibility, V_{IL} = 0.8 V (max), V_{IH} = 2 V (min)
  - CMOS input compatibility, $I_I \leq 1$ µA at V_{OL}, V_{OH}

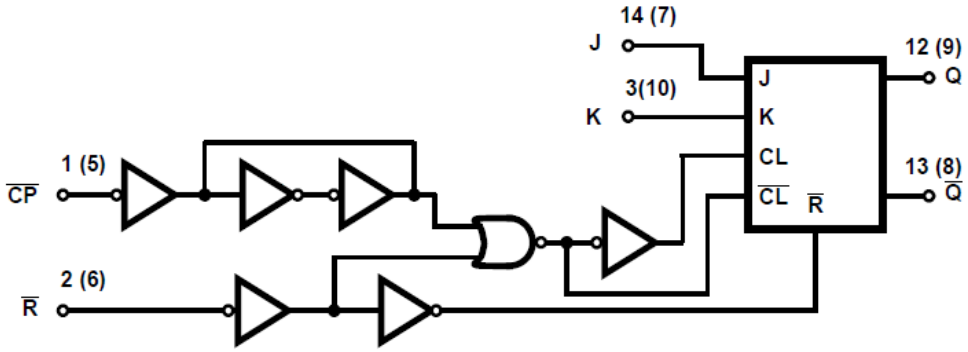
2 Description

The ’HC73 and CD74HCT73 utilize silicon gate CMOS technology to achieve operating speeds equivalent to LSTTL parts. They exhibit the low power consumption of standard CMOS integrated circuits, together with the ability to drive 10 LSTTL loads.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
CD74HC73M	SOIC (14)	8.65 mm × 3.90 mm
CD74HCT73M	SOIC (14)	8.65 mm × 3.90 mm
CD74HC73E	PDIP (14)	19.31 mm × 6.35 mm
CD74HCT73E	PDIP (14)	19.31 mm × 6.35 mm
CD54HC73F	CDIP (14)	19.55 mm × 6.71 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional Block Diagram

Table of Contents

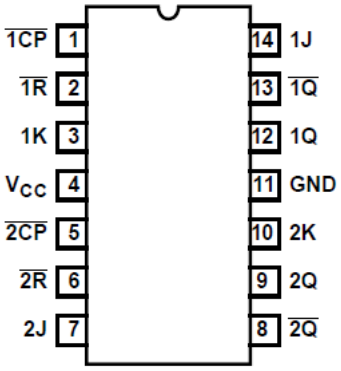
3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (January 2022) to Revision G (October 2022)	Page
• Increased RθJA for packages: D (86 to 138.7); N (80 to 91)	4

Changes from Revision E (August 2003) to Revision F (January 2022)	Page
• Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect modern data sheet standards	1

4 Pin Configuration and Functions



J, N, or D package
14-Pin CDIP, PDIP, or SOIC
Top View

5 Specifications

5.1 Absolute Maximum Ratings[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input diode current	For $V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V		± 20	mA
I_O	Drain current, per output	For $–0.5 V < V_O < V_{CC} + 0.5$ V		± 25	mA
I_{OK}	Output diode current	For $V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V		± 20	mA
I_O	Output source or sink current per output pin	For $V_O > –0.5$ V or $V_O < V_{CC} + 0.5$ V		± 25	mA
I_{CC}	Continuous current through V_{CC} or GND			± 50	mA
T_J	Junction temperature			±150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

5.2 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage range	HC types	2	6	V
		HCT types	4.5	5.5	
V_I, V_O	Input or output voltage		0	V_{CC}	V
t_t	Input rise and fall time	2 V		1000	ns
		4.5 V		500	
		6 V		400	
T_A	Temperature range		–55	125	℃

5.3 Thermal Information

THERMAL METRIC		D (SOIC) 14 PINS	N (PDIP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[1]	138.7	91	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	93.8	78.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	94.7	70.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	49.1	58.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter resistance	94.3	70.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.4 Electrical Specifications

PARAMETER		TEST CONDITIONS(2)	V_{CC} (V)	25℃			–40℃ to 85℃		–55℃ to 125℃		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
V_{IH}	High level input voltage		2	1.5			1.5		1.5		V
			4.5	3.15			3.15		3.15		
			6	4.2			4.2		4.2		
V_{IL}	Low level input voltage		2			0.5		0.5		0.5	V
			4.5			1.35		1.35		1.35	
			6			1.8		1.8		1.8	
V_{OH}	High level output voltage	I_{OH} = – 20 μA	2	1.9			1.9		1.9		V
		I_{OH} = – 20 μA	4.5	4.4			4.4		4.4		
		I_{OH} = – 20 μA	6	5.9			5.9		5.9		
	High level output voltage	I_{OH} = – 4 mA	4.5	3.98			3.84		3.7		
		I_{OH} = – 5.2 mA	6	5.48			5.34		5.2		
V_{OL}	Low level output voltage	I_{OL} = 20 μA	2			0.1		0.1		0.1	V
		I_{OL} = 20 μA	4.5			0.1		0.1		0.1	
		I_{OL} = 20 μA	6			0.1		0.1		0.1	
	Low level output voltage	I_{OL} = 4 mA	4.5			0.26		0.33		0.4	
		I_{OL} = 5.2 mA	6			0.26		0.33		0.4	
I_I	Input leakage current	V_I = V_{CC} or GND	6			±0.1		±1		±1	mA
I_{CC}	Supply current	V_I = V_{CC} or GND	6			4		40		80	mA
HCT TYPES											
V_{IH}	High level input voltage		4.5 to 5.5	2			2		2		V
V_{IL}	Low level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V_{OH}	High level output voltage	I_{OH} = – 20 μA	4.5	4.4			4.4		4.4		V
	High level output voltage	I_{OH} = – 4 mA	4.5	3.98			3.84		3.7		
V_{OL}	Low level output voltage	I_{OL} = 20 μA	4.5			0.1		0.1		0.1	V
	Low level output voltage	I_{OL} = 4 mA	4.5			0.26		0.33		0.4	
I_I	Input leakage current	V_I = V_{CC} and GND	5.5			±0.1		±1		±1	μA
I_{CC}	Supply current	V_I = V_{CC} and GND	5.5			4		40		80	μA
ΔI_{CC} (1)	Additional supply current per input pin	All inputs held at V_{CC} – 2.1	4.5 to 5.5		100	108		135		147	μA

(1) For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.
(2) V_I = V_{IH} or V_{IL}.

5.5 Prerequisite for Switching Specifications

PARAMETER		TEST CONDITIONS	V_{CC}(V)	25℃			–40℃ to 85℃		–55℃ to 125℃		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
t_w	$\overline{CP}$ pulse width	–C_L = 50 pF	2	80			100		120		ns
			4.5	16			20		24		
			6	14			17		20		
t_w	$\overline{R}$ pulse width	–C_L = 50 pF	2	80			100		120		ns
			4.5	16			20		24		
			6	14			17		20		
t_{SU}	Setup time, J, K to $\overline{CP}$	C_L = 50 pF	2	80			100		120		ns
			4.5	16			20		24		
			6	14			17		20		
t_H	Hold time, J, K to $\overline{CP}$	C_L = 50 pF	2	3			3		3		ns
			4.5	3			3		3		
			6	3			3		3		
t_{REM}	Removal time	–C_L = 50 pF	2	80			100		120		ns
			4.5	16			20		24		
			6	14			17		20		
f_{MAX}	$\overline{CP}$ frequency	C_L = 50 pF	2	6			5		4		MHz
			4.5	30			25		20		
		C_L = 15 pF	5		60						
		C_L = 50 pF	6	35			29		23		
HCT TYPES											
t_w	$\overline{CP}$ pulse width	C_L = 50 pF	4.5	16			20		24		ns
t_w	$\overline{R}$ pulse width	C_L = 50 pF	4.5	18			23		27		ns
t_{SU}	Setup time, J, K to $\overline{CP}$	C_L = 50 pF	4.5	16			20		24		ns
t_H	Hold time, J, K to $\overline{CP}$	C_L = 50 pF	4.5	3			3		3		ns
t_{REM}	Removal time	C_L = 50 pF	4.5	12			15		18		ns
f_{MAX}	$\overline{CP}$ frequency	C_L = 50 pF	4.5	30			25		20		MHz
		C_L = 15 pF	5		60						

5.6 Switching Specifications

Input, t_r, t_f = 6 ns

PARAMETER		TEST CONDITIONS	V_{CC} (V)	25℃			–40℃ to 85℃		–55℃ to 125℃		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
t_{PLH}, t_{PHL}	Propagation delay, $\overline{CP}$ to Q	C_L = 50 pF	2			160		200		240	ns
			4.5			32		40		48	
		C_L = 15 pF	5		13						
		C_L = 50 pF	6			28		34		41	
t_{PLH}, t_{PHL}	Propagation delay, $\overline{CP}$ to $\overline{Q}$	C_L = 50 pF	2			160		200		240	ns
			4.5			32		40		48	
		C_L = 15 pF	5		13						
		C_L = 50 pF	6			28		34		41	
t_{PLH}, t_{PHL}	Propagation delay, $\overline{R}$ to Q, $\overline{Q}$	C_L = 50 pF	2			145		180		220	ns
			4.5			29		36		44	
		C_L = 15 pF	5		12						
		C_L = 50 pF	6			25		31		38	
t_{TLH}, t_{THL}	Output transition time	C_L = 50 pF	2			75		95	18	110	ns
			4.5			15		19		22	
			6			13		16		19	
C_I	Input capacitance					10		10		10	pF
C_{PD}	Power dissipation capacitance(1) (2)		5		28						pF
HCT TYPES											
t_{PLH}, t_{PHL}	Propagation delay, $\overline{CP}$ to Q	C_L = 50 pF	4.5			38		48		57	ns
t_{PLH}, t_{PHL}	Propagation delay, $\overline{CP}$ to $\overline{Q}$	C_L = 50 pF	4.5			36		45		54	ns
t_{PLH}, t_{PHL}	Propagation delay, $\overline{R}$ to Q, $\overline{Q}$	C_L = 50 pF	4.5			34		43		51	ns
t_{TLH}, t_{THL}	Output transition time	C_L = 50 pF	4.5			15		19		22	ns
C_I	Input capacitance					10		10		10	pF
C_{PD}	Power dissipation capacitance(1) (2)		5		28						pF

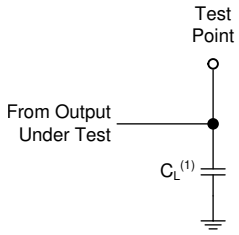
(1) C_{PD} is used to determine the dynamic power consumption, per flip-flop.
(2) $P_D = C_{PD} V_{CC}{}^2 f_i + \sum C_L V_{CC}{}^2 f_o$ where f_i = input frequency, f_o = output frequency, C_L = output load capacitance, V_{CC} = supply voltage.

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_t < 2.5 ns.

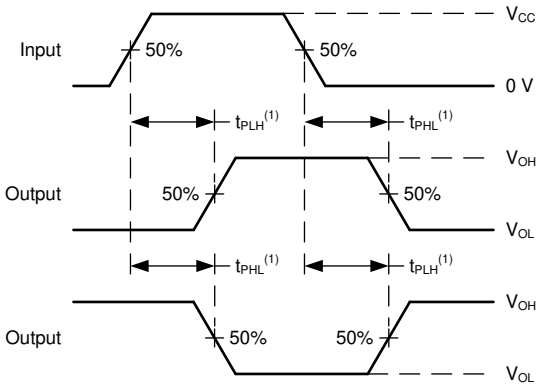
For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



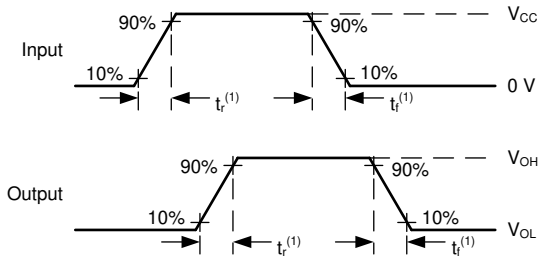
(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for Push-Pull Outputs



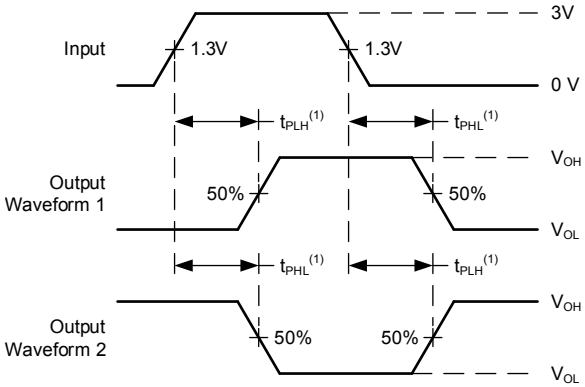
(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 6-2. Voltage Waveforms, Propagation Delays for Standard CMOS Inputs



(1) The greater between t_r and t_f is the same as t_t.

Figure 6-3. Voltage Waveforms, Input and Output Transition Times for Standard CMOS Inputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 6-4. Voltage Waveforms, Propagation Delays for TTL-Compatible Inputs

7 Detailed Description

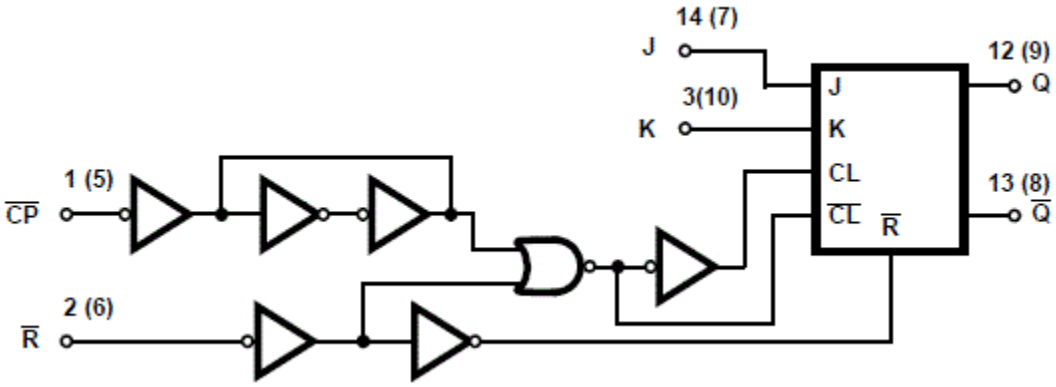
7.1 Overview

The ’HC73 and CD74HCT73 utilize silicon gate CMOS technology to achieve operating speeds equivalent to LSTTL parts. They exhibit the low power consumption of standard CMOS integrated circuits, together with the ability to drive 10 LSTTL loads

These flip-flops have independent J, K, Reset and Clock inputs and Q and $\overline{Q}$ outputs. They change state on the negative-going transition of the clock pulse. Reset is accomplished asynchronously by a low level input. This device is functionally identical to the HC/HCT107 but differs in terminal assignment and in some parametric limits.

The HCT logic family is functionally as well as pin compatible with the standard LS logic family

7.2 Functional Block Diagram



7.3 Device Functional Modes

Table 7-1. Truth Table(1)

INPUTS				OUTPUTS	
R	$\overline{CP}$	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	No change	
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	X	X	No change	

(1) H = high level (steady state), L = low level (steady state), X = irrelevant, ↓ = high-to-low transition

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.3 Trademarks

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10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8515301CA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8515301CA CD54HC73F3A	Samples
CD54HC73F	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54HC73F	Samples
CD54HC73F3A	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8515301CA CD54HC73F3A	Samples
CD74HC73E	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC73E	Samples
CD74HC73M96	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	HC73M	Samples
CD74HC73MT	ACTIVE	SOIC	D	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC73M	Samples
CD74HCT73E	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT73E	Samples
CD74HCT73M	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT73M	Samples
CD74HCT73M96	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCT73M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF CD54HC73, CD74HC73 :

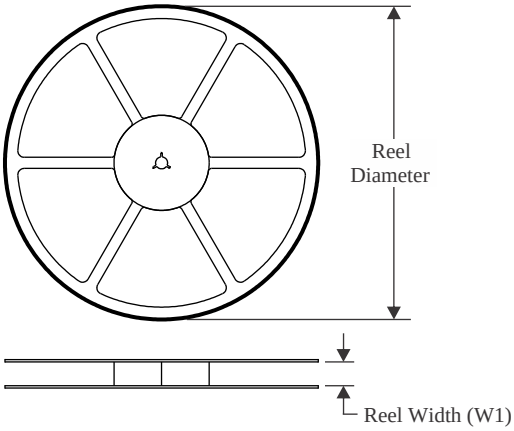
- Catalog : CD74HC73
- Military : CD54HC73

NOTE: Qualified Version Definitions:

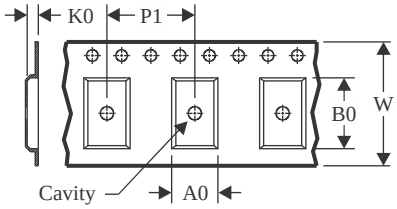
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

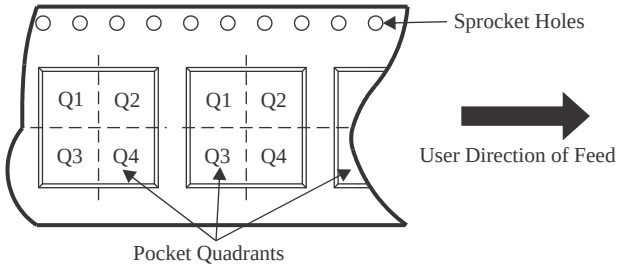


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

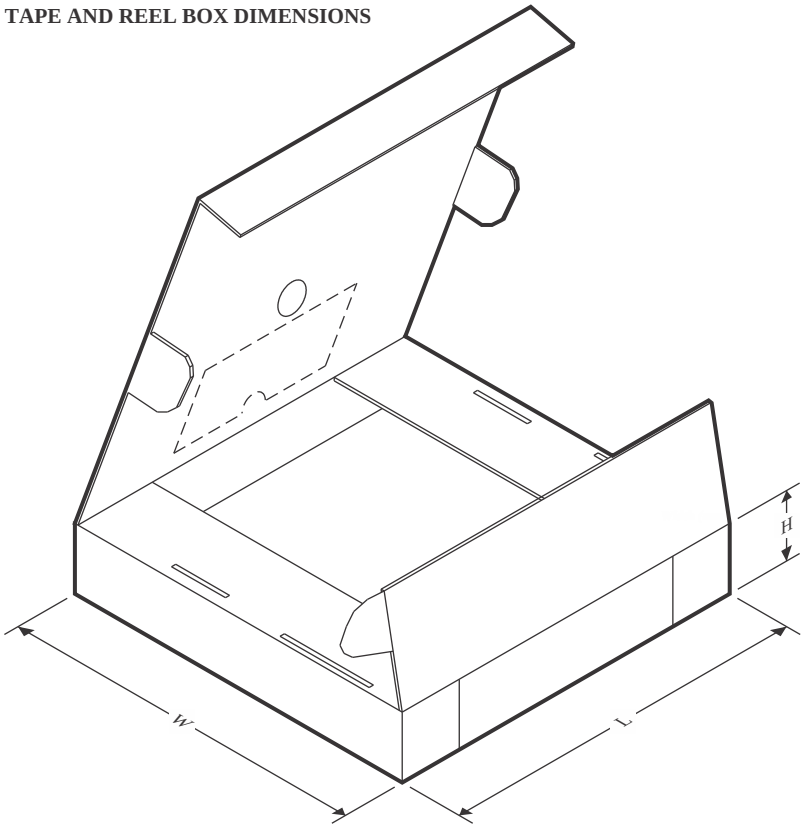
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC73M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HC73M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HC73MT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HCT73M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

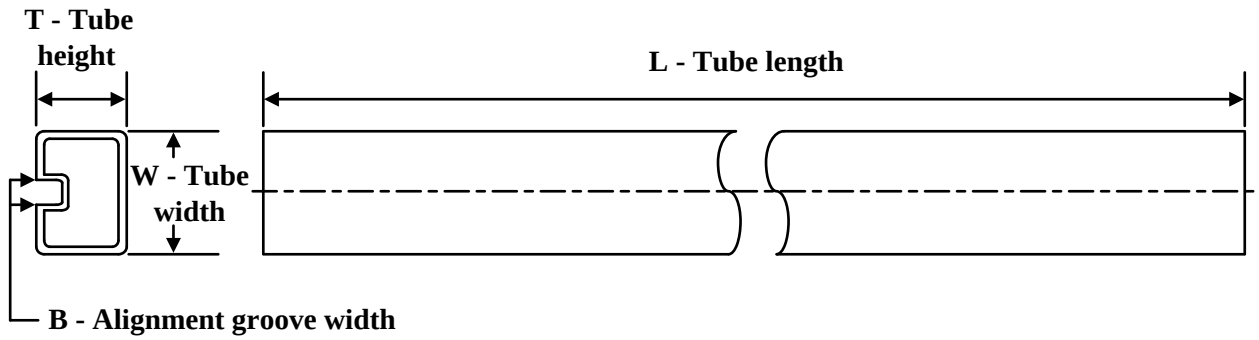
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC73M96	SOIC	D	14	2500	356.0	356.0	35.0
CD74HC73M96	SOIC	D	14	2500	356.0	356.0	35.0
CD74HC73MT	SOIC	D	14	250	210.0	185.0	35.0
CD74HCT73M96	SOIC	D	14	2500	356.0	356.0	35.0

TUBE



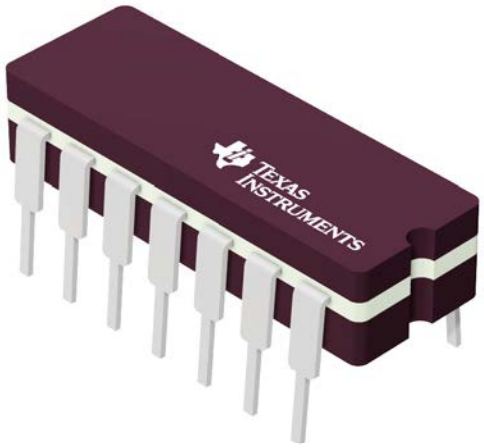
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HC73E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT73E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT73E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT73M	D	SOIC	14	50	506.6	8	3940	4.32

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

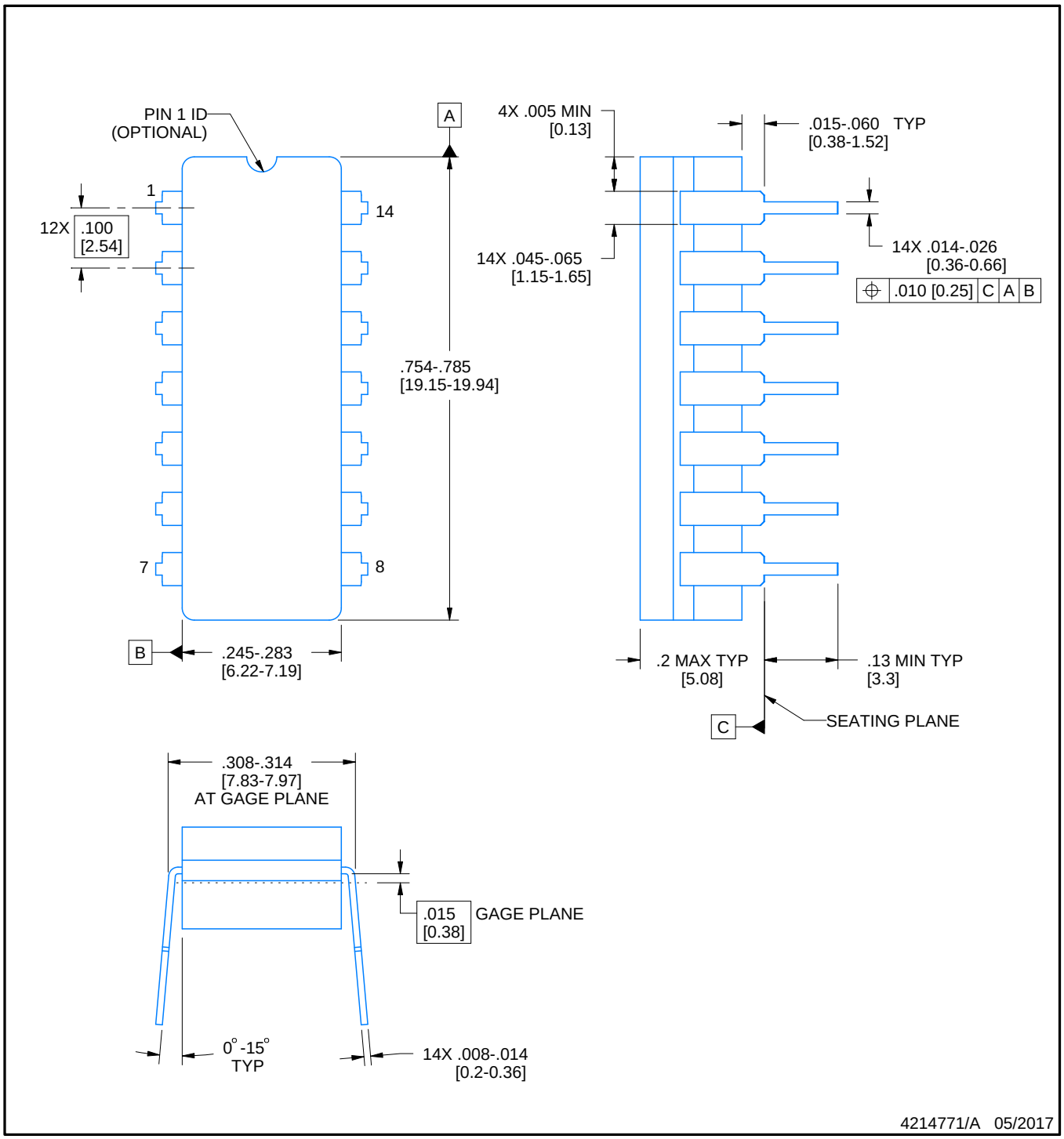
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

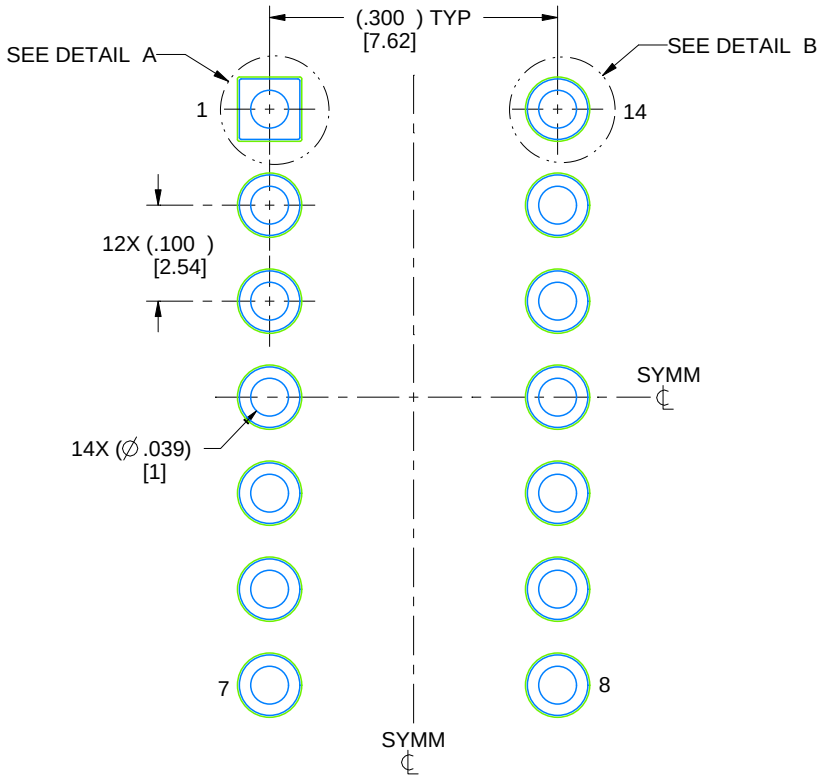
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

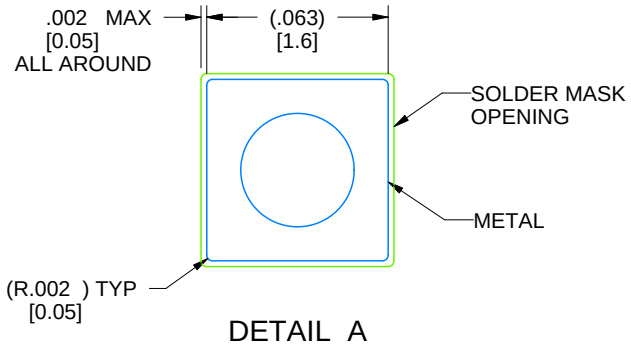
J0014A

CDIP - 5.08 mm max height

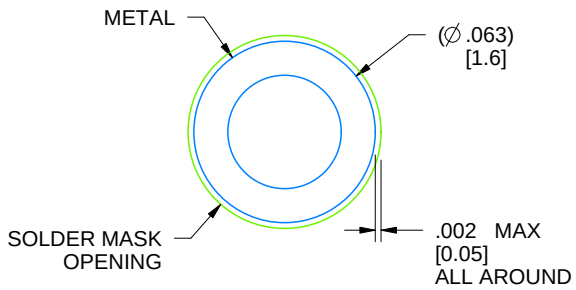
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



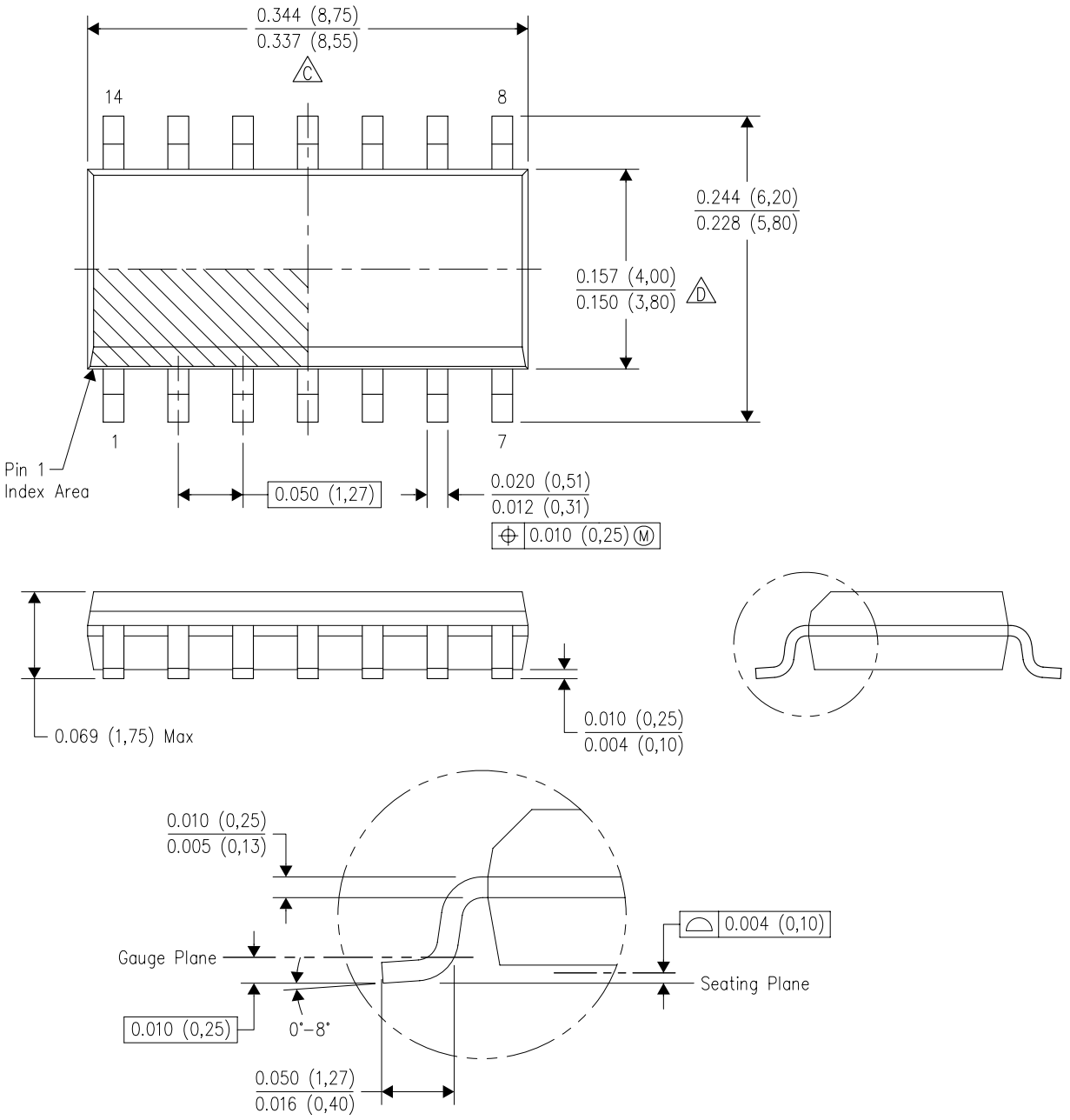
DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

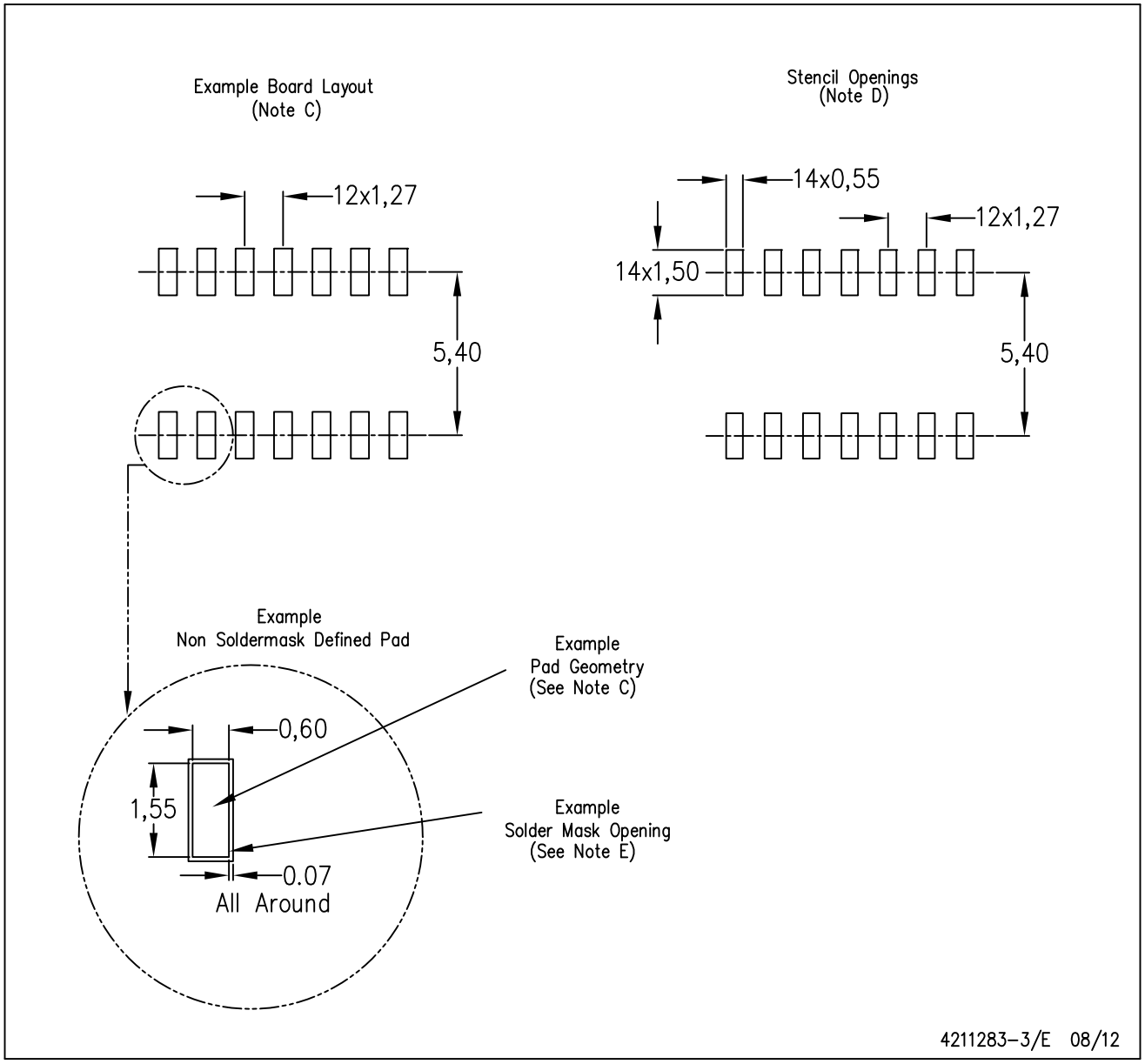
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE

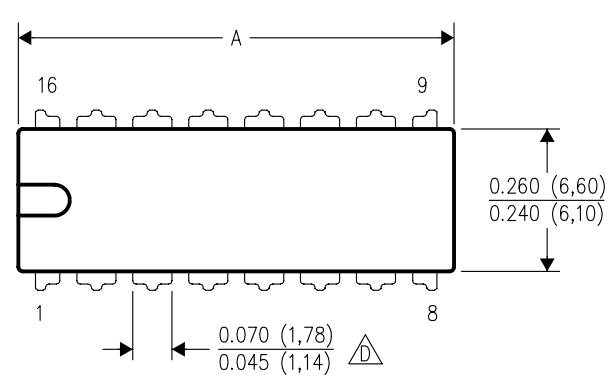


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

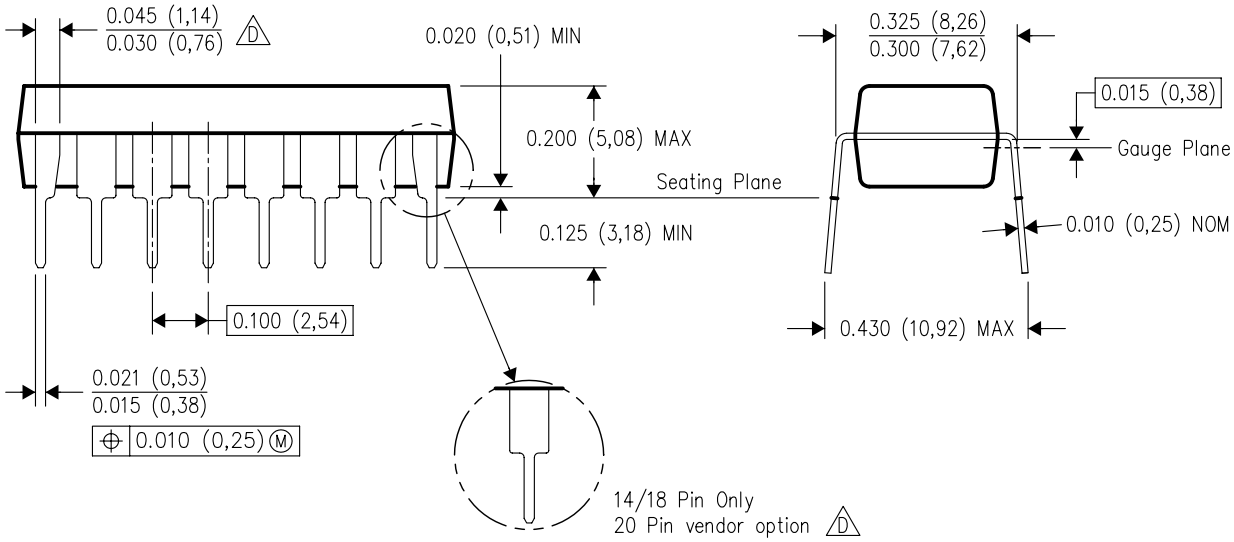
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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