LMH6657 and LMH6658 270-MHz Single Supply, Single and Dual Amplifiers

1 Features

V_S = 5 V, T_A = 25°C, R_L = 100 Ω (Typical Values Unless Specified)

- −3dB BW (A_V = +1) 270 MHz
- Supply Voltage Range 3 V to 12 V
- Slew Rate, (V_S = ±5 V) 700 V/µs
- Supply Current 6.2 mA/amp
- Output Current +80/−90 mA
- Input Common-Mode Volt. 0.5 V Beyond V^-, 1.7 V from V^+
- Output Voltage Swing (R_L = 2 kΩ) 0.8 V from Rails
- Input Voltage Noise 11 nV/√Hz
- Input Current Noise 2.1 pA√Hz/
- DG Error 0.03%
- DP Error 0.10°
- THD (5MHz) −55 dBc
- Settling Time (0.1%) 37ns
- Fully Characterized for 5 V, and ±5 V
- Output Overdrive Recovery 18 ns
- Output Short Circuit Protected(1)
- No Output Phase Reversal With CMVR Exceeded

2 Applications

- CD/DVD ROM
- ADC Buffer Amps
- Portable Video
- Current Sense Buffers
- Portable Communications

(1) Short Circuit Test is a momentary test. See Note 3 under *Absolute Maximum Ratings*.

3 Description

The LMH6657 and LMH6658 devices are low-cost operational amplifiers that operate from a single supply with input voltage range extending below the V^-. Based on easy to use voltage feedback topology and boasting fast slew rate (700 V/µs) and high speed (140 MHz GBWP), the LMH6657 (Single) and LMH6658 (dual) can be used in high speed large signal applications. These applications include instrumentation, communication devices, set-top boxes, and so forth.

With a -3dB BW of 100 MHz (A_V = +2) and DG & DP of 0.03% & 0.10° respectively, the LMH6657 and LMH6658 are well suited for video applications. The output stage can typically supply 80 mA into the load with a swing of about 1 V from either rail.

For Industrial applications, the LMH6657 and LMH6658 are excellent cost-saving choices. Input referred voltage noise is low and the input voltage can extend below V^- to ease amplification of low level signals that could be at or near the system ground. With low distortion and fast settling, LMH6657 and LMH6658 can provide buffering for A/D and D/A applications.

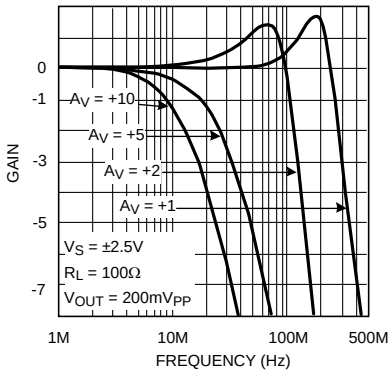
The LMH6657 and LMH6658 versatility and ease of use is extended even further by offering these high slew rate, high-speed operational amplifiers in miniature packages such as SOT-23-5, SC70, SOIC-8, and VSSOP-8.

Device Information(1)

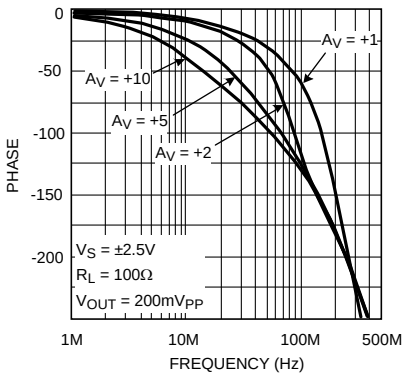
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMH6657	SC70 (5)	2.00 mm × 1.25 mm
	SOT-23 (5)	2.90 mm × 1.60 mm
LMH6658	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Noninverting Frequency Response, Gain



Noninverting Frequency Response, Phase



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (April 2013) to Revision G **Page**

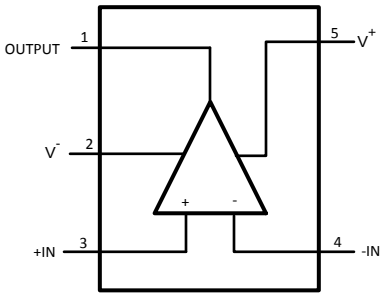
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision E (March 2013) to Revision F **Page**

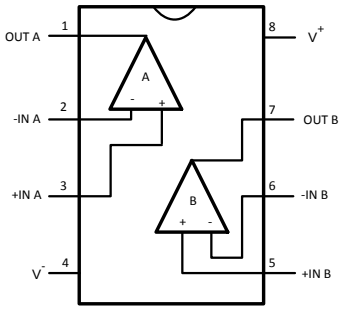
- Changed layout of National Data Sheet to TI format ... 1

5 Pin Configuration and Functions

DBV and DCK Package
5-Pin SOT-23 and SC70
Top View



D and DGK Package
8-Pin SOIC and VSSOP
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	SOT-23 AND SC70	SOIC AND VSSOP		
OUTPUT	1	—	O	Output
–IN	4	—	I	Inverting input
+IN	3	—	I	Noninverting input
OUT A	—	1	O	Output A
–IN A	—	2	I	Inverting input A
+IN A	—	3	I	Noninverting input A
V^-	2	4	I	Negative Supply
OUT B	—	7	O	Output B
–IN B	—	6	I	Inverting input channel B
+IN B	—	5	I	Noninverting input channel B
V^+	5	8	I	Positive supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN} Differential			±2.5	V
Output Short Circuit Duration			See (2)(3)	
Input Current			±10	mA
Supply Voltage (V^+ - V^-)			12.6	V
Voltage at Input/Output pins		V^- − 0.8	V^+ + 0.8	V
Soldering Information	Infrared or Convection (20 sec.)		260	°C
	Wave Soldering (10 sec.)		260	
Storage temperature, T_{stg}		–65	100	°C
Junction Temperature(4)			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(3) Output short circuit duration is infinite for V_S < 6 V at room temperature and below. For V_S > 6 V, allowable short circuit duration is 1.5ms.
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)(2)	±2000	V
		Machine Model(3)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(2) Human body model, 1.5 kΩ in series with 100 pF.
(3) Machine Model, 0 Ω in series with 200 pF.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply Voltage (V^+ – V^-)	3	12	V
Operating Temperature(1)	−40	85	°C

(1) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

6.4 Thermal Information

THERMAL METRIC(1)		LMH6657		LMH6658		UNIT
		DBV (SOT-23)	DCK (SC70)	D (SOIC)	DGK (VSSOP)	
		5 PINS		8 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	265	478	190	235	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

6.5 Electrical Characteristics, 5 V

Unless otherwise specified, all limits ensured for at T_J = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = V_O = $V^+/2$, and R_L = 100Ω (or as specified) tied to $V^+/2$.

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
GB	Gain Bandwidth Product	V_{OUT} < 200 mV_{PP}			140		MHz
SSBW	−3-dB BW	A_V = +1, V_{OUT} = 200 mV_{PP}		220	270		MHz
		A_V = +2 or −1, V_{OUT} = 200 mV_{PP}			100		
GFP	Frequency Response Peaking	A_V = +2, V_{OUT} = 200 mV_{PP}, DC to 100 MHz			1.5		dB
GFR	Frequency Response Rolloff	A_V = +2, V_{OUT} = 200 mV_{PP}, DC to 100 MHz			0.5		dB
$LPD_{1°}$	1° Linear Phase Deviation	A_V = +2, V_{OUT} = 200 mV_{PP}, ±1°			30		MHz
$GF_{0.1dB}$	0.1-dB Gain Flatness	A_V = +2, ±0.1 dB, V_{OUT} = 200 mV_{PP}			13		MHz
PBW	Full Power Bandwidth	−1 dB, V_{OUT} = 3 V_{PP}, A_V = −1			55		MHz
DG	Differential Gain	NTSC, V_{CM} = 2 V, R_L = 150 Ω to $V^+/2$, Pos. Video Only			0.03%		
DP	Differential Phase	NTSC, V_{CM} = 2 V, R_L=150 Ω to $V^+/2$ Pos. Video Only			0.1		deg
TIME DOMAIN RESPONSE							
t_r	Rise and Fall Time	A_V = +2, V_{OUT} = 500 mV_{PP}			3.3		ns
		A_V = −1, V_{OUT} = 500 mV_{PP}			3.4		
OS	Overshoot, Undershoot	A_V = +2, V_{OUT} = 500 mV_{PP}			18%		
t_s	Settling Time	V_O = 2 V_{PP}, ±0.1%, R_L = 500 Ω to $V^+/2$, A_V = −1			37		ns
SR	Slew Rate(3)	A_V = −1, V_O = $3V_{PP}$(4)			470		V/µs
		A_V = +2, V_O = $3V_{PP}$(4)			420		
DISTORTION AND NOISE RESPONSE							
HD2	2^{nd} Harmonic Distortion	f = 5MHz, V_O = $2V_{PP}$, A_V = -1			−70		dBc
HD3	3^{rd} Harmonic Distortion	f = 5MHz, V_O = $2V_{PP}$, A_V = -1			−57		dBc
THD	Total Harmonic Distortion	f = 5MHz, V_O = $2V_{PP}$, A_V = -1			−55.5		dBc
V_n	Input-Referred Voltage Noise	f = 100KHz			11		nV/√Hz
		f = 1KHz			19		
I_n	Input-Referred Current Noise	f = 100KHz			2.1		pA/√Hz
		f = 1KHz			7.5		
XTLKA	Cross-Talk Rejection (LMH6658)	f = 5MHz, R_L (SND) = 100Ω RCV: R_F = R_G = 1k			69		dB
STATIC, DC PERFORMANCE							
A_{VOL}	Large Signal Voltage Gain	V_O = 1.25V to 3.75V, R_L = 2k to $V^+/2$		85	95		dB
		V_O = 1.5V to 3.5V, R_L = 150Ω to $V^+/2$		75	85		
		V_O = 2V to 3V, R_L = 50Ω to $V^+/2$		70	80		
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 50dB		−0.2	−0.5		V
			At the temperature extremes	−0.1			
				3	3.3		
			At the temperature extremes	2.8			
V_{OS}	Input Offset Voltage				±1.1	±5	mV
		At the temperature extremes				±7	
TC V_{OS}	Input Offset Voltage Average Drift	See(5)			±2		µV/C

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Slew rate is the "worst case" of the rising and falling slew rates.
(4) Output Swing not limited by Slew Rate limit.
(5) Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.

Electrical Characteristics, 5 V (continued)

Unless otherwise specified, all limits ensured for at T_J = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = V_O = V^+/2, and R_L = 100Ω (or as specified) tied to V^+/2.

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
I_B	Input Bias Current	See(6)			−5	−20	µA
			At the temperature extremes			−30	
TC $_{IB}$	Input Bias Current Average Drift	See(5)			0.01		nA/°C
I_{OS}	Input Offset Current				50	300	nA
		At the temperature extremes				500	
CMRR	Common-Mode Rejection Ratio	V_{CM} Stepped from 0V to 3.0V		72	82		dB
+PSRR	Positive Power Supply Rejection Ratio	V^+ = 4.5V to 5.5V, V_{CM} = 1V		72	82		dB
I_S	Supply Current (per channel)	No load			6.2	8.5	mA
			At the temperature extremes			10	
MISCELLANEOUS PERFORMANCE							
V_{OH}	Output Swing High	R_L = 2k to V^+/2		4.1	4.25		V
			At the temperature extremes	3.8			
		R_L = 150Ω to V^+/2		4	4.19		
			At the temperature extremes	3.7			
		R_L = 75Ω to V^+/2		3.85	4.15		
			At the temperature extremes	3.5			
V_{OL}	Output Swing Low	R_L = 2k to V^+/2		900	800		mV
			At the temperature extremes	1100			
		R_L = 150Ω to V^+/2		970	870		
			At the temperature extremes	1200			
		R_L = 75Ω to V^+/2		990	885		
			At the temperature extremes	1250			
I_{OUT}	Output Current	V_{OUT} = 1V from either rail	Sourcing	40	85		mA
			Sinking	–40	105		
I_{SC}	Output Short CircuitCurrent(7)	Sourcing to V^+/2		100	155		mA
			At the temperature extremes	80			
		Sinking to V^+/2		100	220		
			At the temperature extremes	80			
R_{IN}	Common-Mode Input Resistance				3		MΩ
C_{IN}	Common-Mode Input Capacitance				1.8		pF
R_{OUT}	Output Impedance	f = 1MHz, A_V = +1			0.06		Ω

(6) Positive current corresponds to current flowing into the device.
(7) Short circuit test is a momentary test. See Note 3 under *Absolute Maximum Ratings*.

6.6 Electrical Characteristics, ±5 V

Unless otherwise specified, all limits ensured for at T_J = 25°C, V^+ = 5 V, V^- = −5 V, V_{CM} = V_O, and R_L = 100 Ω (or as specified) tied to 0 V.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
GB	Gain Bandwidth Product	V_{OUT} < 200 mV_{PP}		140		MHz
SSBW	−3-dB BW	A_V = +1, V_{OUT} = 200 mV_{PP}	220	270		MHz
		A_V = +2 or −1, V_{OUT} = 200 mV_{PP}		100		
GFP	Frequency Response Peaking	A_V = +2, V_{OUT} = 200 mV_{PP}, DC to 100 MHz		1		dB
GFR	Frequency Response Rolloff	A_V = +2, V_{OUT} = 200 mV_{PP}, DC to 100 MHz		0.9		dB
$LPD_{1°}$	1° Linear Phase Deviation	A_V = +2, V_{OUT} = 200mV_{PP}, ±1°		30		MHz
$GF_{0.1dB}$	0.1-dB Gain Flatness	A_V = +2, ±0.1 dB, V_{OUT} = 200 mV_{PP}		20		MHz
PBW	Full Power Bandwidth	−1 dB, V_{OUT} = 8 V_{PP}, A_V = −1		30		MHz
DG	Differential Gain	NTSC, R_L = 150 Ω, Pos. or Neg. Video		0.03%		
DP	Differential Phase	NTSC,R_L = 150 Ω, Pos. or Neg. Video		0.1		deg
TIME DOMAIN RESPONSE						
t_r	Rise and Fall Time	A_V = +2, V_{OUT} = 500 mV_{PP}		3.3		ns
		A_V = −1, V_{OUT} = 500 mV_{PP}		3.3		
OS	Overshoot, Undershoot	A_V = +2, V_{OUT} = 500 mV_{PP}		16%		
t_s	Settling Time	V_O = 5 V_{PP}, ±0.1%, R_L =500 Ω, A_V = −1		35		ns
SR	Slew Rate(3)	A_V = −1, V_O = 8 V_{PP}		700		V/µs
		A_V = +2, V_O = 8 V_{PP}		500		
DISTORTION AND NOISE RESPONSE						
HD2	2nd Harmonic Distortion	f = 5 MHz, V_O = 2 V_{PP}, A_V = -1		−70		dBc
HD3	3rd Harmonic Distortion	f = 5 MHz, V_O = 2 V_{PP}, A_V = -1		−57		dBc
THD	Total Harmonic Distortion	f = 5 MHz, V_O = 2 V_{PP}, A_V = -1		−55.5		dBc
V_n	Input-Referred Voltage Noise	f = 100 KHz		11		nV/√Hz
		f = 1 KHz		19		
I_n	Input-Referred Current Noise	f = 100 KHz		2.1		pA/√Hz
		f = 1 KHz		7.5		
XTLKA	Cross-Talk Rejection (LMH6658)	f = 5 MHz, R_L (SND) = 100 Ω RCV: R_F = R_G = 1 k		69		dB
STATIC, DC PERFORMANCE						
A_{VOL}	Large Signal Voltage Gain	V_O = −3.75 V to 3.75 V, R_L = 2 k	87	100		dB
		V_O = −3.5 V to 3.5 V, R_L = 150 Ω	80	90		
		V_O = −3 V to 3 V, R_L = 50 Ω	75	85		
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 50 dB	−5.2	−5.5		V
		At the temperature extremes	−5.1			
			3	3.3		
		At the temperature extremes	2.8			
V_{OS}	Input Offset Voltage			±1	±5	mV
		Apply at the temperature extremes			±7	
TC V_{OS}	Input Offset Voltage Average Drift	See (4)		±2		µV/C

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Slew rate is the "worst case" of the rising and falling slew rates.
(4) Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.

Electrical Characteristics, ±5 V (continued)

Unless otherwise specified, all limits ensured for at T_J = 25°C, V^+ = 5 V, V^- = −5 V, V_{CM} = V_O, and R_L = 100 Ω (or as specified) tied to 0 V.

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
I_B	Input Bias Current	See (5)			−5	−20	µA
			At the temperature extremes			−30	
TC_{IB}	Input Bias Current Average Drift	See (4)			0.01		nA/°C
I_{OS}	Input Offset Current				50	300	nA
		At the temperature extremes				500	
CMRR	Common-Mode Rejection Ratio	V_{CM} Stepped from −5 V to 3 V		75	84		dB
+PSRR	Positive Power Supply Rejection Ratio	V^+ = 4.5 V to 5.5 V, V_{CM} = −4 V		75	82		dB
−PSRR	Negative Power Supply Rejection Ratio	V^- = −4.5 V to −5.5 V		78	85		dB
I_S	Supply Current (per channel)	No load			6.5	9	mA
			At the temperature extremes			11	
MISCELLANEOUS PERFORMANCE							
V_{OH}	Output Swing High	R_L = 2 k		4.1	4.25		V
			At the temperature extremes	3.8			
		R_L = 150 Ω		4	4.2		
			At the temperature extremes	3.7			
		R_L = 75 Ω		3.85	4.18		
			At the temperature extremes	3.5			
V_{OL}	Output Swing Low	R_L = 2 k		−4.05	−4.19		V
			At the temperature extremes	−3.8			
		R_L = 150 Ω		−3.9	−4.05		
			At the temperature extremes	−3.65			
		R_L = 75 Ω		−3.8	−4		
			At the temperature extremes	−3.5			
I_{OUT}	Output Current	V_{OUT} = 1 V from either rail	Sourcing	45	100		mA
			Sinking	–45	–110		
I_{SC}	Output Short Circuit Current(6)	Sourcing to Ground		120	180		mA
			At the temperature extremes	100			
		Sinking to Ground		120	230		
			At the temperature extremes	100			
R_{IN}	Common-Mode Input Resistance				4		MΩ
C_{IN}	Common-Mode Input Capacitance				1.8		pF
R_{OUT}	Output Impedance	f = 1 MHz, A_V = +1			0.06		Ω

(5) Positive current corresponds to current flowing into the device.
(6) Short circuit test is a momentary test. See Note 3 under *Absolute Maximum Ratings*.

6.7 Typical Characteristics

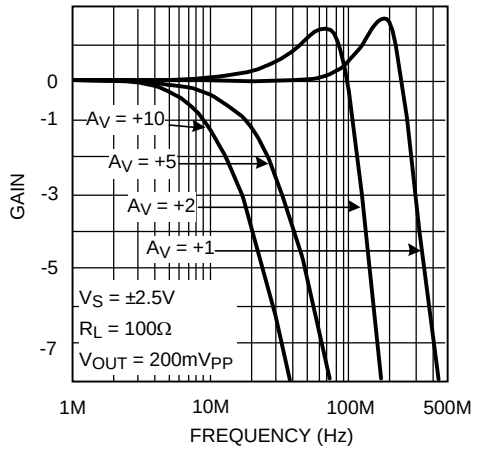


Figure 1. Noninverting Frequency Response, Gain

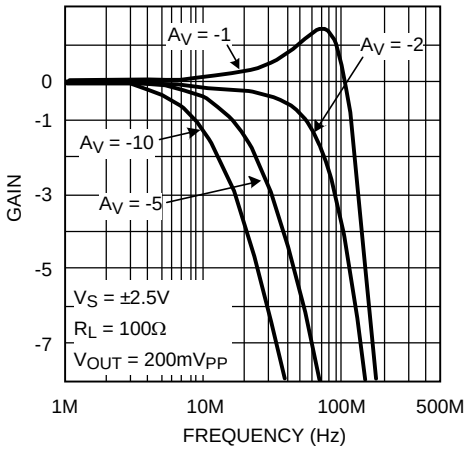


Figure 2. Inverting Frequency Response, Gain

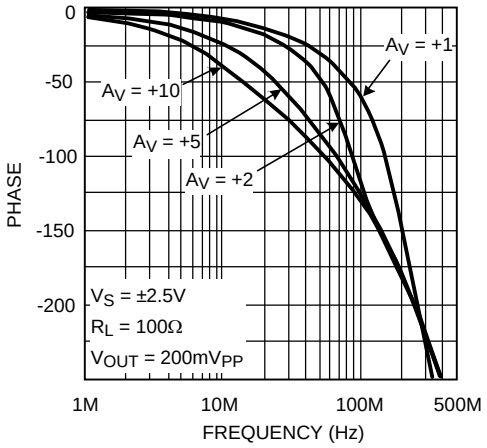


Figure 3. Noninverting Frequency Response, Phase

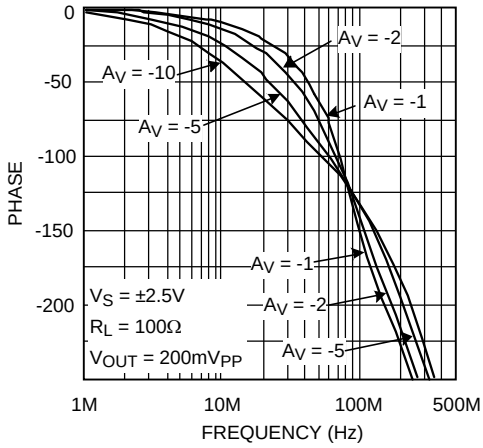


Figure 4. Inverting Frequency Response, Phase

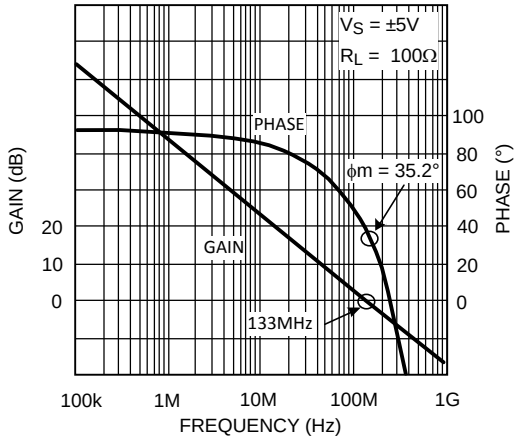


Figure 5. Open Loop Gain/Phase vs. Frequency

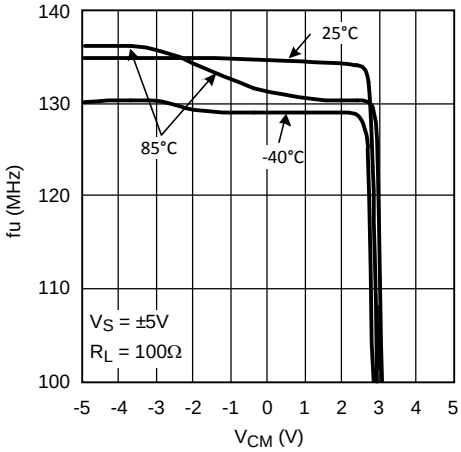


Figure 6. Unity Gain Frequency vs. V_{CM}

Typical Characteristics (continued)

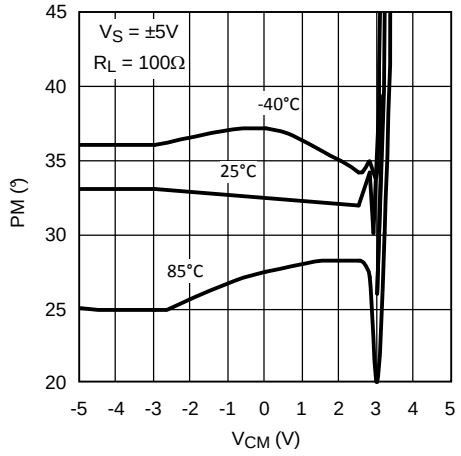


Figure 7. Phase Margin vs. V_{CM}

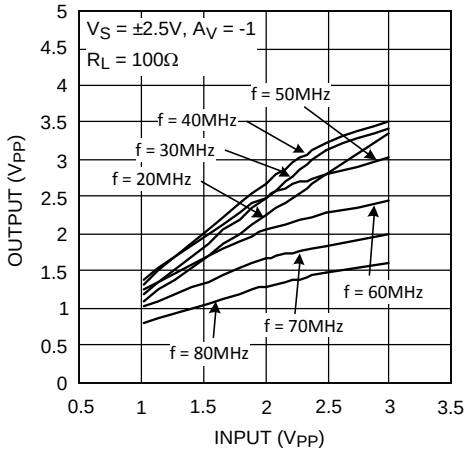


Figure 8. Output vs. Input

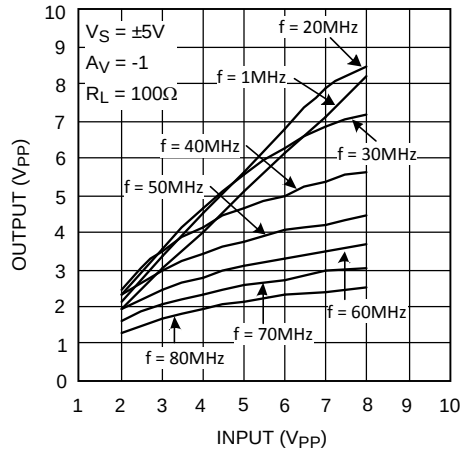


Figure 9. Output vs. Input

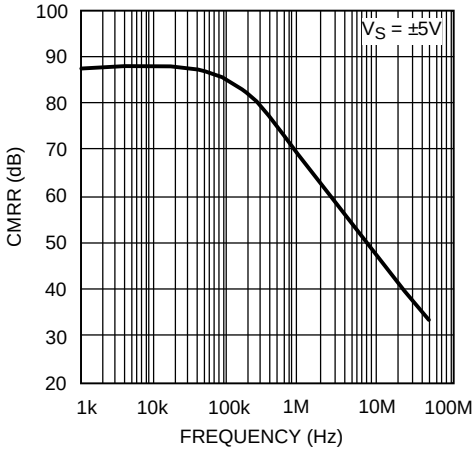


Figure 10. CMRR vs. Frequency

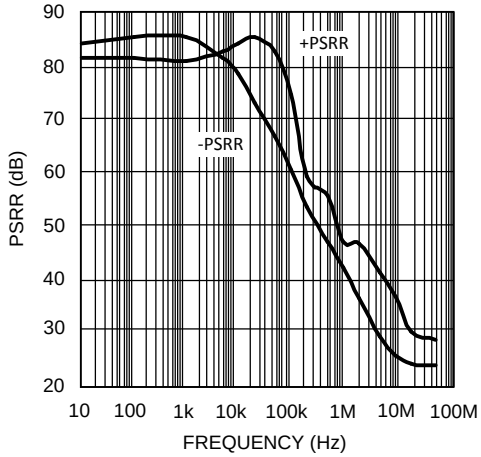


Figure 11. PSRR vs. Frequency

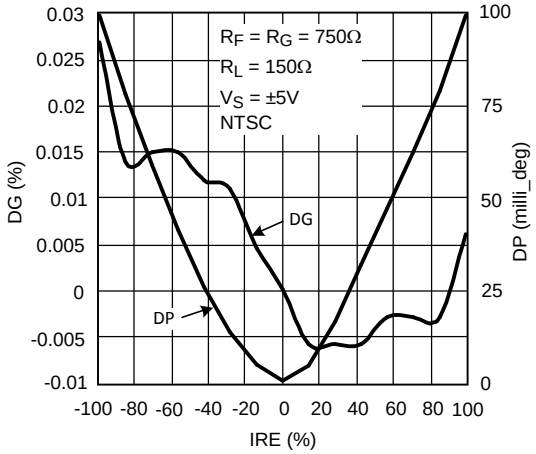


Figure 12. DG/DP vs. IRE

Typical Characteristics (continued)

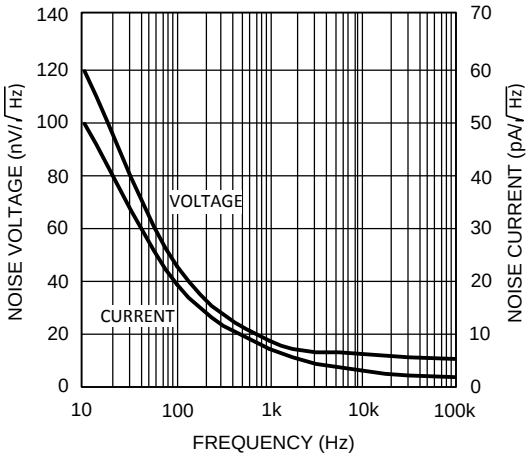


Figure 13. Noise vs. Frequency

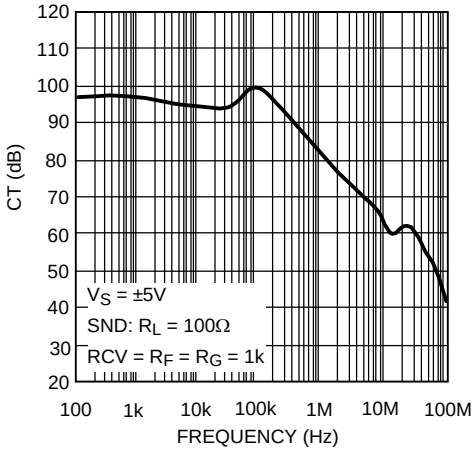


Figure 14. Crosstalk Rejection vs. Frequency

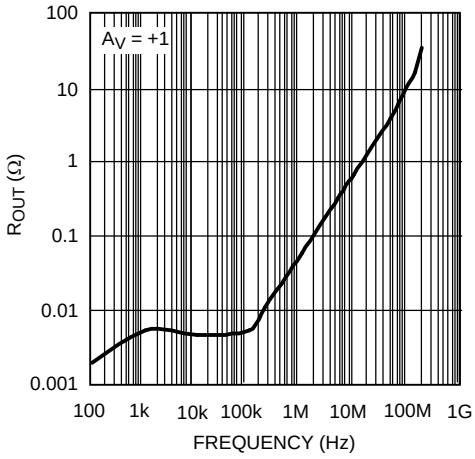


Figure 15. Output Impedance vs. Frequency

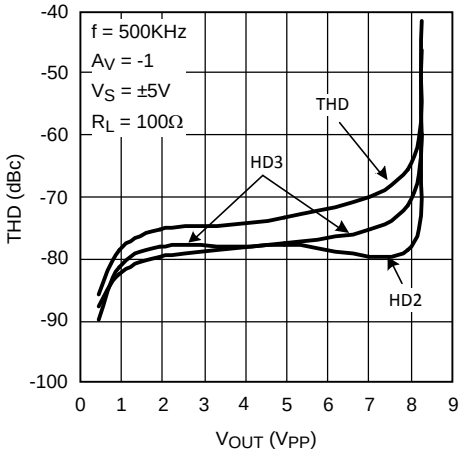


Figure 16. HD vs. V_{OUT}

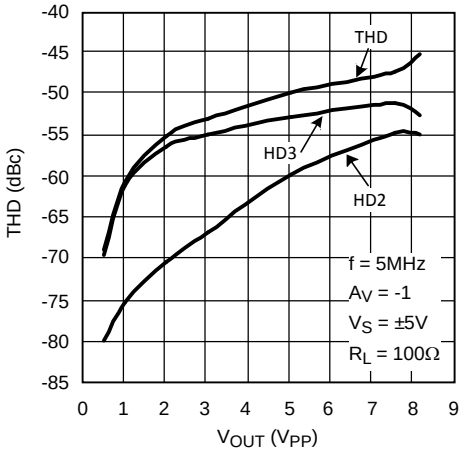


Figure 17. HD vs. V_{OUT}

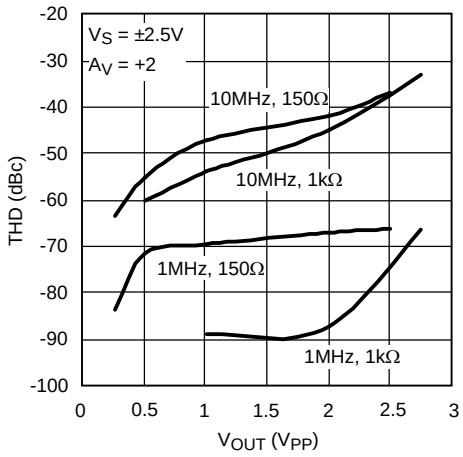


Figure 18. THD vs. V_{OUT}

Typical Characteristics (continued)

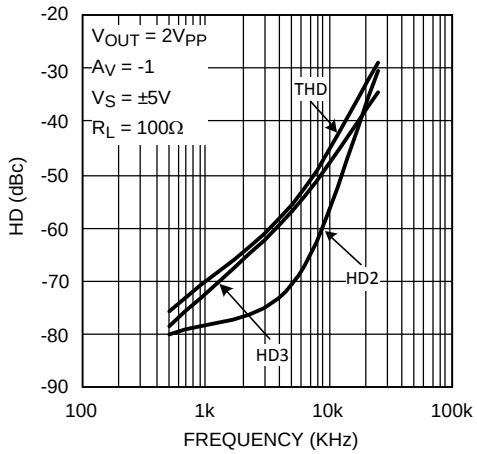


Figure 19. HD vs. Frequency

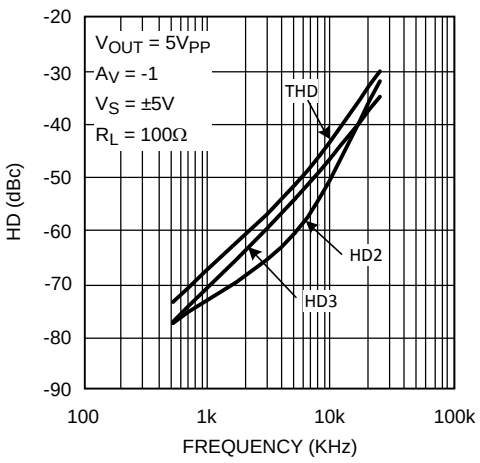


Figure 20. HD vs. Frequency

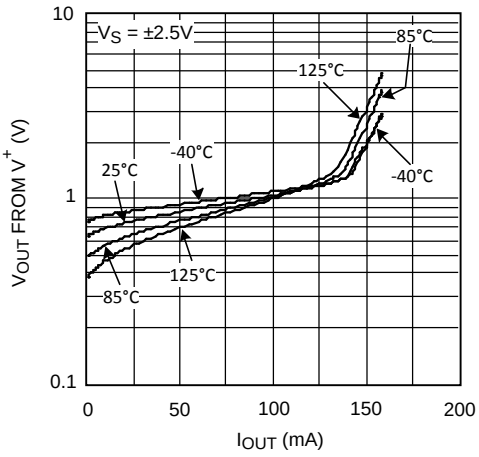


Figure 21. V_{OUT} vs. I_{SOURCE}

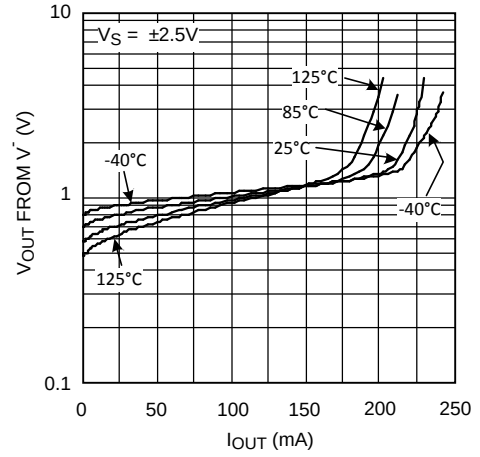


Figure 22. V_{OUT} vs. I_{SINK}

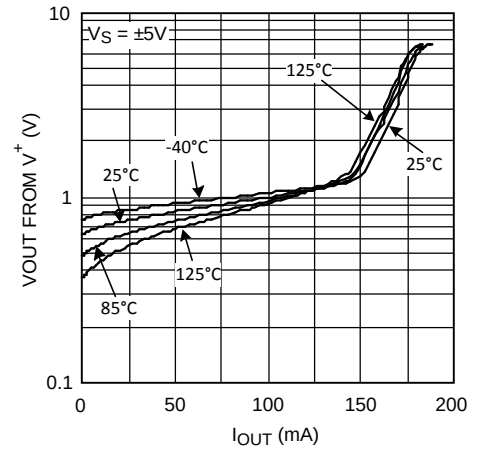


Figure 23. V_{OUT} vs. I_{SOURCE}

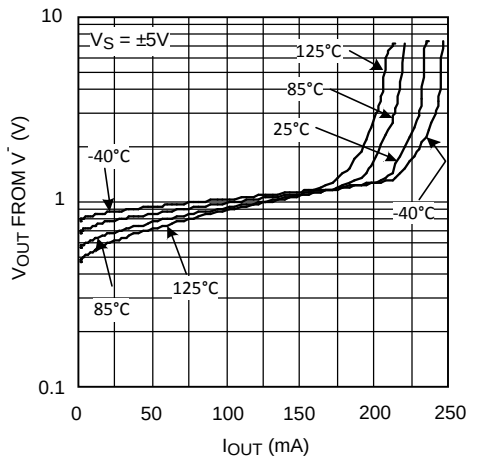


Figure 24. V_{OUT} vs. I_{SINK}

Typical Characteristics (continued)

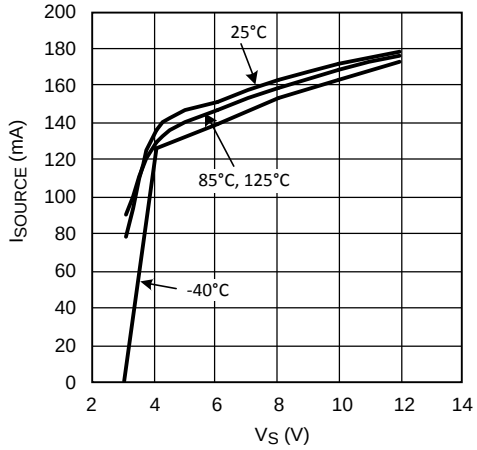


Figure 25. Short Circuit Current

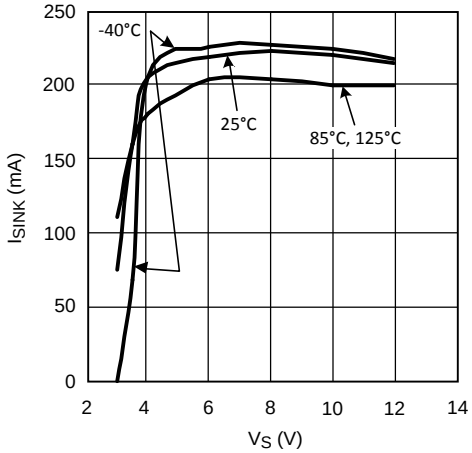


Figure 26. Short Circuit Current

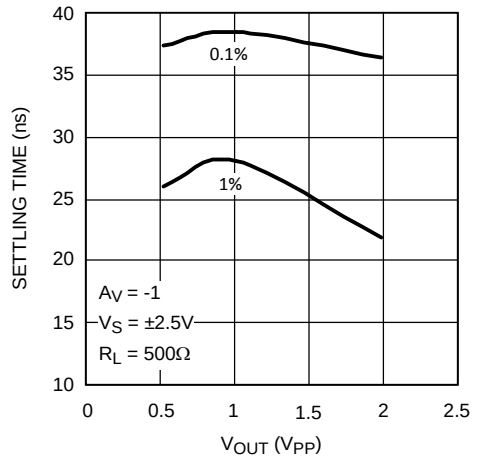


Figure 27. Settling Time vs. Output Step Amplitude

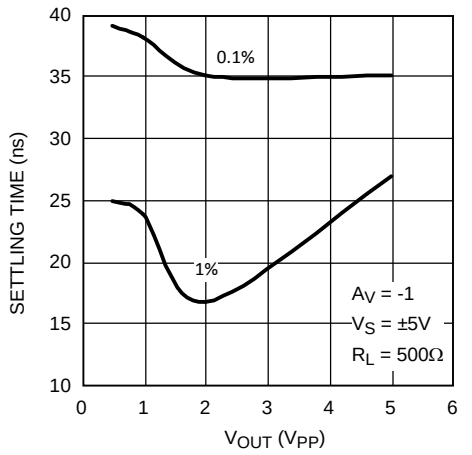


Figure 28. Settling Time vs. Output Step Amplitude

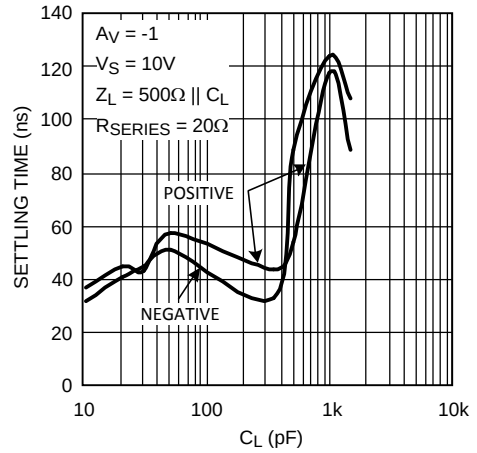


Figure 29. 0.1% Settling Time vs. Cap Load

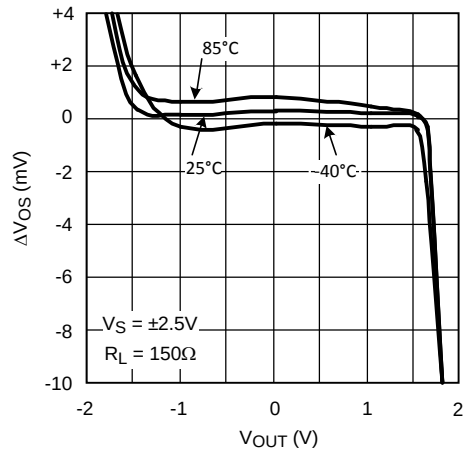


Figure 30. ΔV_{OS} vs. V_{OUT}

Typical Characteristics (continued)

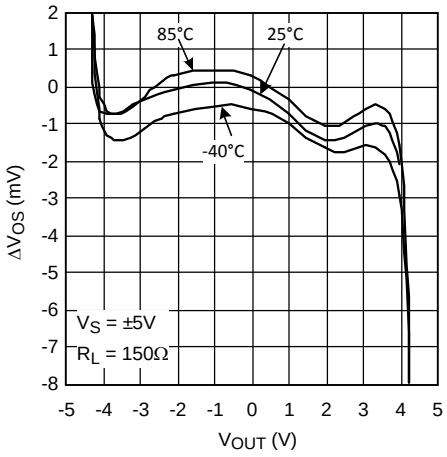


Figure 31. ΔV_{OS} vs. V_{OUT}

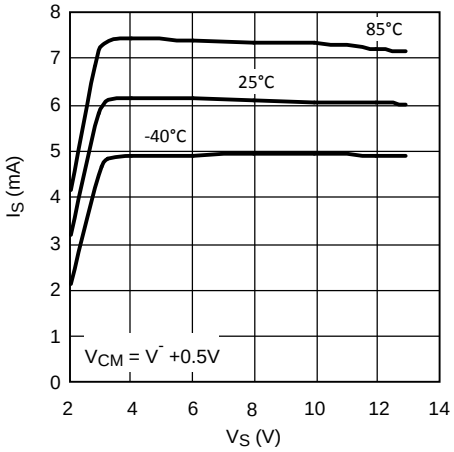


Figure 32. I_S /Amp vs. V_S

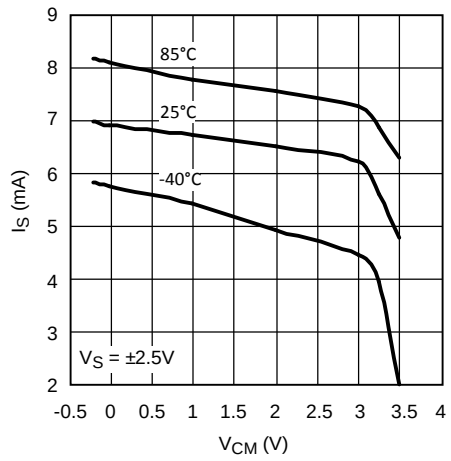


Figure 33. I_S/Amp vs. V_{CM}

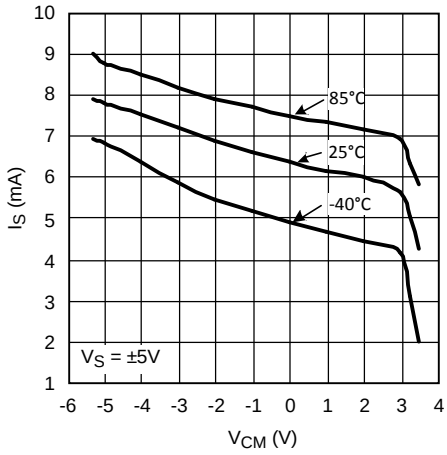


Figure 34. I_S/Amp vs. V_{CM}

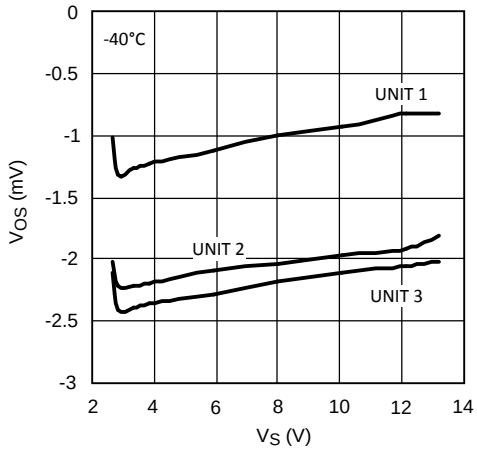


Figure 35. V_{OS} vs. V_S (for 3 Representative Units)

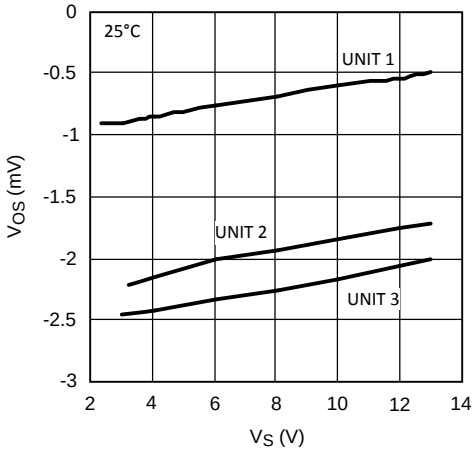


Figure 36. V_{OS} vs. V_S (for 3 Representative Units)

Typical Characteristics (continued)

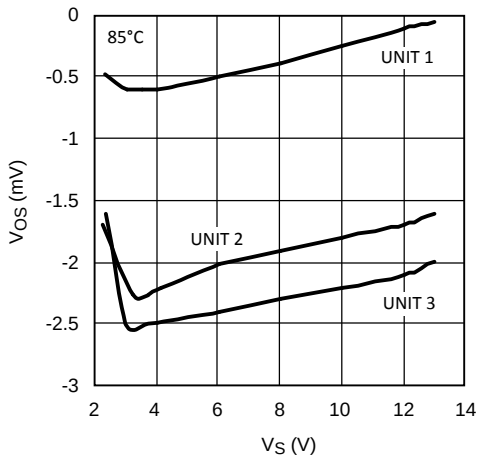


Figure 37. V_{OS} vs. V_S (for 3 Representative Units)

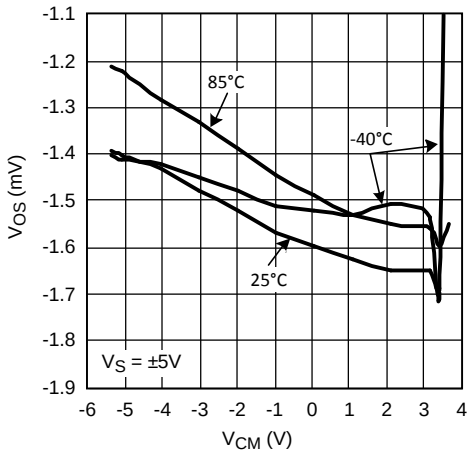


Figure 38. V_{OS} vs. V_{CM} (A Typical Unit)

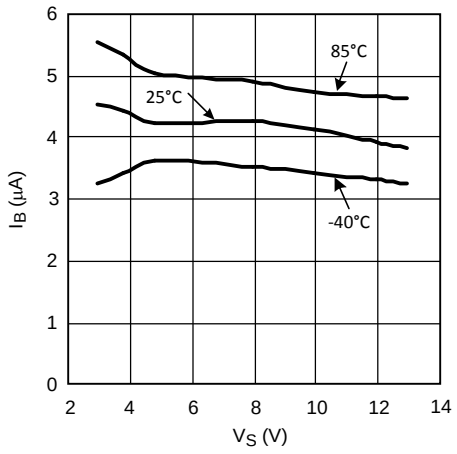


Figure 39. $|I_B|$ vs. V_S

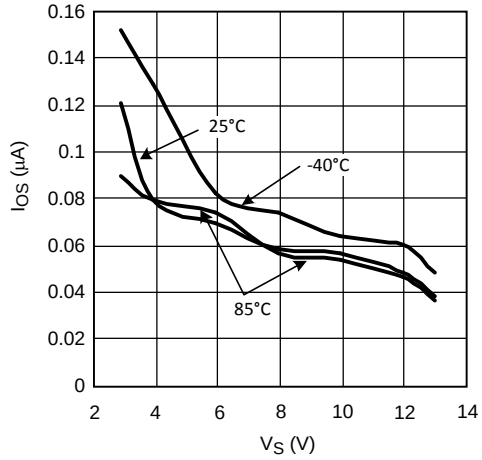


Figure 40. I_{OS} vs. V_S

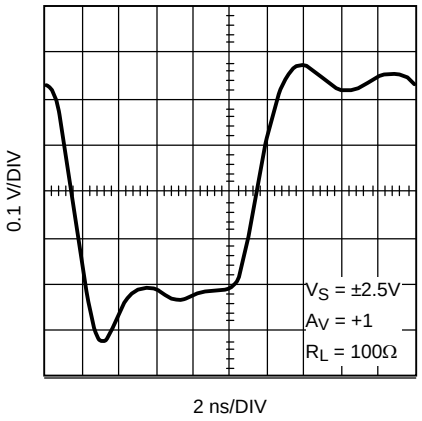


Figure 41. Small Signal Step Response

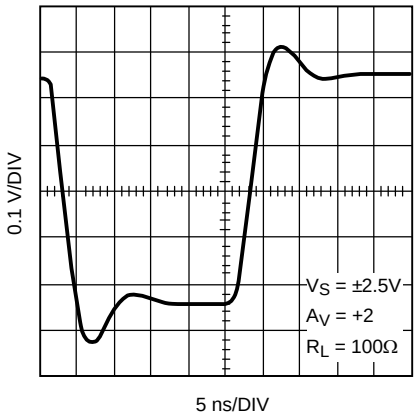


Figure 42. Small Signal Step Response

Typical Characteristics (continued)

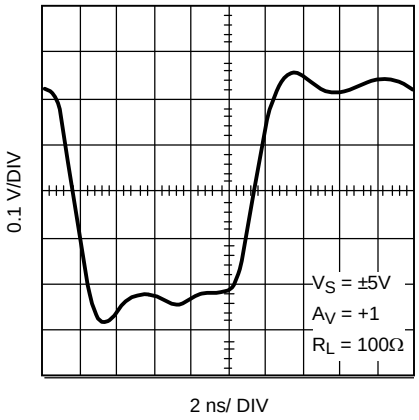


Figure 43. Small Signal Step Response

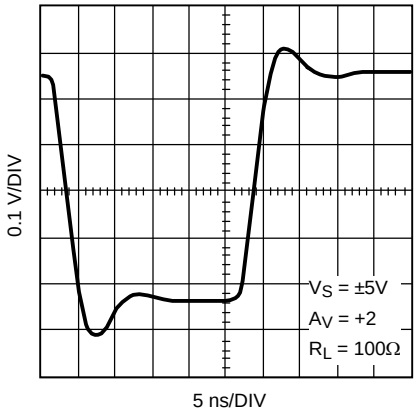


Figure 44. Small Signal Step Response

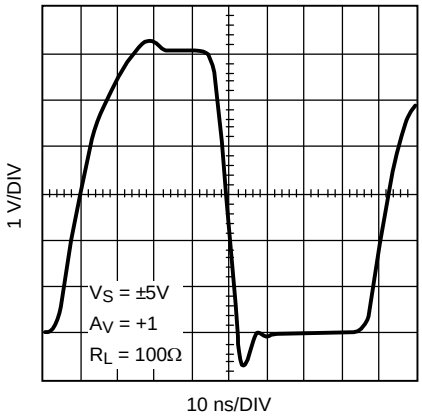


Figure 45. Large Signal Step Response

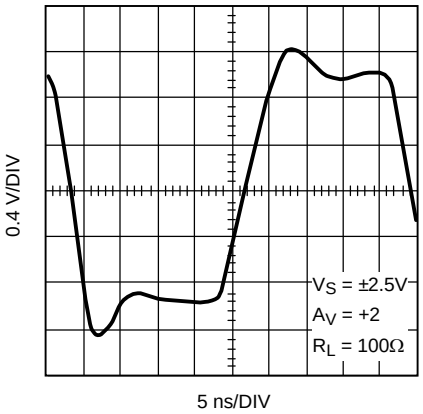


Figure 46. Large Signal Step Response

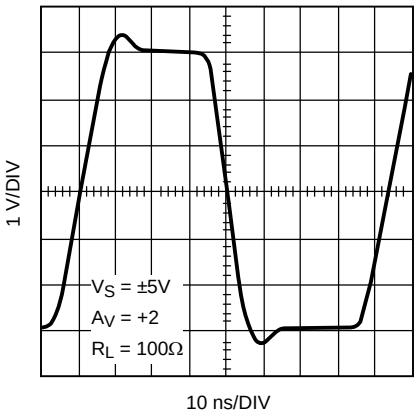


Figure 47. Large Signal Step Response

7 Detailed Description

7.1 Overview

7.1.1 Large Signal Behavior

The LMH6657 and LMH6658 are large-bandwidth, fast slew rate, voltage feedback operational ampplifers ideal for high-speed, large signal applications. The low input referred voltage noise in conjunction with an input voltage range, which extends below V–, eases the adoption of this part in applications having a tiny signal at or near system ground, as well as other high-speed, low-distortion, and low-noise systems. Also, the large Gain Bandwidth Product allows high gain operation that does not compromise speed.

7.2 Feature Description

The LMH6657 and LMH6658 input stage is designed to provide excess overdrive when needed. This occurs when fast input signal excursions cannot be followed by the output stage. In these situations, the device encounters larger input signals than would be encountered under normal closed loop conditions. The LMH6657 and LMH6658 input stage is designed to take advantage of this "input overdrive" condition. The larger the amount of this overdrive, the greater is the speed with which the output voltage can change. Here is a plot of how the output slew rate limitation varies with respect to the amount of overdrive imposed on the input:

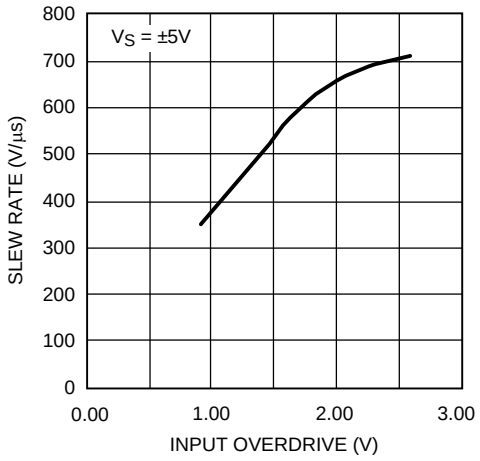


Figure 48. Plot Showing the Relationship Between Slew Rate and Input Overdrive

To relate the explanation above to a practical example, consider the following application example. Consider the case of a closed loop amplifier with a gain of −1 amplifying a sinusoidal waveform. From the plot of Output vs. Input (Figure 8), with a 30-MHz signal and $7V_{PP}$ input signal, it can be seen that the output will be limited to a swing of 6.9 V_{PP}. From the frequency Response plot it can be seen that the inverting gain of −1 has a −32° output phase shift at this frequency.

It can be shown that this setup will result in about 1.9 V_{PP} differential input voltage corresponding to 650 V/µs of slew rate from Figure 48, above ($SR = V_O(pp) \times \pi \times f = 650V/\mu s$)

Note that the amount of overdrive appearing on the input for a given sinusoidal test waveform is affected by the following:

- Output swing
- Gain setting
- Input/output phase relationship for the given test frequency
- Amplifier configuration (inverting or noninverting)

Due to the higher frequency phase shift between input and output, there is no closed form solution to input overdrive for a given input. Therefore, Figure 48 is not very useful by itself in determining the output swing.

The following plots aid in predicting the output transition time based on the amount of swing required for a given gain setting.

Feature Description (continued)

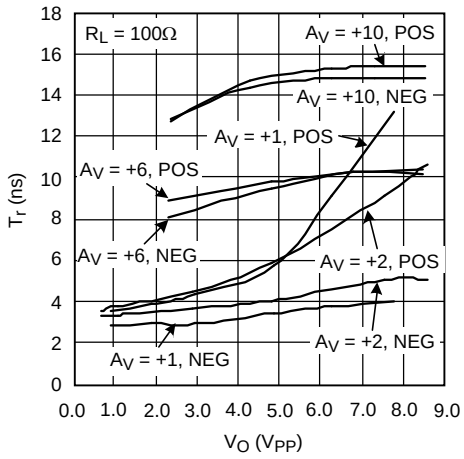


Figure 49. Output 20%-80% Transition vs. Output Voltage Swing (Noninverting Gain)

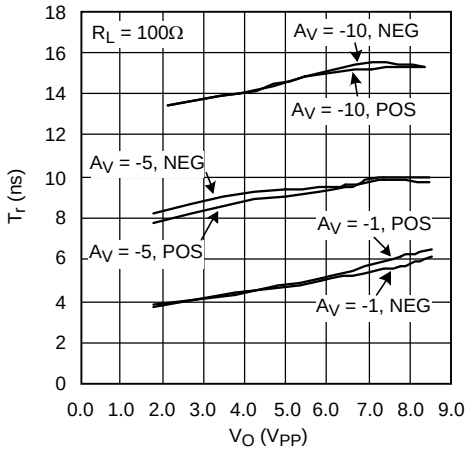


Figure 50. Output 20%-80% Transition vs. Output Voltage Swing (Inverting Gain)

Beyond a gain of 5 or so, the LMH6657/6658 output transition would be limited by bandwidth. For example, with a gain of 5, the −3dB BW would be around 30MHz corresponding to a rise time of about 12ns (10% - 90%). Assuming a near linear transition, the 20%-80% transition time would be around 9ns which matches the measured results as shown in Figure 49.

When the output is heavily loaded, output swing may be limited by current capability of the device. Refer to *Output Current Capability* section for more details.

7.3 Device Functional Modes

7.3.1 Output Phase Reversal

This is a problem with some operational amplifiers. This effect is caused by phase reversal in the input stage due to saturation of one or more of the transistors when the inputs exceed the normal expected range of voltages. Some applications, such as servo control loops among others, are sensitive to this kind of behavior and would need special safeguards to ensure proper functioning. The LMH6657 and LMH6658 is immune to output phase reversal with input overload. With inputs exceeded, the LMH6657 and LMH6658 output will stay at the clamped voltage from the supply rail. Exceeding the input supply voltages beyond the *Absolute Maximum Ratings* of the device could however damage or otherwise adversely effect the reliability or life of the device.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Output Characteristics

8.1.1.1 Output Current Capability

The LMH6657/6658 output swing for a given load can be determined by referring to the Output Voltage vs. Output Current plots in *Typical Characteristics*. Characteristic Tables show the output current when the output is 1V from either rail. The plots and table values can be used to predict closed loop continuous value of current for a given load. If left unchecked, the output current capability of the LMH6657 and LMH6658 could easily result in junction temperature exceeding the maximum allowed value specified under *Absolute Maximum Ratings*. Proper heat sinking or other precautions are required if conditions as such exist.

Under transient conditions, such as when the input voltage makes a large transition and the output has not had time to reach its final value, the device can deliver output currents in excess of the typical plots mentioned above. Plots shown in Figure 51 and Figure 52 depict how the output current capability improves under higher input overdrive voltages:

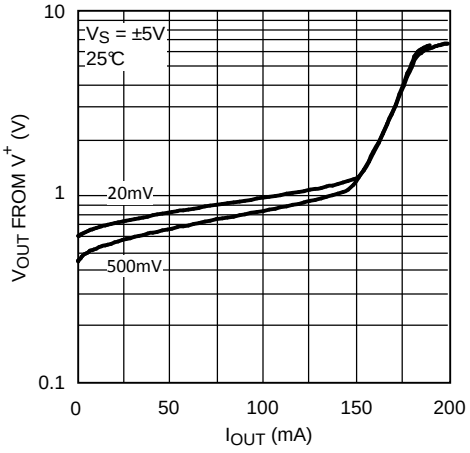


Figure 51. V_{OUT} vs. I_{SOURCE} (for Various Overdrive)

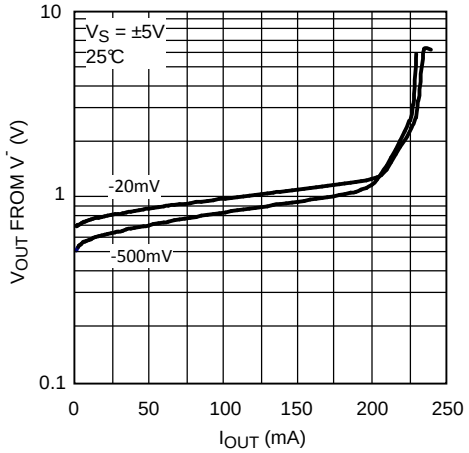


Figure 52. V_{OUT} vs. I_{SINK} (for Various Overdrive)

The LMH6657 and LMH6658 output stage is designed to swing within approximately one diode drop of each supply voltage by utilizing specially designed high speed output clamps. This allows adequate output voltage swing even with 5-V supplies and yet avoids some of the issues associated with rail-to-rail output operational amplifiers. Some of these issues are:

- Supply current increases when output reaches saturation at or near the supply rails
- Prolonged recovery when output approaches the rails

The LMH6657 and LMH6658 output is exceedingly well-behaved when it comes to recovering from an overload condition. As can be seen from Figure 53, the LMH6657 and LMH6658 will typically recover from an output overload condition in about 18 ns, regardless of the duration of the overload.

Application Information (continued)

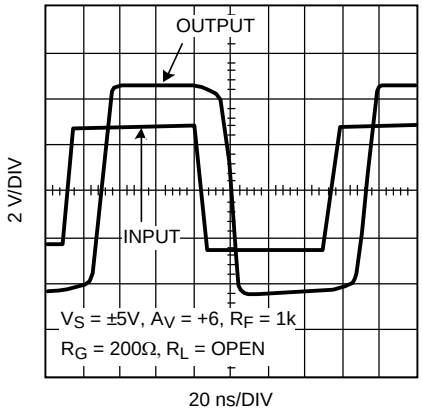


Figure 53. Output Overload Recovery

8.1.1.2 Driving Capacitive Loads

The LMH6657 and LMH6658 can drive moderate values of capacitance by utilizing a series isolation resistor between the output and the capacitive load. *Typical Characteristics* shows the settling time behavior for various capacitive loads and 20 Ω of isolation resistance. Capacitive load tolerance will improve with higher closed loop gain values. Applications such as ADC buffers, among others, present complex and varying capacitive loads to the operational amplifier; best value for this isolation resistance is often found by experimentation and actual trial and error for each application.

8.1.1.3 Distortion

Applications with demanding distortion performance requirements are best served with the device operating in the inverting mode. The reason for this is that in the inverting configuration, the input common-mode voltage does not vary with the signal and there is no subsequent ill effects due to this shift in operating point and the possibility of additional non-linearity. Moreover, under low closed loop gain settings (most suited to low distortion), the noninverting configuration is at a further disadvantage of having to contend with the input common voltage range. There is also a strong relationship between output loading and distortion performance (that is, 1 kΩ vs. 100 Ω distortion improves by about 20 dB at 100 KHz) especially at the lower frequency end where the distortion tends to be lower. At higher frequency, this dependence diminishes greatly such that this difference is only about 4 dB at 10 MHz. But, in general, lighter output load leads to reduced HD3 term and thus improves THD.

9 Power Supply Recommendations

The LMH665x can operate off a single-supply or with dual supplies. The input CM capability of the parts (CMVR) extends all the way down to the V- rail to simplify single-supply applications. Supplies should be decoupled with low-inductance, often ceramic, capacitors to ground less than 0.5 inches from the device pins. TI recommends the use of ground plane, and as in most high-speed devices, it is advisable to remove ground plane close to device sensitive pins such as the inputs.

10 Layout

10.1 Layout Guidelines

Generally, a good high frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillations. See Application Note OA-15, *Frequent Faux Pas in Applying Wideband Current Feedback Amplifiers* (SNOA367) for more information. TI suggests the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization:

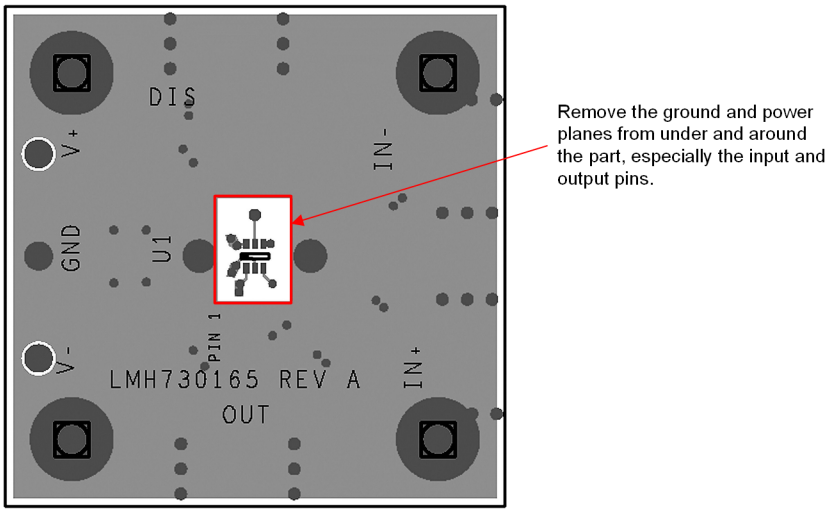
Layout Guidelines (continued)

Table 1. Evaluation Board Guide

DEVICE	PACKAGE	EVALUATION BOARD PIN
LMH6657MF	SOT-23-5	LMH730216
LMH6657MG	SC-70	LMH730165
LMH6658MA	8-Pin SOIC	LMH730036
LMH6658MM	8-Pin VSSOP	LMH730123

Another important parameter in working with high speed/high performance amplifiers, is the component values selection. Choosing external resistors that are large in value will effect the closed loop behavior of the stage because of the interaction of these resistors with parasitic capacitances. These capacitors could be inherent to the device or a by-product of the board layout and component placement. Either way, keeping the resistor values lower, will diminish this interaction to a large extent. On the other hand, choosing very low value resistors will load down nodes and will contribute to higher overall power dissipation.

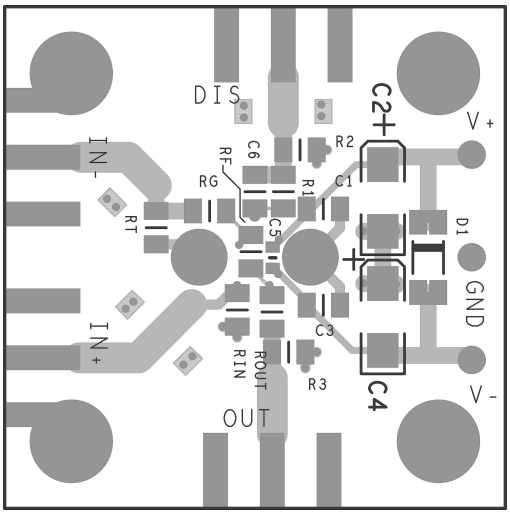
10.2 Layout Example



SC-70 Board Layout (Actual size = 1.5 in × 1.5 in)

Figure 54. Layer 1 Silk

Layout Example (continued)



SC-70 Board Layout (Actual size = 1.5 in × 1.5 in)

Figure 55. Layer 2 Silk

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

See Application Note OA-15, *Frequent Faux Pas in Applying Wideband Current Feedback Amplifiers*, SNOA367

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMH6657	Click here	Click here	Click here	Click here	Click here
LMH6658	Click here	Click here	Click here	Click here	Click here

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6657MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	A85A	Samples
LMH6657MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	A85A	Samples
LMH6657MG	LIFEBUY	SC70	DCK	5	1000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 85	A76	
LMH6657MG/NOPB	ACTIVE	SC70	DCK	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	A76	Samples
LMH6658MA/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMH66 58MA	Samples
LMH6658MAX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMH66 58MA	Samples
LMH6658MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	A88A	Samples
LMH6658MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	A88A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

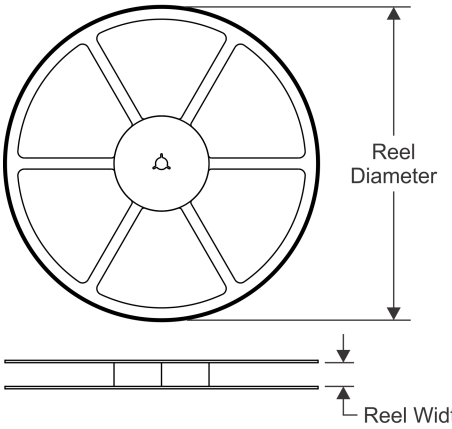
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

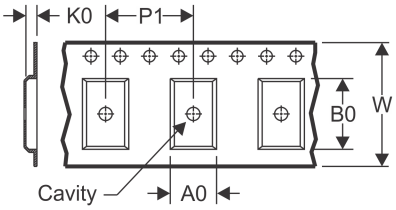
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

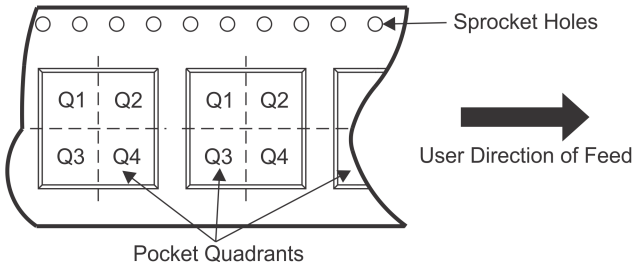


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

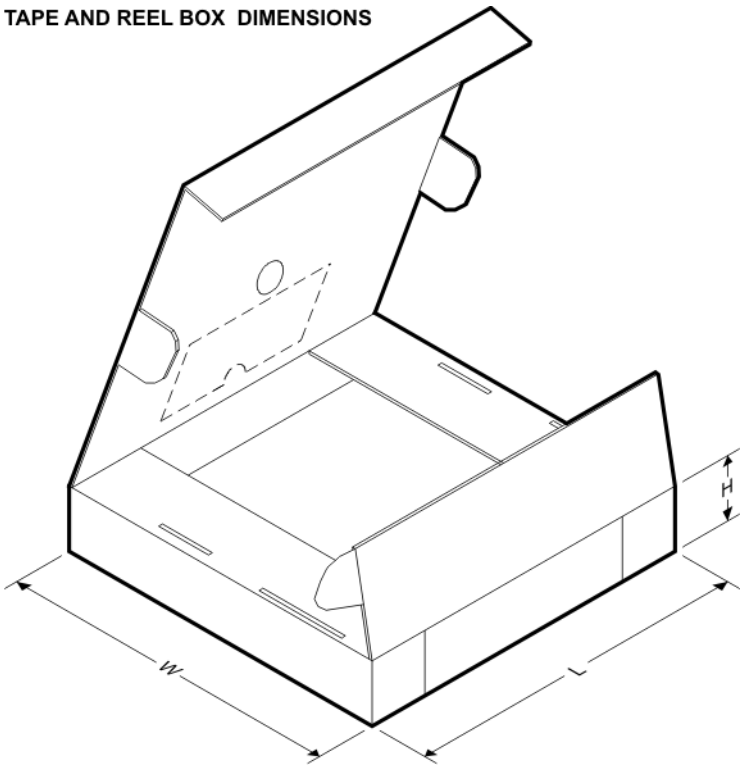
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6657MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6657MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6657MG	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMH6657MG/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMH6658MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6658MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMH6658MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

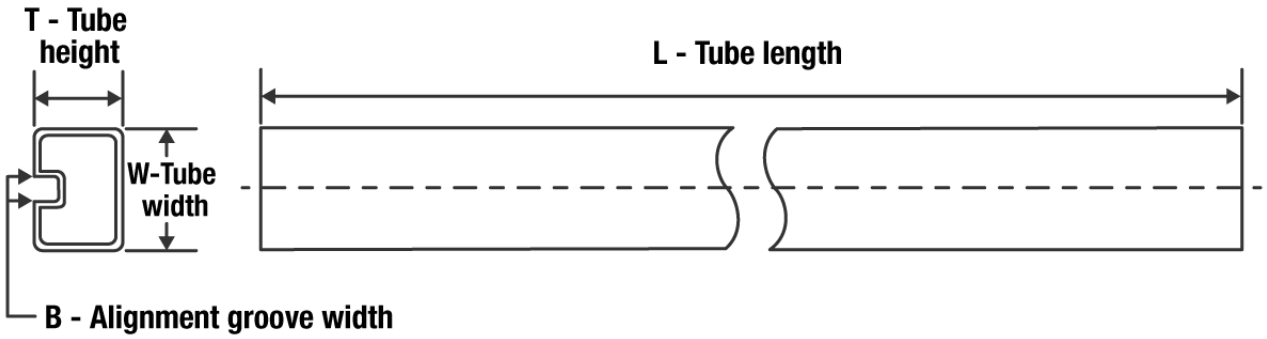
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6657MF/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMH6657MFX/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LMH6657MG	SC70	DCK	5	1000	208.0	191.0	35.0
LMH6657MG/NOPB	SC70	DCK	5	1000	208.0	191.0	35.0
LMH6658MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH6658MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LMH6658MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

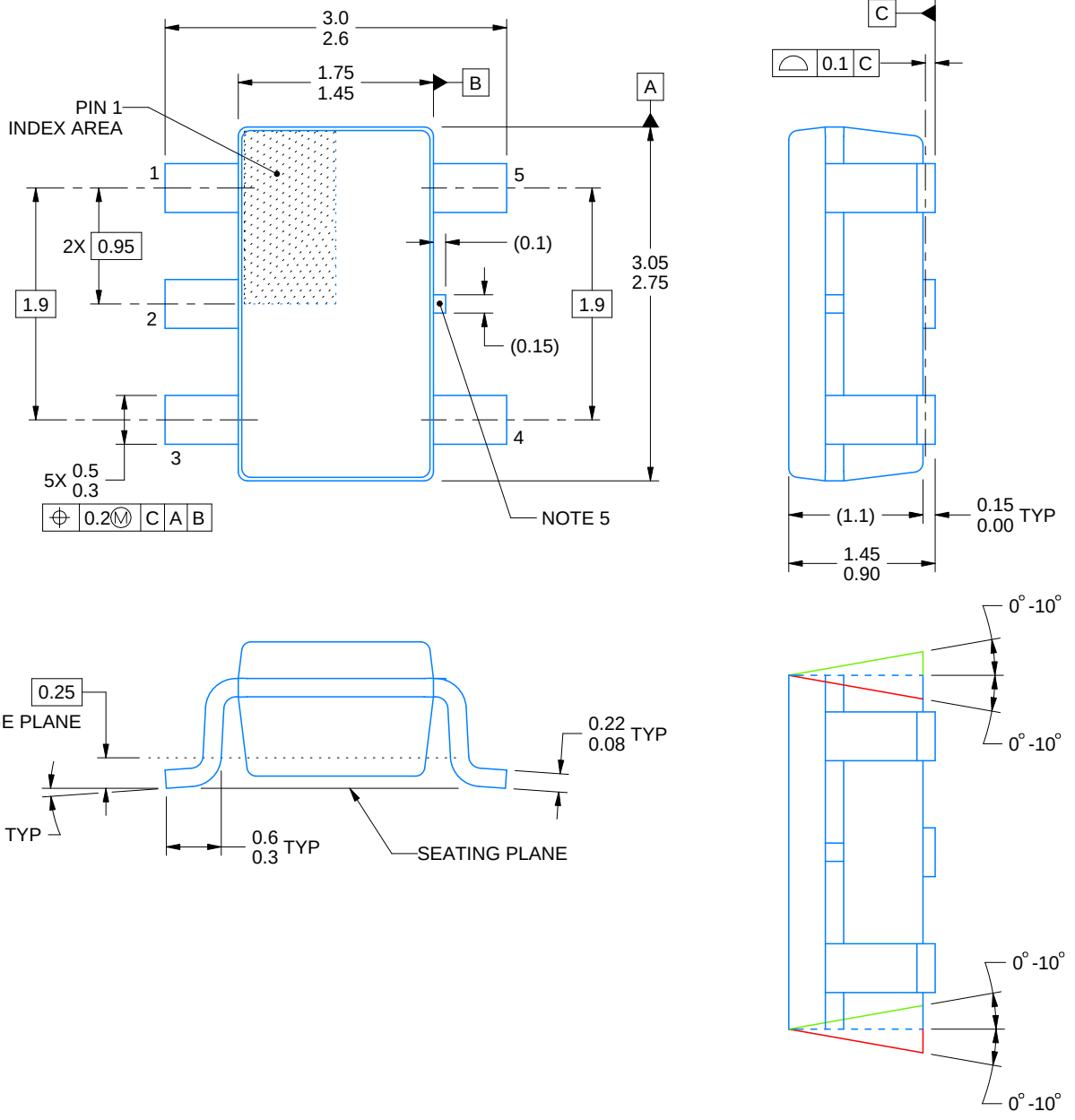
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMH6658MA/NOPB	D	SOIC	8	95	495	8	4064	3.05

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

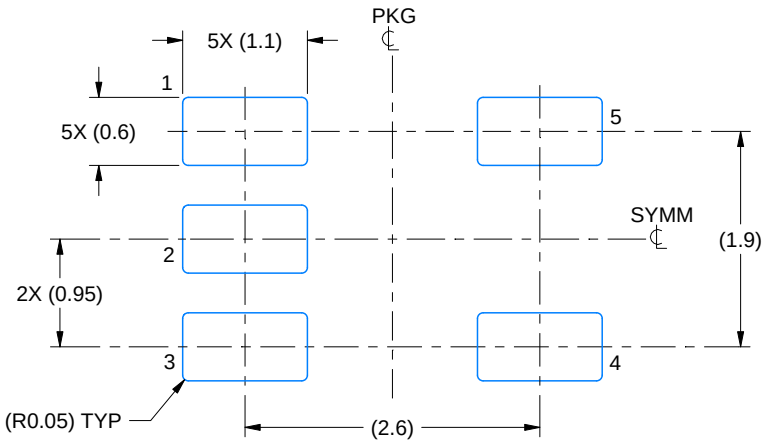


ALTERNATIVE PACKAGE SINGULATION VIEW

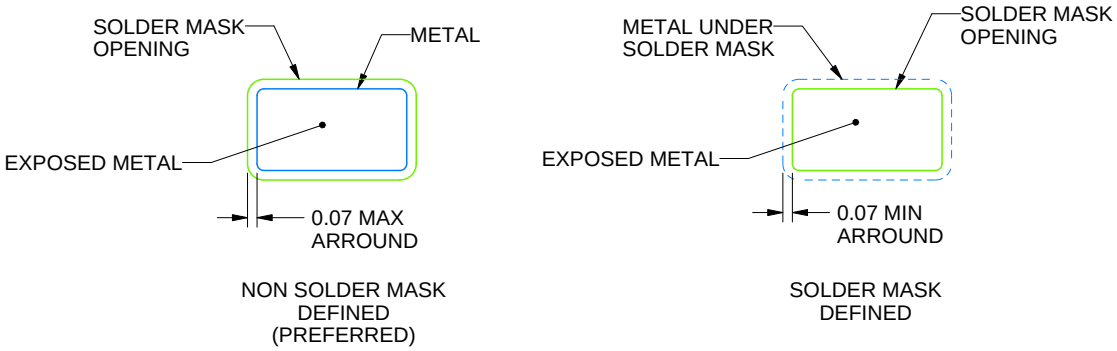
4214839/H 09/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

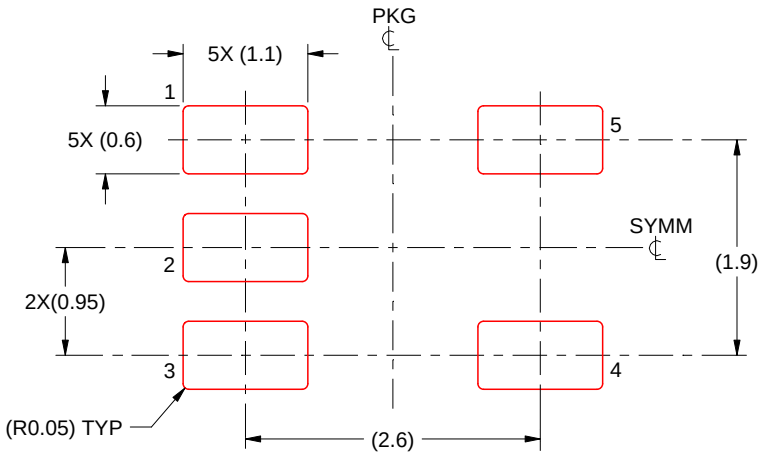


SOLDER MASK DETAILS

4214839/H 09/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

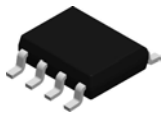


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/H 09/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

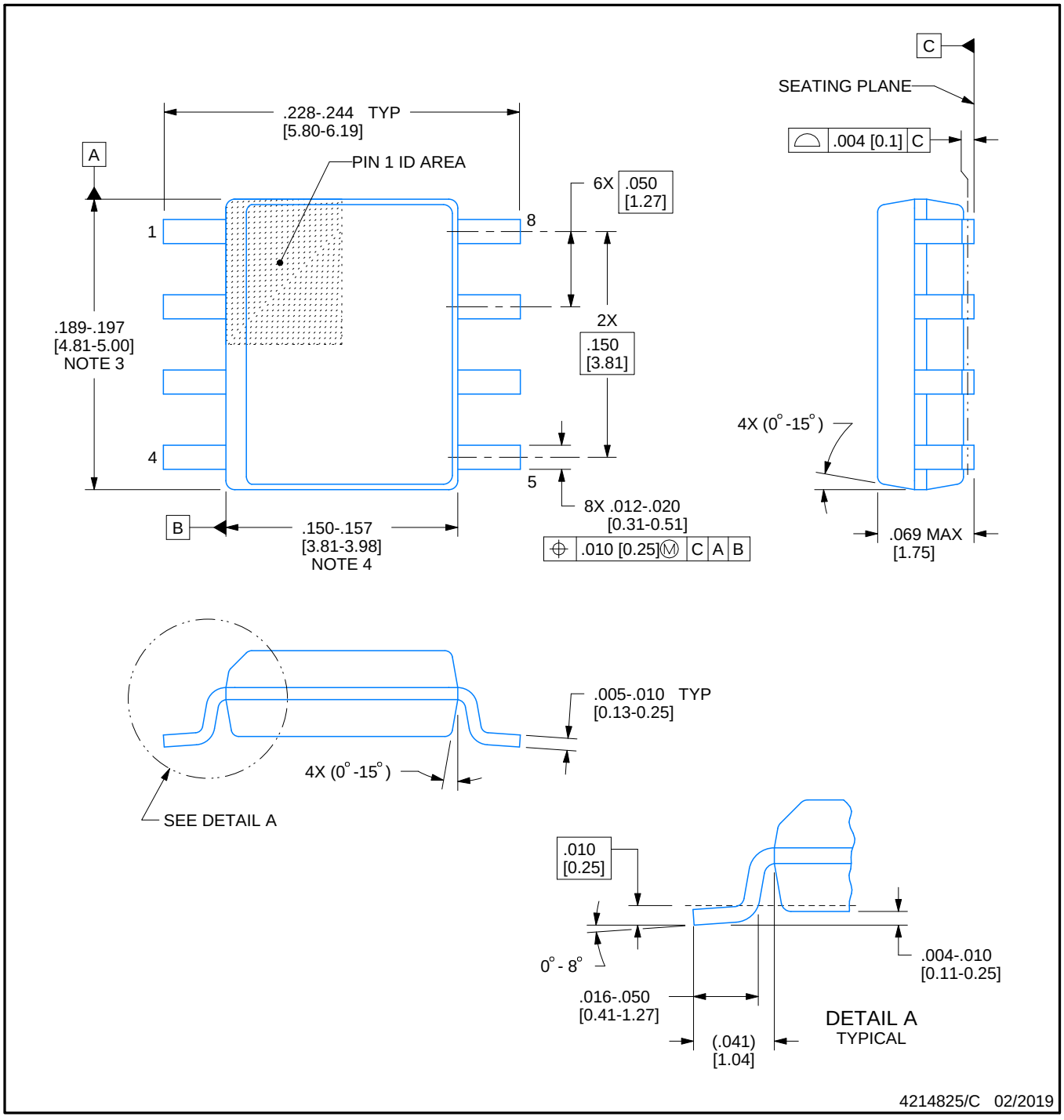


PACKAGE OUTLINE

D0008A

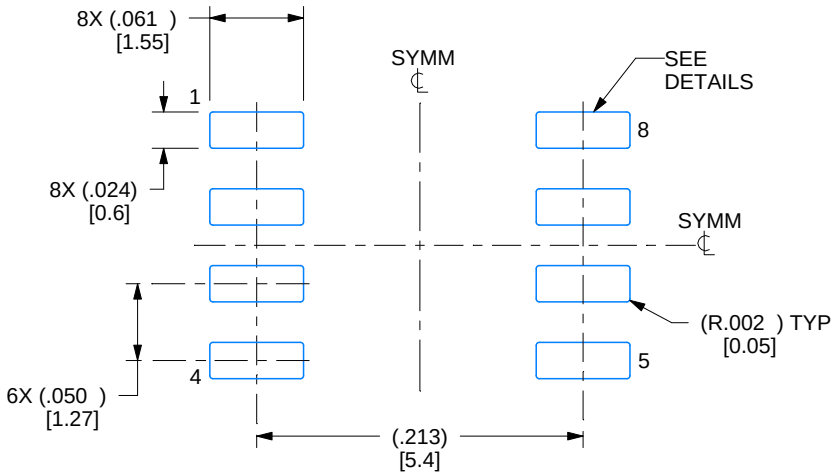
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

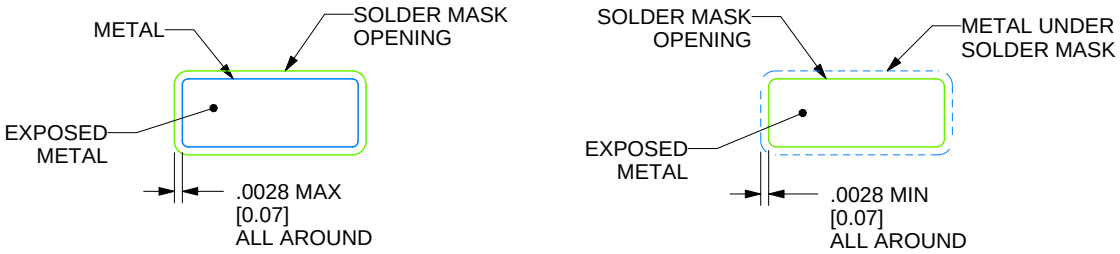


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

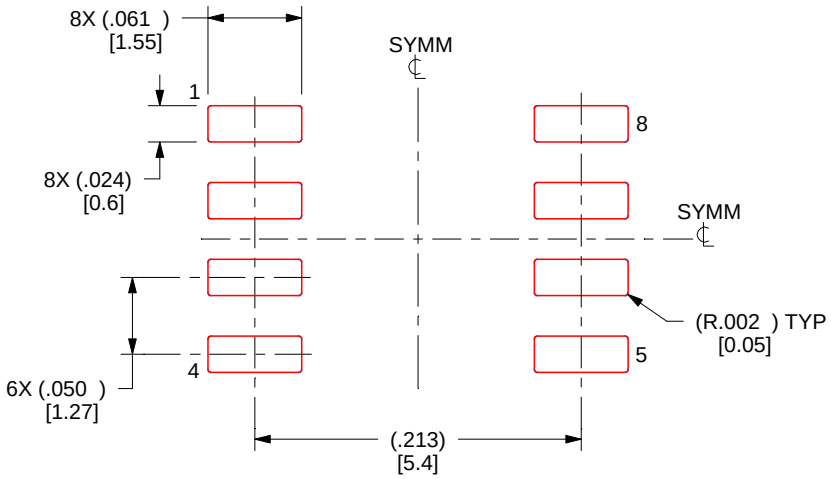
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



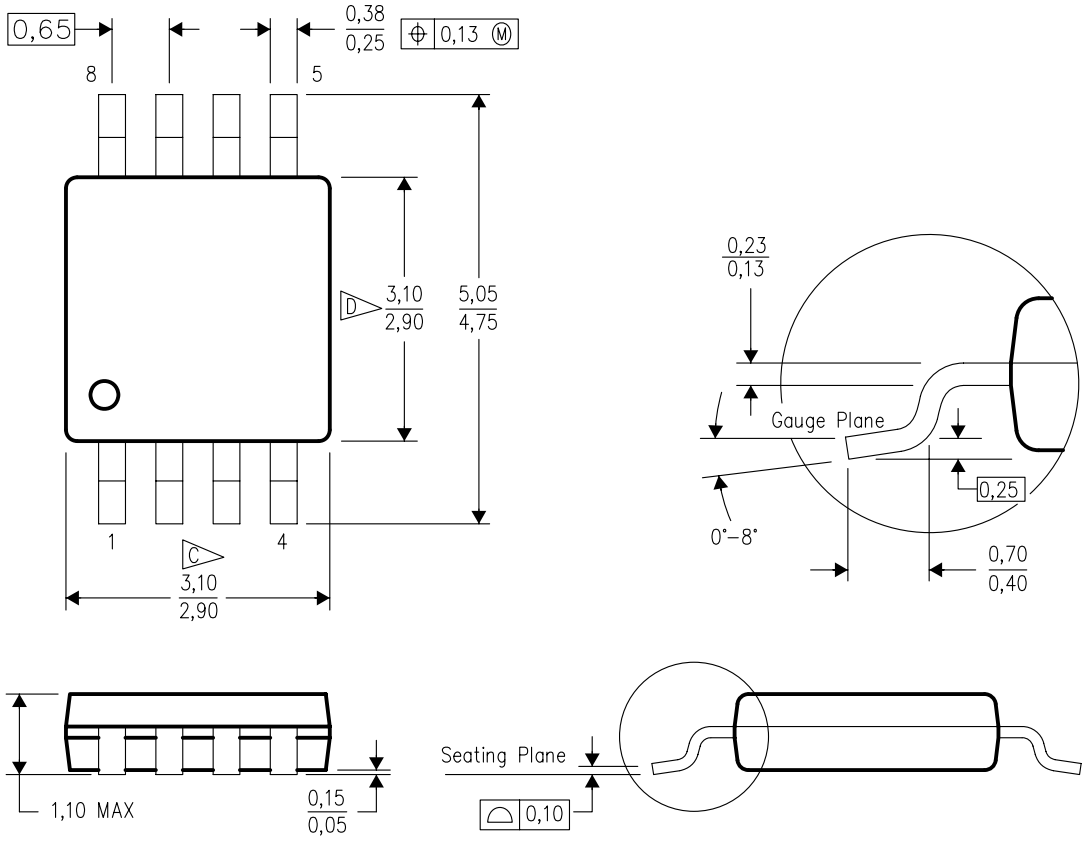
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

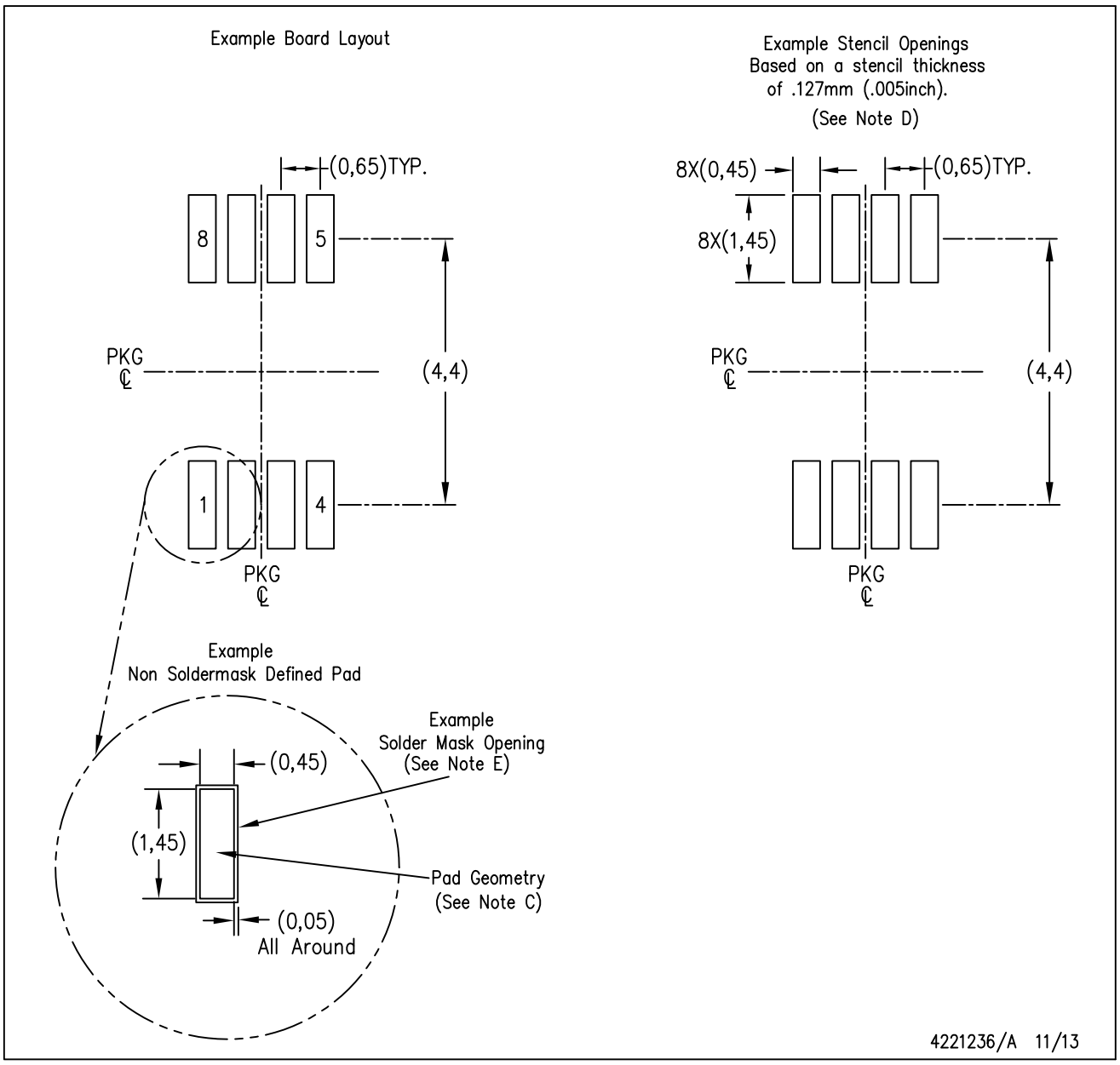
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



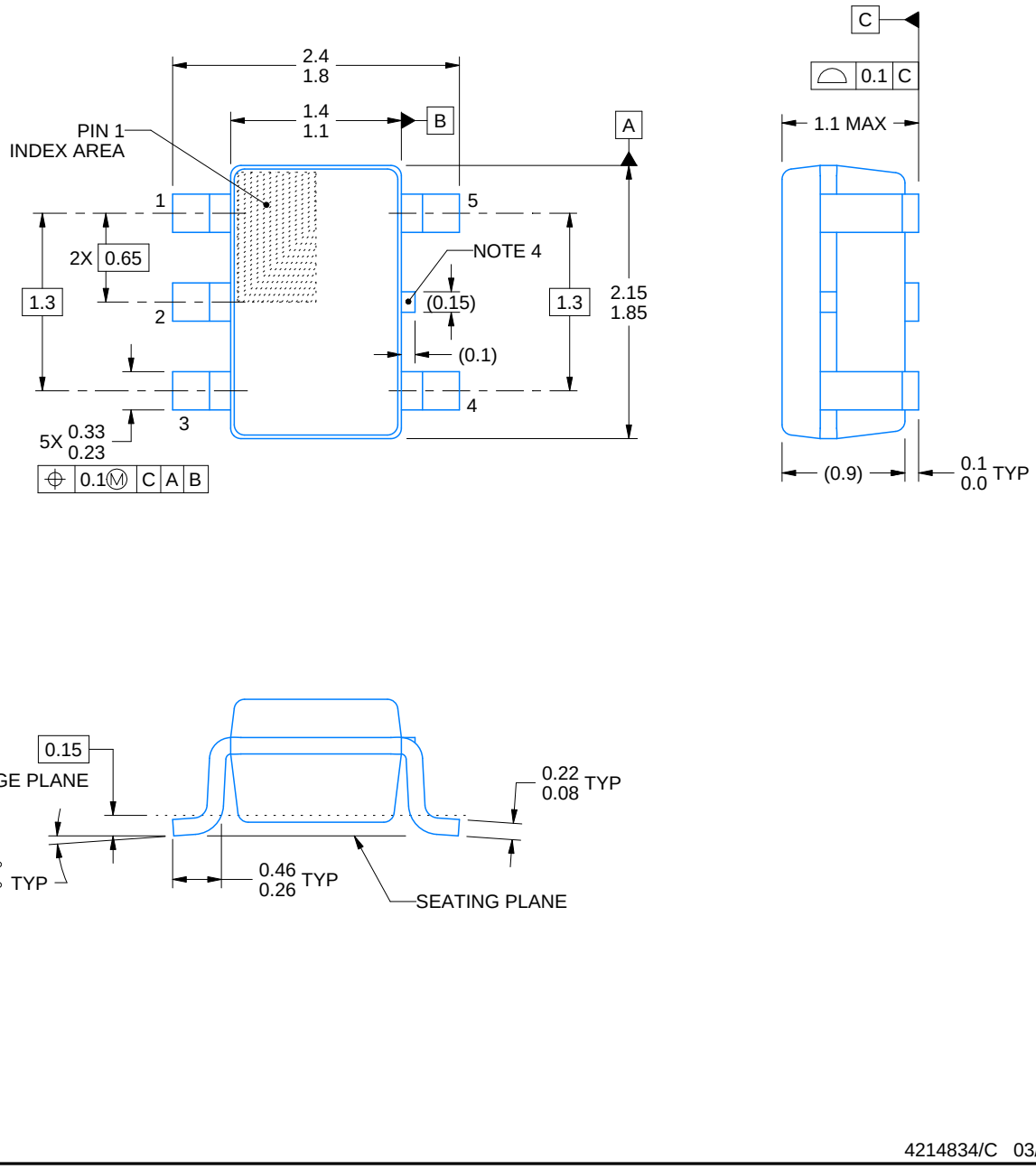
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

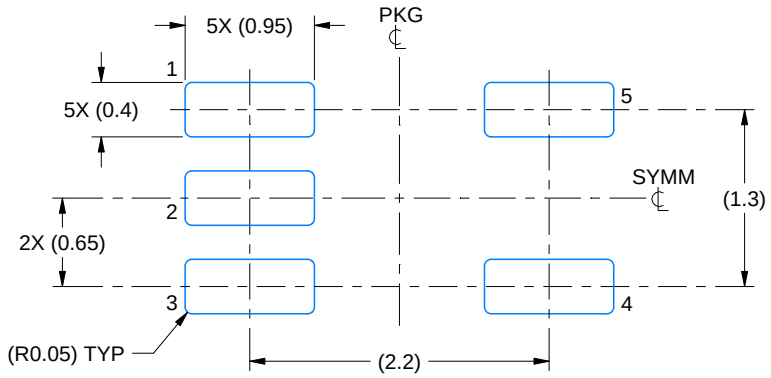
SMALL OUTLINE TRANSISTOR



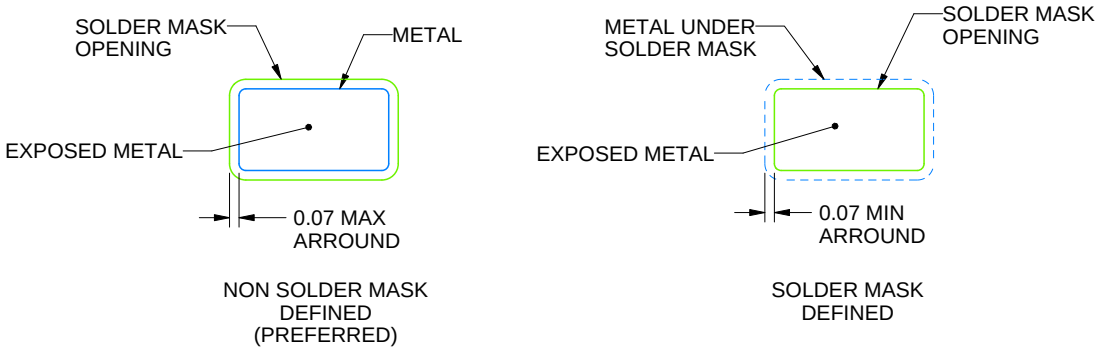
4214834/C 03/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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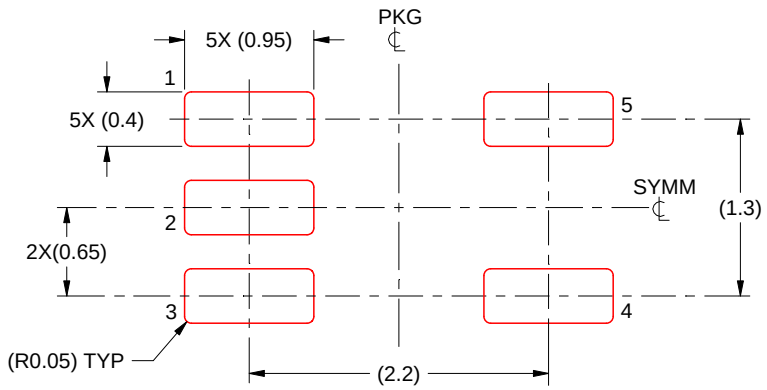
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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