

TPD8S300A USB Type-C™ Port Protector: Short-to- V_{BUS} Overvoltage and IEC ESD Protection

1 Features

- 4-Channels of Short-to- V_{BUS} Overvoltage Protection (CC1, CC2, SBU1, SBU2 or CC1, CC2, DP, DM): 24- V_{DC} Tolerant
- 8-Channels of IEC 61000-4-2 ESD Protection (CC1, CC2, SBU1, SBU2, DP_T, DM_T, DP_B, DM_B)
- CC1 and CC2 Overvoltage Protection FETs 600 mA Capable for Passing V_{CONN} Power
- CC Dead Battery Resistors Integrated for Handling Dead Battery Use Case in Mobile Devices
- Advantages over TPD8S300
 - Improved Dead Battery Performance
 - USB Type-C Port Stays Connected during an IEC 61000-4-2 ESD Strike
- 3-mm x 3-mm WQFN Package

2 Applications

- Laptop PC
- Tablets
- Smartphones
- Monitors and TVs
- Docking Stations

3 Description

The TPD8S300A is a single-chip USB Type-C port protection device that provides 20-V Short-to- V_{BUS} overvoltage and IEC ESD protection.

Since the release of the USB Type-C connector, many products and accessories for USB Type-C have been released that do not meet the USB Type-C specification. One example of this is USB Type-C Power Delivery adaptors that only place 20 V on the V_{BUS} line. Another concern for USB Type-C is that mechanical twisting and sliding of the connector could short pins due to the close proximity they have in this small connector. This can cause 20-V V_{BUS} to be shorted to the CC and SBU pins. Also due to the proximity of the pins in the Type-C connector, there is a heightened concern that debris and moisture will cause the 20-V V_{BUS} pin to be shorted to the CC and SBU pins.

These non-ideal equipments and mechanical events make it necessary for the CC and SBU pins to be 20-V tolerant, even though the pins only operate at 5 V or lower. The TPD8S300A enables the CC and SBU pins to be 20-V tolerant without interfering with normal operation by providing overvoltage protection on the CC and SBU pins. The device places high voltage FETs in series on the SBU and CC lines. When a voltage above the OVP threshold is detected on these lines, the high voltage switches are opened up, isolating the rest of the system from the high voltage condition present on the connector.

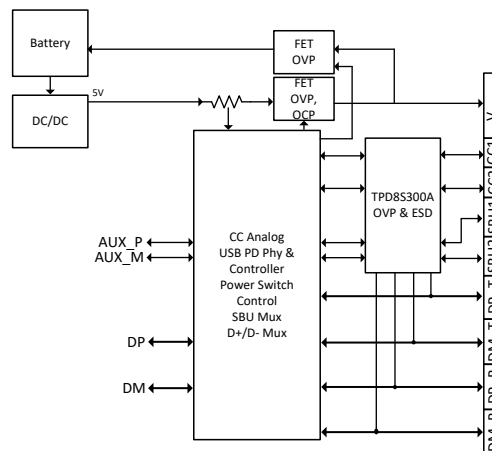
Finally, most systems require IEC 61000-4-2 system level ESD protection for external pins. The TPD8S300A integrates IEC 61000-4-2 ESD protection for the CC1, CC2, SBU1, SBU2, DP, and DM pins, eliminating the need to place high voltage TVS diodes externally on the connector.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD8S300A	WQFN (20)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

CC and SBU Over-Voltage Protection



CC and DP/DM Over-Voltage Protection

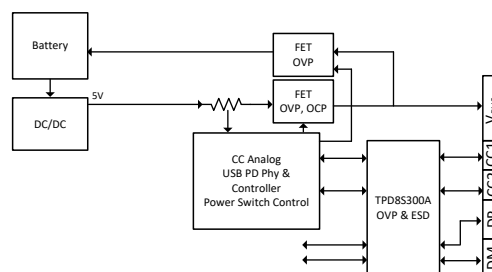


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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

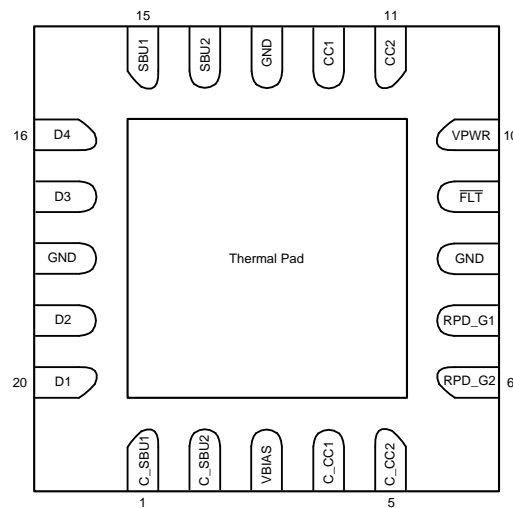
DATE	REVISION	NOTES
June 2018	*	Initial release.

5 Device Comparison Table

Part Number	Over Voltage Protected Channels	IEC 61000-4-2 ESD Protected Channels
TPD6S300A	4-Ch (CC1, CC2, SBU1, SBU2 or CC1, CC2, DP, DM)	6-Ch (CC1, CC2, SBU1, SBU2, DP, DM)
TPD8S300A	4-Ch (CC1, CC2, SBU1, SBU2 or CC1, CC2, DP, DM)	8-Ch (CC1, CC2, SBU1, SBU2, DP_T, DM_T, DP_B, DM_B)

6 Pin Configuration and Functions

**RUK Package
20-Pin WQFN
Top View**



Pin Functions

NO.	PIN		DESCRIPTION
	NAME	TYPE ⁽¹⁾	
1	C_SBU1	I/O	Connector side of the SBU1 OVP FET. Connect to either SBU pin of the USB Type-C connector. Alternatively, connect to either USB2.0 pin of the USB Type-C connector to protect the USB2.0 pins instead of the SBU pins
2	C_SBU2	I/O	Connector side of the SBU2 OVP FET. Connect to either SBU pin of the USB Type-C connector. Alternatively, connect to either USB2.0 pin of the USB Type-C connector to protect the USB2.0 pins instead of the SBU pins
3	VBIAS	Power	Pin for ESD support capacitor. Place a 0.1- μ F capacitor on this pin to ground
4	C_CC1	I/O	Connector side of the CC1 OVP FET. Connect to either CC pin of the USB Type-C connector
5	C_CC2	I/O	Connector side of the CC2 OVP FET. Connect to either CC pin of the USB Type-C connector
6	RPD_G2	I/O	Short to C_CC2 if dead battery resistors are needed. If dead battery resistors are not needed, short pin to GND
7	RPD_G1	I/O	Short to C_CC1 if dead battery resistors are needed. If dead battery resistors are not needed, short pin to GND
8	GND	GND	Ground
9	FLT	O	Open drain for fault reporting
10	VPWR	Power	2.7-V to 3.6-V power supply
11	CC2	I/O	System side of the CC2 OVP FET. Connect to either CC pin of the CC/PD controller

(1) I = input, O = output, I/O = input and output, GND = ground, P = power

Pin Functions (continued)

PIN		TYPE ⁽¹⁾	DESCRIPTION
NO.	NAME		
12	CC1	I/O	System side of the CC1 OVP FET. Connect to either CC pin of the CC/PD controller
13	GND	GND	Ground
14	SBU2	I/O	System side of the SBU2 OVP FET. Connect to either SBU pin of the SBU MUX. Alternatively, connect to either USB2.0 pin of the USB2.0 Phy when protecting the USB2.0 pins instead of protecting the SBU pins
15	SBU1	I/O	System side of the SBU1 OVP FET. Connect to either SBU pin of the SBU MUX. Alternatively, connect to either USB2.0 pin of the USB2.0 Phy when protecting the USB2.0 pins instead of protecting the SBU pins
16	D4	I/O	USB2.0 IEC ESD protection. Connect to any of the USB2.0 pins of the USB Type-C connector
17	D3	I/O	USB2.0 IEC ESD protection. Connect to any of the USB2.0 pins of the USB Type-C connector
18	GND	GND	Ground
19	D2	I/O	USB2.0 IEC ESD protection. Connect to any of the USB2.0 pins of the USB Type-C connector
20	D1	I/O	USB2.0 IEC ESD protection. Connect to any of the USB2.0 pins of the USB Type-C connector
—	Thermal Pad	GND	Internally connected to GND. Used as a heatsink. Connect to the PCB GND plane

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT	
V _I	Input voltage	V _{PWR}	-0.3	4	V
		RPD_G1, RPD_G2	-0.3	24	V
V _O	Output voltage	$\overline{\text{FLT}}$	-0.3	6	V
		VBIAS	-0.3	24	V
V _{IO}	I/O voltage	D1, D2	-0.3	6	V
		CC1, CC2, SBU1, SBU2	-0.3	6	V
		C_CC1, C_CC2, C_SBU1, C_SBU2	-0.3	24	V
T _A	Operating free air temperature	-40	85	°C	
T _{stg}	Storage temperature	-65	150	°C	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings—JEDEC Specification

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±500 V may actually have higher performance.

7.3 ESD Ratings—IEC Specification

		VALUE	UNIT	
V _(ESD)	Electrostatic discharge ⁽¹⁾	IEC 61000-4-2, C_CC1, C_CC2, D1, D2	Contact discharge	±8000
			Air-gap discharge	±15000
		IEC 61000-4-2, C_SBU1, C_SBU2	Contact discharge	±6000
			Air-gap discharge	±15000

- (1) Tested on the [TPD6S300 EVM](#) connected to the [TPS65982 EVM](#).

7.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT	
V _I	Input voltage	V _{PWR}	2.7	3.3	3.6	V
		RPD_G1, RPD_G2	0		5.5	V
V _O	Output voltage	$\overline{\text{FLT}}$ pull-up resistor power rail			5.5	V
V _{IO}	I/O voltage	D1, D2	-0.3		5.5	V
		CC1, CC2, C_CC1, C_CC2	0		5.5	V
		SBU1, SBU2, C_SBU1, C_SBU2	0		4.3	V
I _{VCONN}	V _{CONN} current	Current flowing into CC1/2 and flowing out of C_CC1/2, V _{CCx} – V _{C_CCx} ≤ 250 mV			600	mA
I _{VCONN}	V _{CONN} current	Current flowing into CC1/2 and flowing out of C_CC1/2, T _J ≤ 105°C			600	mA
I _{VCONN}	V _{CONN} current	Current flowing into CC1/2 and flowing out of C_CC1/2, T _J ≤ 85°C			1.25	A

Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
External components ⁽¹⁾	FLT pullup resistance	1.7		300	kΩ
	VBIAS capacitance ⁽²⁾		0.1		μF
	V _{PWR} capacitance	0.3	1		μF

- (1) For recommended values for capacitors and resistors, the typical values assume a component placed on the board near the pin. Minimum and maximum values listed are inclusive of manufacturing tolerances, voltage derating, board capacitance, and temperature variation. The effective value presented must be within the minimum and maximums listed in the table.
- (2) The VBIAS pin requires a minimum 35-V_{DC} rated capacitor. A 50-V_{DC} rated capacitor is recommended to reduce capacitance derating. See the [VBIAS Capacitor Selection](#) section for more information on selecting the VBIAS capacitor.

7.5 Thermal Information

THERMAL METRIC ⁽¹⁾		TPD8S300A	UNIT
		RUK (WQFN)	
		20 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	45.2	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	48.8	°C/W
R _{θJB}	Junction-to-board thermal resistance	17.1	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	0.6	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	17.1	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	3.7	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CC OVP SWITCHES						
R _{ON}	On resistance of CC OVP FETs, T _J ≤ 85°C	CCx = 5.5 V		278	392	mΩ
	On resistance of CC OVP FETs, T _J ≤ 105°C	CCx = 5.5 V		278	415	mΩ
R _{ON(FLAT)}	On resistance flatness	Sweep CCx voltage between 0 V and 1.2 V			5	mΩ
C _{ON_CC}	Equivalent on capacitance	Capacitance from C _{CCx} or CCx to GND when device is powered. VC _{CCx} /VCCx = 0 V to 1.2 V, f = 400 kHz	60	74	120	pF
R _D	Dead battery pull-down resistance (only present when device is unpowered). Effective resistance of R _D and FET in series	V _{C_{CCx}} = 2.6 V	4.1	5.1	6.1	kΩ
V _{TH_DB}	Threshold voltage of the pulldown FET in series with RD during dead battery	I _{CC} = 80 μA	0.5	0.9	1.2	V
V _{OVPCC}	OVP threshold on CC pins	Place 5.5 V on C _{CCx} . Step up C _{CCx} until the FLT pin is asserted	5.75	6	6.2	V
V _{OVPCC_HYS}	Hysteresis on CC OVP	Place 6.5 V on C _{CCx} . Step down the voltage on C _{CCx} until the FLT pin is deasserted. Measure difference between rising and falling OVP threshold for C _{CCx}		50		mV
BW _{ON}	On bandwidth single ended (–3 dB)	Measure the –3-dB bandwidth from C _{CCx} to CCx. Single ended measurement, 50-Ω system. V _{cm} = 0.1 V to 1.2 V		100		MHz

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{STBUS_CC}	Short-to-VBUS tolerance on the CC pins	Hot-Plug C_CCx with a 1 meter USB Type C Cable, place a 30- Ω load on CCx			24	V
$V_{STBUS_CC_CLAMP}$	Short-to-VBUS system-side clamping voltage on the CC pins (CCx)	Hot-Plug C_CCx with a 1 meter USB Type C Cable. Hot-Plug voltage C_CCx = 24 V. VPWR = 3.3 V. Place a 30- Ω load on CCx		8		V
SBU OVP SWITCHES						
R_{ON}	On resistance of SBU OVP FETs	$SBUx = 3.6\text{ V}$. $-40^{\circ}\text{C} \leq T_J \leq +85^{\circ}\text{C}$		4	6.5	Ω
$R_{ON(FLAT)}$	On resistance flatness	Sweep SBUx voltage between 0 V and 3.6 V. $-40^{\circ}\text{C} \leq T_J \leq +85^{\circ}\text{C}$		0.7	1.5	Ω
C_{ON_SBU}	Equivalent on capacitance	Capacitance from SBUx or C_SBUx to GND when device is powered. Measure at VC_SBUx/VSBUX = 0.3 V to 3.6 V		6		pF
V_{OVPSBU}	OVP threshold on SBU pins	Place 3.6 V on C_SBUx. Step up C_SBUx until the FLT pin is asserted	4.35	4.5	4.7	V
V_{OVPSBU_HYS}	Hysteresis on SBU OVP	Place 5 V on C_CCx. Step down the voltage on C_CCx until the FLT pin is deasserted. Measure difference between rising and falling OVP threshold for C_SBUx		50		mV
BW_{ON}	On bandwidth single ended (–3 dB)	Measure the –3-dB bandwidth from C_SBUx to SBUx. Single ended measurement, 50- Ω system. $V_{cm} = 0.1\text{ V}$ to 3.6 V		1000		MHz
X_{TALK}	Crosstalk	Measure crosstalk at $f = 1\text{ MHz}$ from SBU1 to C_SBU2 or SBU2 to C_SBU1. $V_{cm1} = 3.6\text{ V}$, $V_{cm2} = 0.3\text{ V}$. Be sure to terminate open sides to 50 Ω		–80		dB
V_{STBUS_SBU}	Short-to-VBUS tolerance on the SBU pins	Hot-Plug C_SBUx with a 1 meter USB Type C Cable. Put a 100-nF capacitor in series with a 40- Ω resistor to GND on SBUx			24	V
$V_{STBUS_SBU_CLAMP}$	Short-to-VBUS system-side clamping voltage on the SBU pins (SBUx)	Hot-Plug C_SBUx with a 1 meter USB Type C Cable. Hot-Plug voltage C_SBUx = 24 V. VPWR = 3.3 V. Put a 150-nF capacitor in series with a 40- Ω resistor to GND on SBUx		8		V
POWER SUPPLY and LEAKAGE CURRENTS						
V_{PWR_UVLO}	V_{PWR} under voltage lockout	Place 1 V on VPWR and raise voltage until SBU or CC FETs turnon	2.1	2.3	2.5	V
$V_{PWR_UVLO_HYS}$	V_{PWR} UVLO hysteresis	Place 3 V on VPWR and lower voltage until SBU or CC FETs turnoff; measure difference between rising and falling UVLO to calculate hysteresis	100	150	200	mV
I_{PWR}	V_{PWR} supply current	VPWR = 3.3 V (typical), VPWR = 3.6 V (maximum). $-40^{\circ}\text{C} \leq T_J \leq +85^{\circ}\text{C}$.		90	120	μA
I_{CC_LEAK}	Leakage current for CC pins when device is powered	VPWR = 3.3 V, VC_CCx = 3.6 V, CCx pins are floating, measure leakage into C_CCx pins. Result must be same if CCx side is biased and C_CCx is left floating			5	μA

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SBU_LEAK}	Leakage current for SBU pins when device is powered	VPWR = 3.3 V, VC_SBUx = 3.6 V, SBUx pins are floating, measure leakage into C_SBUx pins. Result must be same if SBUx side is biased and C_SBUx is left floating. $-40^{\circ}\text{C} \leq T_J \leq +85^{\circ}\text{C}$			3	μA
$I_{C_CC_LEAK_OVP}$	Leakage current for CC pins when device is in OVP	VPWR = 0 V or 3.3 V, VC_CCx = 24 V, CCx pins are set to 0 V, measure leakage into C_CCx pins			1200	μA
$I_{C_SBU_LEAK_OVP}$	Leakage current for SBU pins when device is in OVP	VPWR = 0 V or 3.3 V, VC_SBUx = 24 V, SBUx pins are set to 0 V, measure leakage into C_SBUx pins			400	μA
$I_{CC_LEAK_OVP}$	Leakage current for CC pins when device is in OVP	VPWR = 0 V or 3.3 V, VC_CCx = 24 V, CCx pins are set to 0 V, measure leakage out of CCx pins			30	μA
$I_{SBU_LEAK_OVP}$	Leakage current for SBU pins when device is in OVP	VPWR = 0 V or 3.3 V, VC_SBUx = 24 V, SBUx pins are set to 0 V, measure leakage out of SBUx pins	-1		1	μA
I_{Dx_LEAK}	Leakage current for Dx pins	V_Dx = 3.6 V, measure leakage into Dx pins			1	μA
FLT PIN						
V_{OL}	Low-level output voltage	IOL = 3 mA. Measure the voltage at the FLT pin			0.4	V
OVER TEMPERATURE PROTECTION						
T_{SD_RISING}	The rising over-temperature protection shutdown threshold		150	175		$^{\circ}\text{C}$
$T_{SD_FALLING}$	The falling over-temperature protection shutdown threshold		130	140		$^{\circ}\text{C}$
T_{SD_HYST}	The over-temperature protection shutdown threshold hysteresis			35		$^{\circ}\text{C}$
Dx ESD PROTECTION						
V_{RWM_POS}	Reverse stand-off voltage from Dx to GND	Dx to GND. $I_{Dx} \leq 1 \mu\text{A}$			5.5	V
V_{RWM_NEG}	Reverse stand-off voltage from GND to Dx	GND to Dx			0	V
V_{BR_POS}	Break-down voltage from Dx to GND	Dx to GND. $I_{BR} = 1 \text{ mA}$	7			V
V_{BR_NEG}	Break-down voltage from GND to Dx	GND to Dx. $I_{BR} = 8 \text{ mA}$	0.6			V
C_{IO}	Dx to GND or GND to Dx	f = 1 MHz, VIO = 2.5 V		1.7		pF
ΔC_{IO}	Differential capacitance between two Dx pins	f = 1 MHz, VIO = 2.5 V		0.02		pF
R_{DYN}	Dynamic on-resistance Dx IEC clamps	Dx to GND or GND to Dx		0.4		Ω

7.7 Timing Requirements

over operating free-air temperature range (unless otherwise noted)

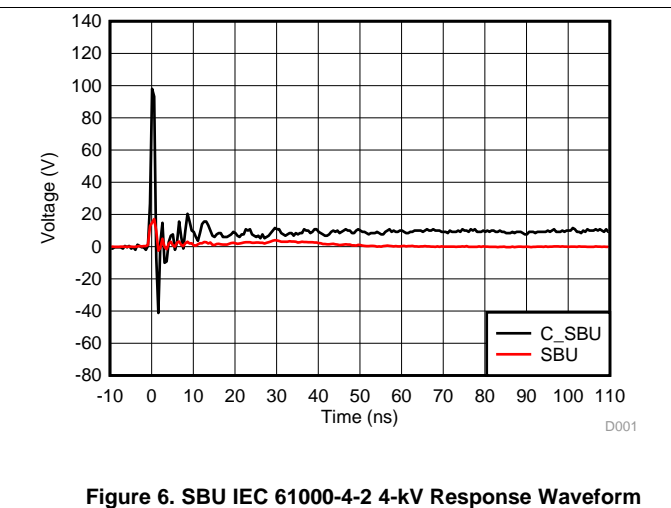
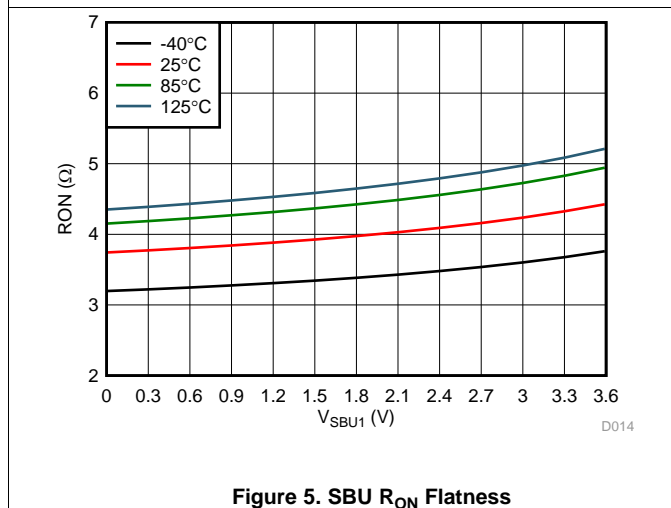
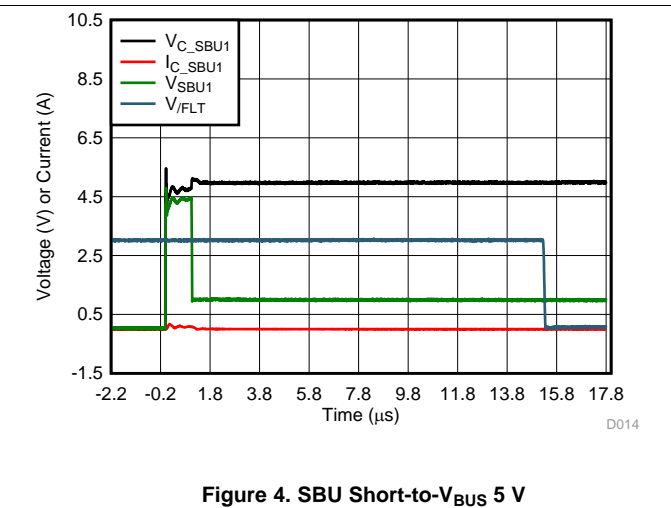
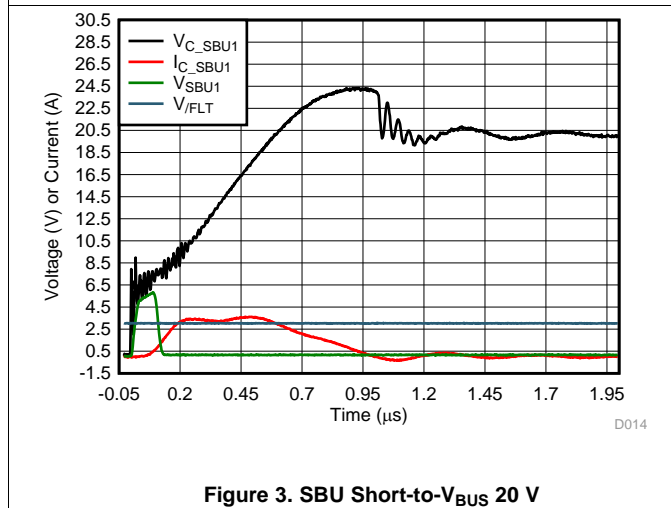
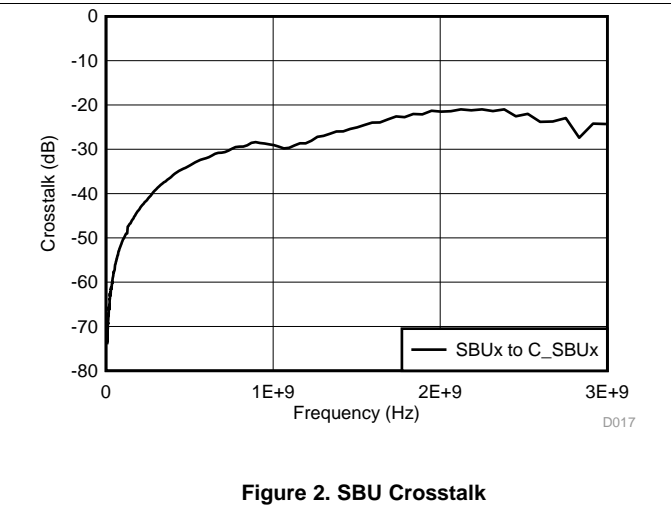
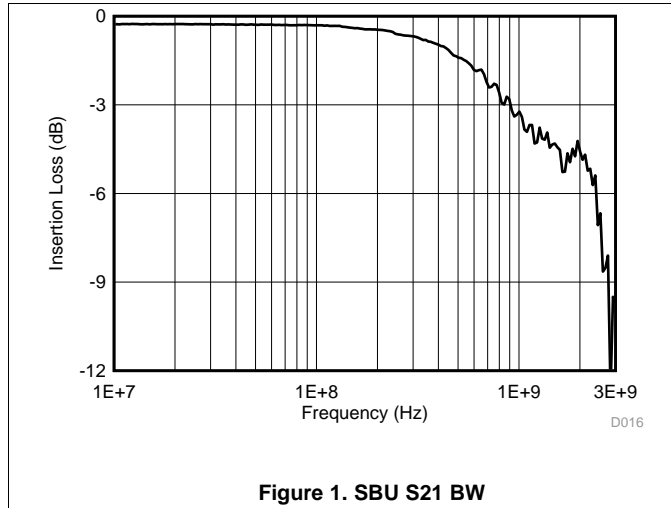
		MIN	NOM	MAX	UNIT
POWER-ON and Off TIMINGS					
t_{ON_FET}	Time from crossing rising VPWR UVLO until CC and SBU OVP FETs are on		1.3	3.5	ms
$t_{ON_FET_DB}$	Time from crossing rising VPWR UVLO until CC and SBU OVP FETs are on and the dead battery resistors are turned off		5.7	9.5	ms
dV_{PWR_OFF}/dt	Minimum Slew rate allowed to guarantee CC and SBU FETs turnoff during a power off	-0.5			V/ μs

Timing Requirements (continued)

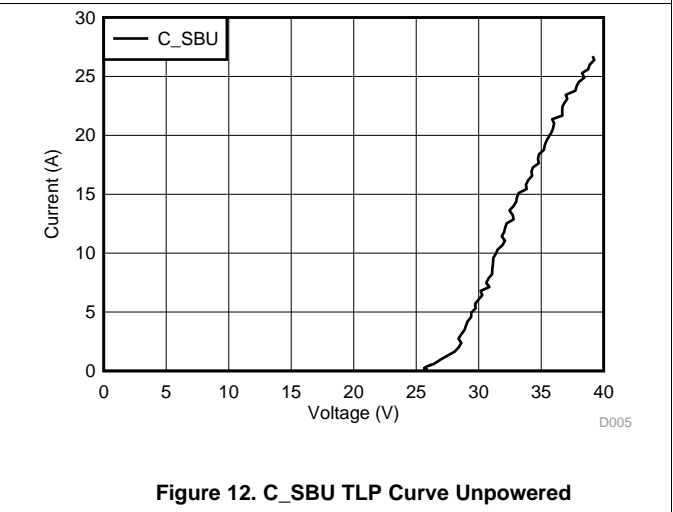
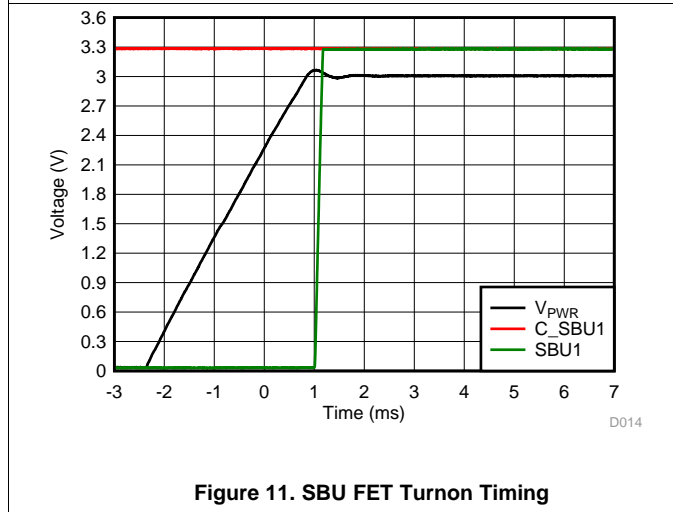
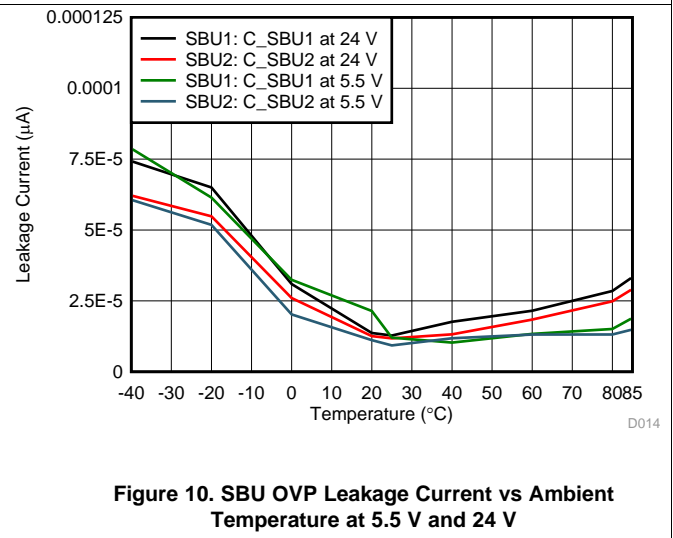
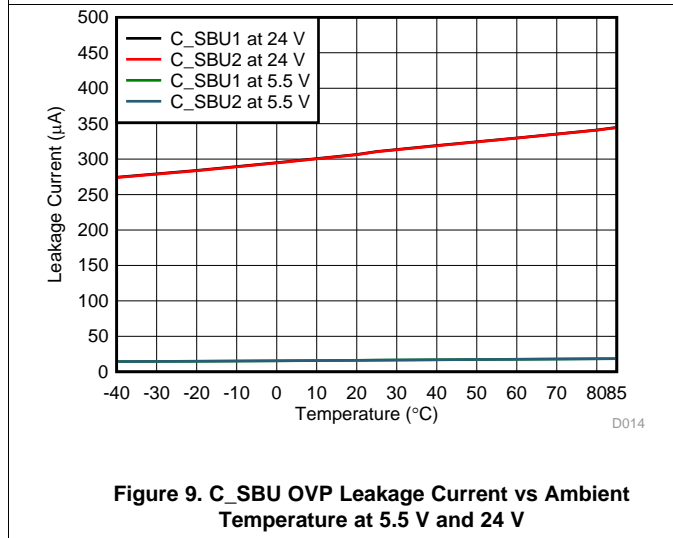
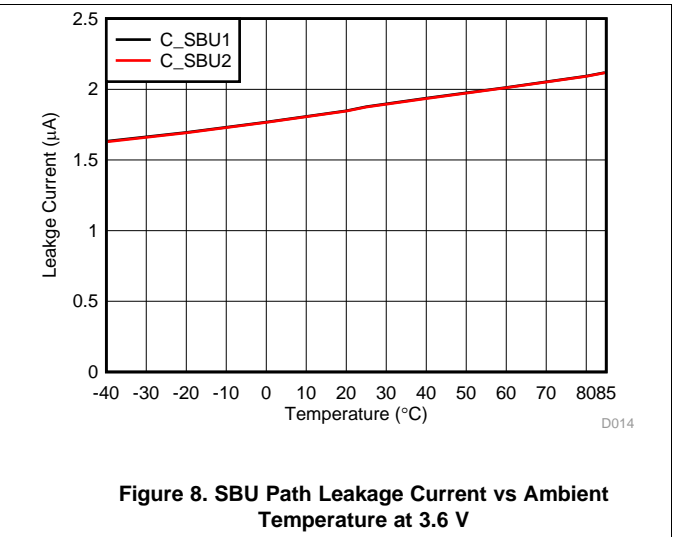
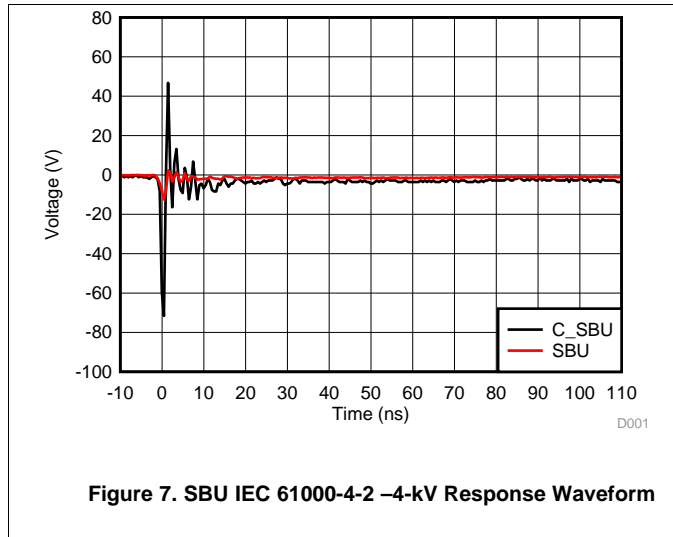
over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
OVER VOLTAGE PROTECTION					
$t_{OVP_RESPONSE_CC}$	OVP response time on the CC pins. Time from OVP asserted until OVP FETs turnoff		70		ns
$t_{OVP_RESPONSE_SBU}$	OVP response time on the SBU pins. Time from OVP asserted until OVP FETs turnoff		80		ns
$t_{OVP_RECOVERY_CC_1_FET}$	OVP recovery time on the CC pins. Once an OVP has occurred, the minimum time duration until the CC FETs turn back on. OVP must be removed for CC FETs to turn back on		0.93		ms
$t_{OVP_RECOVERY_CC_1_DB}$	OVP recovery time on the CC pins. Once an OVP has occurred, the minimum time duration until the CC FETs turn back on and the dead battery resistors turn off. OVP must be removed for CC FETs to turn back on		5		ms
$t_{OVP_RECOVERY_SBU_1}$	OVP recovery time on the SBU pins. Once an OVP has occurred, the minimum time duration until the SBU FETs turn back on. OVP must be removed for SBU FETs to turn back on		0.62		ms
$t_{OVP_RECOVERY_CC_2_FET}$	OVP recovery time on the CC pins. Time from OVP Removal until CC FETs turn back on, if device has been in OVP > 0.6 ms		0.61		ms
$t_{OVP_RECOVERY_CC_2_DB}$	OVP recovery time on the CC pins. Time from OVP Removal until CC FETs turn back on and dead battery resistors turn off, if device has been in OVP > 0.6 ms		4.75		ms
$t_{OVP_RECOVERY_SBU_2}$	OVP recovery time on the SBU pins. Time from OVP Removal until SBU FETs turn back on, if device has been in OVP > 0.6 ms		0.3		ms
$t_{OVP_FLT_ASSERTION}$	Time from OVP asserted to \overline{FLT} assertion		20		μ s
$t_{OVP_FLT_DEASSERTION}$	Time from CC FET turnon after an OVP to \overline{FLT} deassertion		4.1		ms

7.8 Typical Characteristics



Typical Characteristics (continued)



Typical Characteristics (continued)

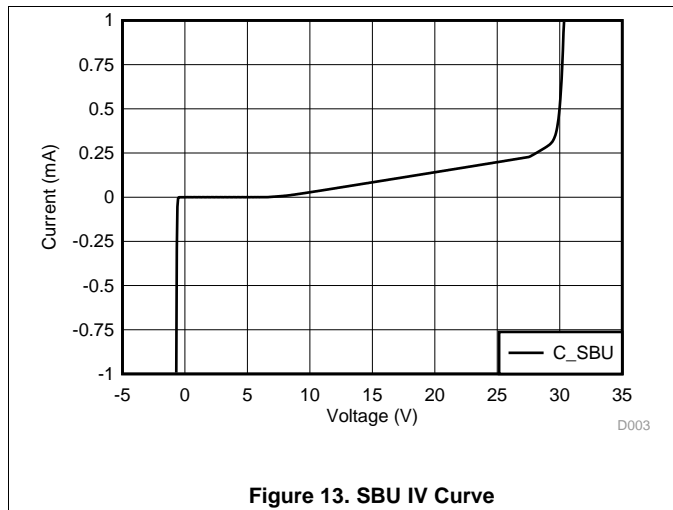


Figure 13. SBU IV Curve

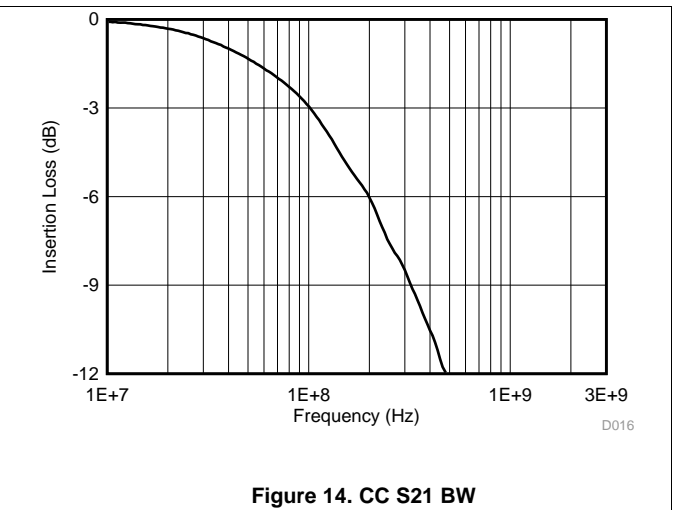


Figure 14. CC S21 BW

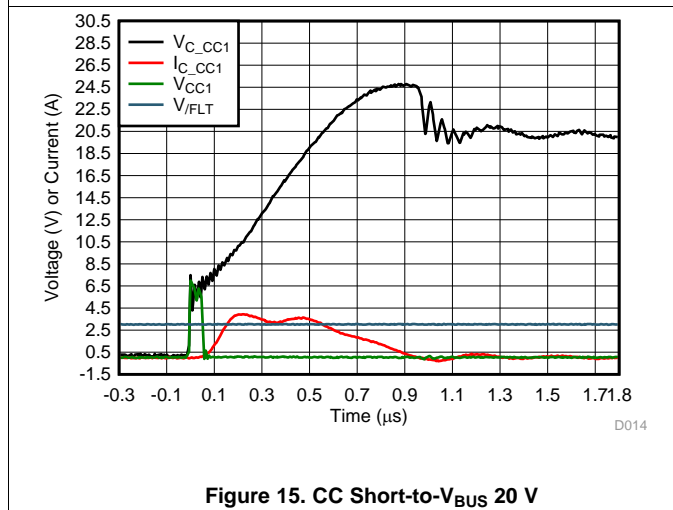


Figure 15. CC Short-to-V_{BUS} 20 V

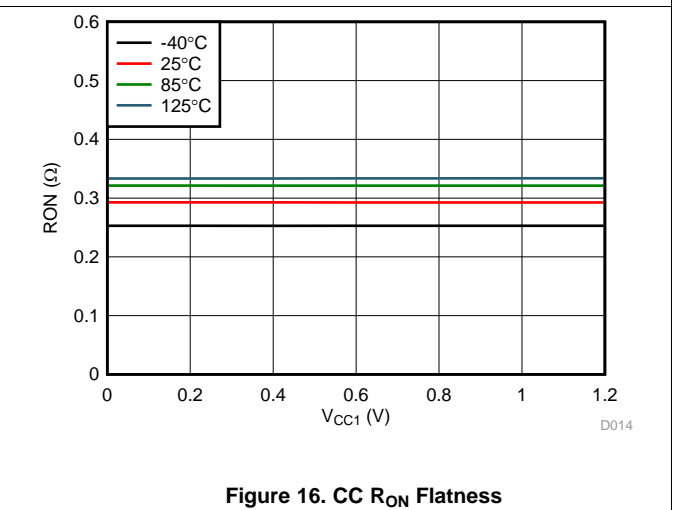


Figure 16. CC R_{ON} Flatness

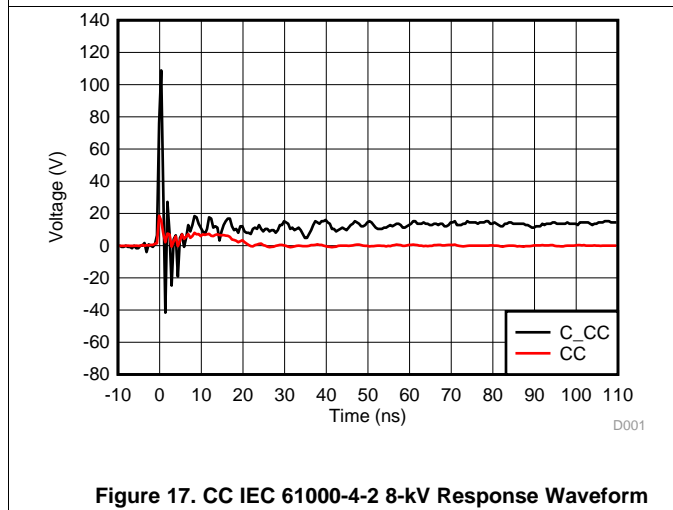


Figure 17. CC IEC 61000-4-2 8-kV Response Waveform

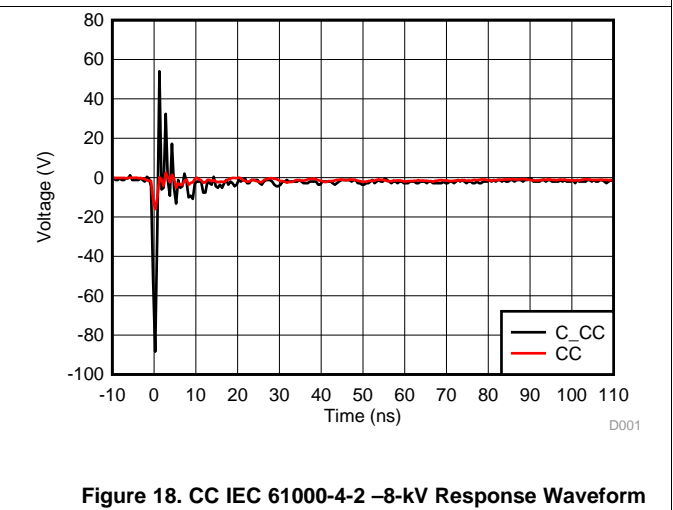


Figure 18. CC IEC 61000-4-2 -8-kV Response Waveform

Typical Characteristics (continued)

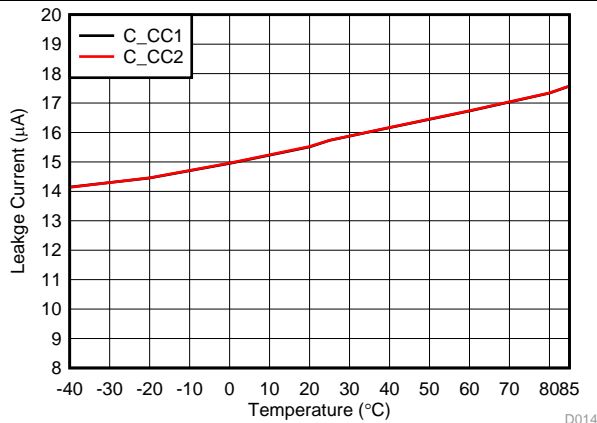


Figure 19. C_CC Path Leakage Current vs Ambient Temperature at C_CC = 5.5 V

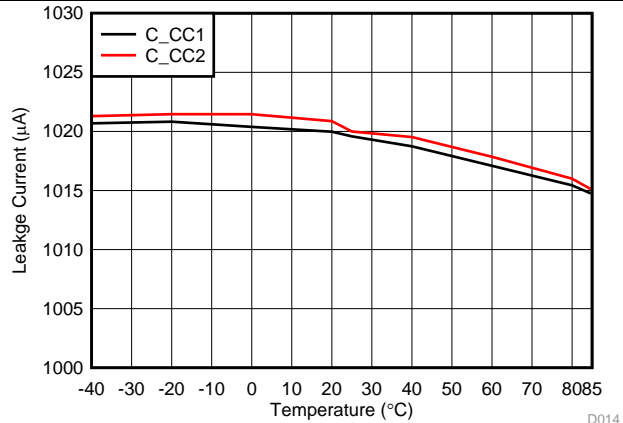


Figure 20. C_CC OVP Leakage Current vs Ambient Temperature at C_CC = 24 V

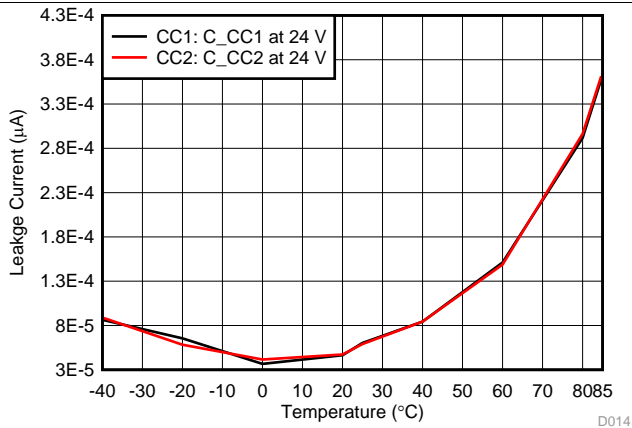


Figure 21. CC OVP Leakage Current vs Ambient Temperature at C_CC = 24 V

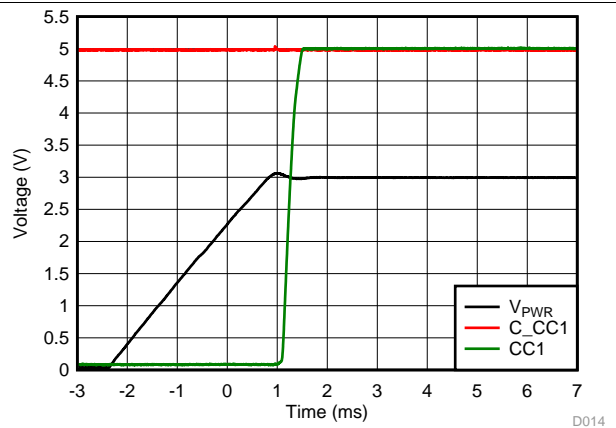


Figure 22. CC FET Turnon Timing

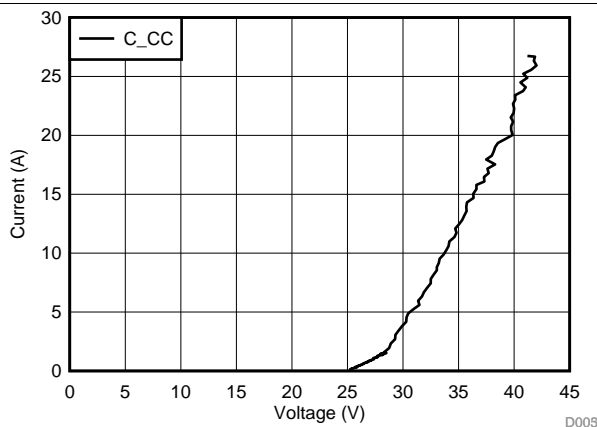


Figure 23. C_CC TLP Curve Unpowered

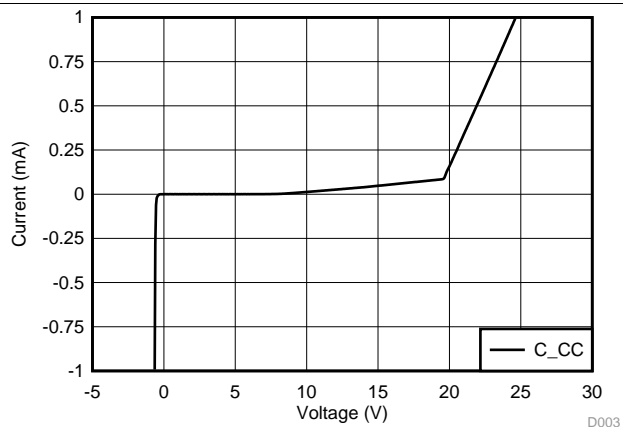


Figure 24. C_CC IV Curve

Typical Characteristics (continued)

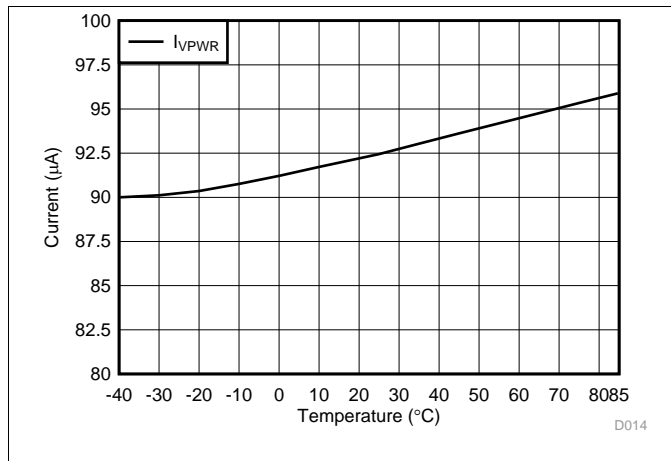


Figure 25. V_{PWR} Supply Leakage vs Ambient Temperature at 3.6 V

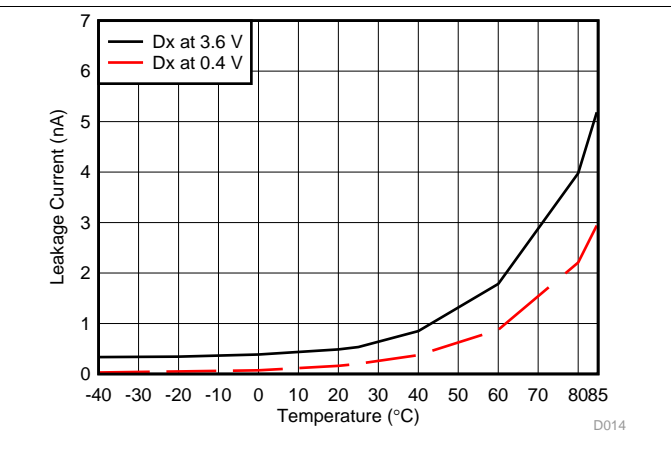


Figure 26. Dx Leakage Current vs Ambient Temperature at 0.4 V and 3.6 V

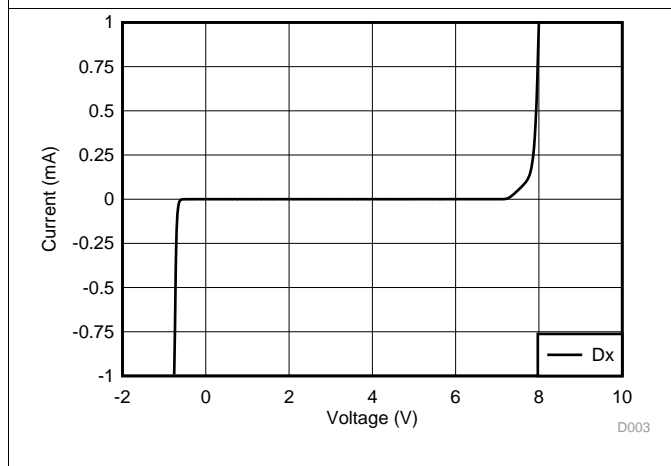


Figure 27. Dx IV Curve

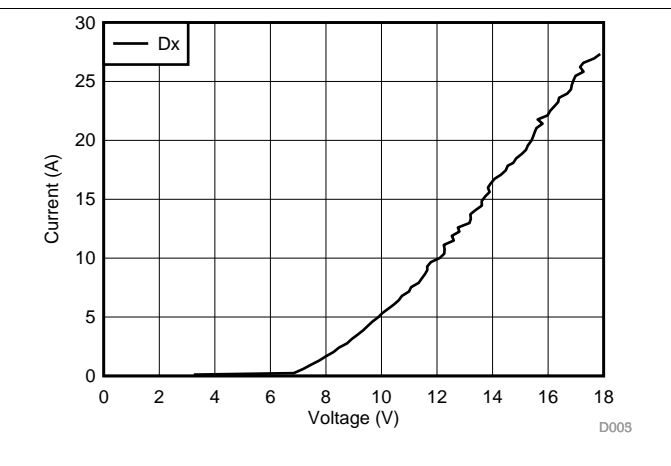


Figure 28. Dx TLP Curve

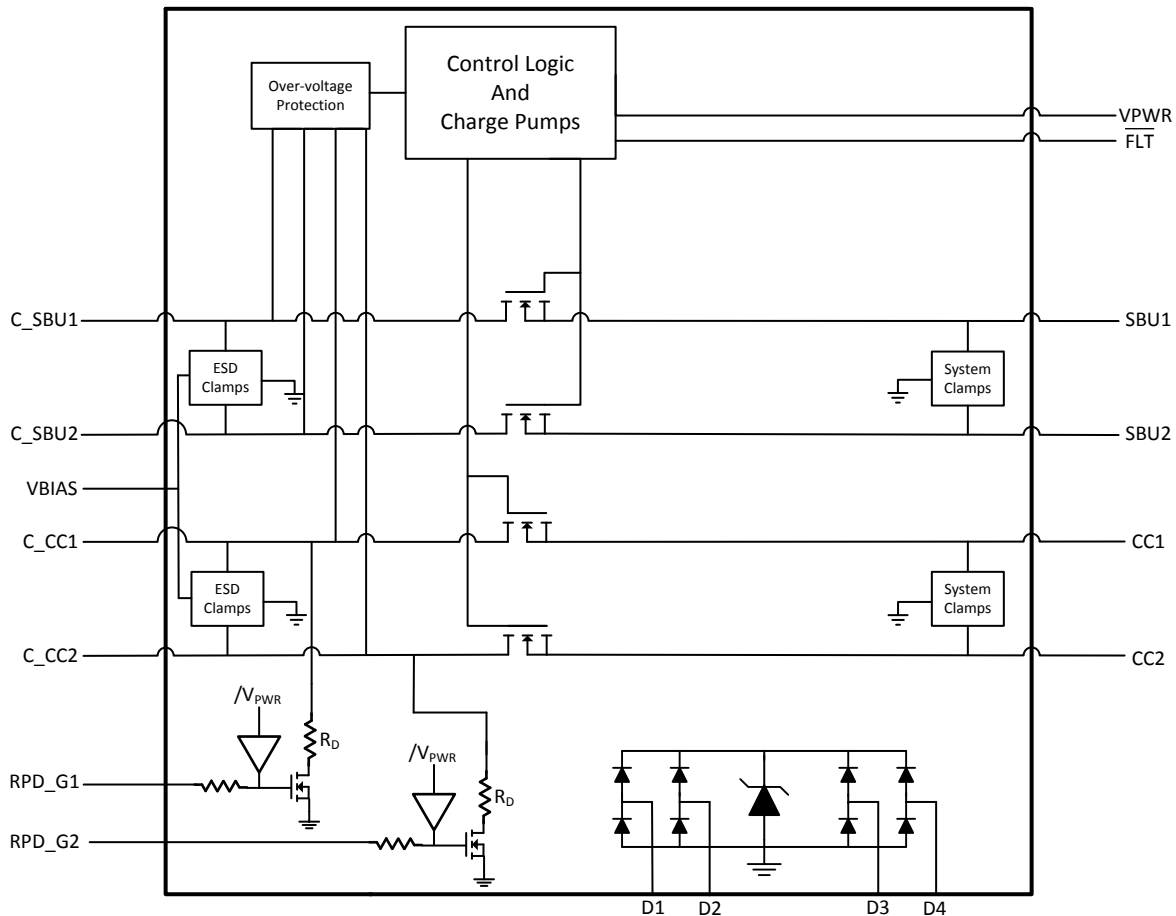
8 Detailed Description

8.1 Overview

The TPD8S300A is a single chip USB Type-C port protection solution that provides 20-V Short-to- V_{BUS} overvoltage and IEC ESD protection. Due to the small pin pitch of the USB Type-C connector and non-compliant USB Type-C cables and accessories, the V_{BUS} pins can get shorted to the CC and SBU pins inside the USB Type-C connector. Because of this short-to- V_{BUS} event, the CC and SBU pins need to be 20-V tolerant, to support protection on the full USB PD voltage range. Even if a device does not support 20-V operation on V_{BUS} , non-complaint adaptors can start out with 20-V V_{BUS} condition, making it necessary for any USB Type-C device to support 20 V protection. The TPD8S300A integrates four channels of 20-V Short-to- V_{BUS} overvoltage protection for the CC1, CC2, SBU1, and SBU2 pins of the USB Type-C connector.

Additionally, IEC 61000-4-2 system level ESD protection is required in order to protect a USB Type-C port from ESD strikes generated by end product users. The TPD8S300A integrates eight channels of IEC61000-4-2 ESD protection for the CC1, CC2, SBU1, SBU2, DP_T (Top side D+), DM_T (Top Side D–), DP_B (Bottom Side D+), and DM_B (Bottom Side D–) pins of the USB Type-C connector. This means IEC ESD protection is provided for all of the low-speed pins on the USB Type-C connector in a single chip in the TPD8S300A. Additionally, high-voltage IEC ESD protection that is 22-V DC tolerant is required for the CC and SBU lines in order to simultaneously support IEC ESD and Short-to- V_{BUS} protection; there are not many discrete market solutions that can provide this kind of protection. This high-voltage IEC ESD diode is what the TPD8S300A integrates, specifically designed to guarantee it works in conjunction with the overvoltage protection FETs inside the device. This sort of solution is very hard to generate with discrete components.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 4-Channels of Short-to- V_{BUS} Overvoltage Protection (CC1, CC2, SBU1, SBU2 Pins or CC1, CC2, DP, DM Pins): 24- V_{DC} Tolerant

The TPD8S300A provides 4-channels of Short-to- V_{BUS} Overvoltage Protection for the CC1, CC2, SBU1, and SBU2 pins (or the CC1, CC2, DP, and DM pins) of the USB Type-C connector. The TPD8S300A is able to handle 24- V_{DC} on its C_CC1, C_CC2, C_SBU1, and C_SBU2 pins. This is necessary because according to the USB PD specification, with V_{BUS} set for 20-V operation, the V_{BUS} voltage is allowed to legally swing up to 21 V and 21.5 V on voltage transitions from a different USB PD V_{BUS} voltage. The TPD8S300A builds in tolerance up to 24- V_{BUS} to provide margin above this 21.5-V specification to be able to support USB PD adaptors that may break the USB PD specification.

When a short-to- V_{BUS} event occurs, ringing happens due to the RLC elements in the hot-plug event. With very low resistance in this RLC circuit, ringing up to twice the settling voltage can appear on the connector. More than 2x ringing can be generated if any capacitor on the line derates its capacitance value during the short-to- V_{BUS} event. This means that more than 44 V could be seen on a USB Type-C pin during a Short-to- V_{BUS} event. The TPD8S300A has built in circuit protection to handle this ringing. The diode clamps used for IEC ESD protection also clamp the ringing voltage during the short-to- V_{BUS} event to limit the peak ringing to approximately 30 V. Additionally, the overvoltage protection FETs integrated inside the TPD8S300A are 30-V tolerant, therefore being capable of supporting the high-voltage ringing waveform that is experienced during the short-to- V_{BUS} event. The well designed combination of voltage clamps and 30-V tolerant OVP FETs insures the TPD8S300A can handle Short-to- V_{BUS} hot-plug events with hot-plug voltages as high as 24- V_{DC} .

Feature Description (continued)

The TPD8S300A has an extremely fast turnoff time of 70 ns typical. Furthermore, additional voltage clamps are placed after the OVP FET on the system side (CC1, CC2, SBU1, SBU2) pins of the TPD8S300A, to further limit the voltage and current that are exposed to the USB Type-C CC/PD controller during the 70 ns interval while the OVP FET is turning off. The combination of connector side voltage clamps, OVP FETs with extremely fast turnoff time, and system side voltage clamps all work together to insure the level of stress seen on a CC1, CC2, SBU1, or SBU2 pin during a short-to- V_{BUS} event is less than or equal to an HBM event. This is done by design, as any USB Type-C CC/PD controller will have built in HBM ESD protection.

The SBU OVP FETs were designed with a 1-GHz bandwidth to be able to be used to protect the DP, DM (USB2.0) pins in addition to the SBU pins. Some systems designers also prefer to protect the DP, DM pins from Short-to- V_{BUS} events due to the potential for moisture/water in the connector to short the V_{BUS} pins to DP, DM pins. This can be especially applicable in cases where the end equipment with a USB Type-C connector is trying to be made water-proof. If desiring to protect the DP, DM pins on the USB Type-C connector from a Short-to- V_{BUS} event, connect the C_SBUx pins to the DP, DM pins on the USB Type-C connector, and the SBUx pins to the USB2.0 pins of the system device being protected from the Short-to- V_{BUS} event.

Figure 29 is an example of the TPD8S300A successfully protecting the TPS65982, the world's first fully integrated, full-featured USB Type-C and PD controller.

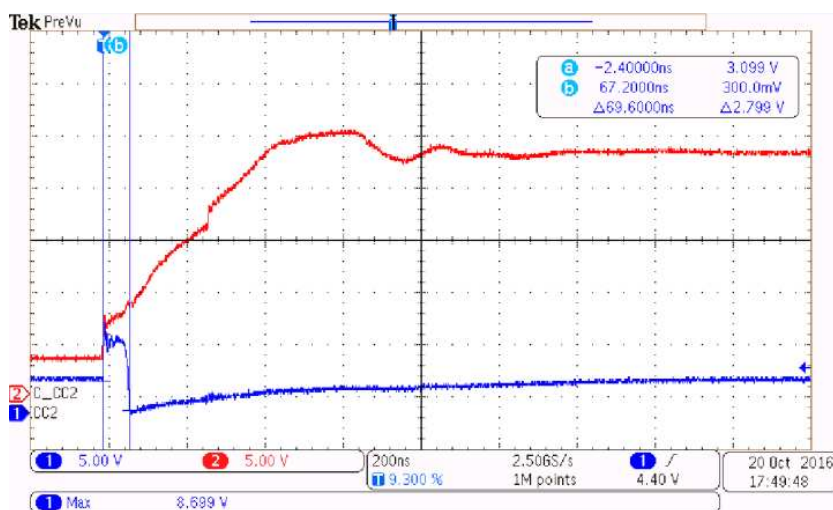


Figure 29. TPD8S300A Protecting the TPS65982 During a Short-to- V_{BUS} Event

8.3.2 8-Channels of IEC 61000-4-2 ESD Protection (CC1, CC2, SBU1, SBU2, DP_T, DM_T, DP_B, DM_B Pins)

The TPD8S300A integrates 8-Channels of IEC 61000-4-2 system level ESD protection for the CC1, CC2, SBU1, SBU2, DP_T (Top side D+), DM_T (Top Side D-), DP_B (Bottom Side D+), and DM_B (Bottom Side D-) pins. USB Type-C ports on end-products need system level IEC ESD protection in order to provide adequate protection for the ESD events that the connector can be exposed to from end users. The TPD8S300A integrates IEC ESD protection for all of the low-speed pins on the USB Type-C connector in a single chip. Also note, that while the RPD_Gx pins are not individually rated for IEC ESD, when they are shorted to the C_CCx pins, the C_CCx pins provide protection for both the C_CCx pins and the RPD_Gx pins. Additionally, high-voltage IEC ESD protection that is 24-V DC tolerant is required for the CC and SBU lines in order to simultaneously support IEC ESD and Short-to- V_{BUS} protection; there are not many discrete market solutions that can provide this kind of protection. The TPD8S300A integrates this type of high-voltage ESD protection so a system designer can meet both IEC ESD and Short-to- V_{BUS} protection requirements in a single device.

Feature Description (continued)

8.3.3 CC1, CC2 Overvoltage Protection FETs 600 mA Capable for Passing VCONN Power

The CC pins on the USB Type-C connector serve many functions; one of the functions is to be a provider of power to active cables. Active cables are required when desiring to pass greater than 3 A of current on the V_{BUS} line or when the USB Type-C port uses the super-speed lines (TX1+, TX2-, RX1+, RX1-, TX2+, TX2-, RX2+, RX2-). When CC is configured to provide power, it is called VCONN. VCONN is a DC voltage source in the range of 3 V to 5.5 V. If supporting VCONN, a VCONN provider must be able to provide 1 W of power to a cable; this translates into a current range of 200 mA to 333 mA (depending on your VCONN voltage level). Additionally, if operating in a USB PD alternate mode, greater power levels are allowed on the VCONN line.

When a USB Type-C port is configured for VCONN and using the TPD8S300A, this VCONN current flows through the OVP FETs of the TPD8S300A. Therefore, the TPD8S300A has been designed to handle these currents and have an RON low enough to provide a specification compliant VCONN voltage to the active cable. The TPD8S300A is designed to handle up to 600 mA of DC current to allow for alternate mode support in addition to the standard 1 W required by the USB Type-C specification.

8.3.4 CC Dead Battery Resistors Integrated for Handling the Dead Battery Use Case in Mobile Devices

An important feature of USB Type-C and USB PD is the ability for this connector to serve as the sole power source to mobile devices. With support up to 100 W, the USB Type-C connector supporting USB PD can be used to power a whole new range of mobile devices not previously possible with legacy USB connectors.

When the USB Type-C connector is the sole power supply for a battery powered device, the device must be able to charge from the USB Type-C connector even when its battery is dead. In order for a USB Type-C power adaptor to supply power on V_{BUS} , RD pulldown resistors must be exposed on the CC pins. These RD resistors are typically included inside a USB Type-C CC/PD controller. However, when the TPD8S300A is used to protect the USB Type-C port, the OVP FETs inside the device isolate these RD resistors in the CC/PD controller when the mobile device has no power. This is because when the TPD8S300A has no power, the OVP FETs are turned off to guarantee overvoltage protection in a dead battery condition. Therefore, the TPD8S300A integrates high-voltage, dead battery RD pull-down resistors to allow dead battery charging simultaneously with high-voltage OVP protection.

If dead battery support is required, short the RPD_G1 pin to the C_CC1 pin, and short the RPD_G2 pin to the C_CC2 pin. This connects the dead battery resistors to the connector CC pins. When the TPD8S300A is unpowered, and the RP pull-up resistor is connected from a power adaptor, this RP pull-up resistor activates the RD resistor inside the TPD8S300A. This enables V_{BUS} to be applied from the power adaptor even in a dead battery condition. Once power is restored back to the system and back to the TPD8S300A on its VPWR pin, the TPD8S300A turns ON its OVP FETs in 3.5 ms and then turns OFF its dead battery RD. The TPD8S300A first turns ON its CC OVP FETs fully, and then removes its dead battery RDs. This is to make sure the PD controller RD is fully exposed before removing the RD of the TPD8S300A. This is to help ensure the USB Type-C source remains attached because a USB Type-C sink must have an RD present on CC at all times to guarantee according to the USB Type-C spec that the USB Type-C source remains attached.

If desiring to power the CC/PD controller during dead battery mode and if the CC/PD Controller is configured as a DRP, it is critical that the TPD8S300A be powered before or at the same time that the CC/PD controller is powered. It is also critical that when unpowered, the CC/PD controller also expose its dead battery resistors. When the TPD8S300A gets powered, it exposes the CC pins of the CC/PD controller within 3.5 ms, and then removes its own RD dead battery resistors. Once the TPD8S300A turns on, the RD pull-down resistors of the CC/PD controller must be present immediately, in order to guarantee the power adaptor connected to power the dead battery device keeps its V_{BUS} turned on. If the power adaptor does not see RD present, it can disconnect V_{BUS} . This removes power from the device with its battery still not sufficiently charged, which consequently removes power from the CC/PD controller and the TPD8S300A. Then the RD resistors of the TPD8S300A are exposed again, and connects the power adaptor's V_{BUS} to start the cycle over. This creates an infinite loop, never or very slowly charging the mobile device.

Feature Description (continued)

If the CC/PD Controller is configured for DRP and has started its DRP toggle before the TPD8S300A turns on, this DRP toggle is unable to guarantee that the power adaptor does not disconnect from the port. Therefore, it is recommended if the CC/PD controller is configured for DRP, that its dead battery resistors be exposed as well, and that they remain exposed until the TPD8S300A turns on. This is typically accomplished by powering the TPD8S300A at the same time as the CC/PD controller when powering the CC/PD controller in dead battery operation. When protecting the TPS6598x family of PD controllers with TPD8S300A, this is accomplished by powering TPD8S300A from TPS6598x's LDO_3V3 pin (connect TPS6598x's LDO_3V3 pin to TPD8S300A's V_{PWR} pin).

If dead battery charging is not required in your application, connect the RPD_G1 and RPD_G2 pins to ground.

8.3.5 Advantages over TPD8S300

8.3.5.1 Improved Dead Battery Performance

The TPD8S300A has improved dead battery performance over TPD8S300. In the TPD8S300 when the device is first powered (V_{PWR} pin goes from 0V to 3.3V), the CC RD dead battery resistors are disabled at the same time the CC OVP FETs are enabled. This leads to a small ~400us time window where the CC pin can float up above the SRC.RD voltage threshold because the CC OVP FETs are still too resistive for the source to detect RD from the USB-PD controller. If the tSRCDisconnect debounce time of the USB Type-C source is less than ~400us, this could cause a USB Type-C disconnect for the source port during the dead battery boot-up event. Many USB Type-C Sources do not have a tSRCDisconnect debounce time less than ~400us; however, the USB Type-C spec allows the tSRCDisconnect time to be as low as 0ms, so some USB Type-C sources may have a tSRCDisconnect debounce time that is less than ~400us. TPD8S300A solves this problem. When the TPD8S300A is first powered (V_{PWR} pin goes from 0V to 3.3V), TPD8S300A waits for its CC OVP FETs to be completely ON before it removes its RD dead battery resistors. This guarantees that an RD resistor will always be present on the CC line during the dead battery boot-up, and that the USB Type-C source's CC voltage will always stay in the SRC.RD range; therefore, even if a source had a tSRCDisconnect debounce time of 0ms, it will remain connected. See [Figure 32](#) for an oscilloscope capture of TPD8S300A's proper dead battery boot-up behavior.

8.3.5.2 USB Type-C Port Stays Connected during an IEC 61000-4-2 ESD Strike

The TPD8S300A will also make sure the USB Type-C ports stay connected, even during an IEC 61000-4-2 ESD strike, whereas the TPD8S300 has the potential to cause a USB Type-C port disconnect during an IEC 61000-4-2 ESD strike. In TPD8S300, in some PCB layouts an IEC 61000-4-2 ESD strike would cause TPD8S300 to go into the OVP state. In TPD8S300, the CC OVP recovery time was 21ms minimum. This means that if an OVP happened in TPD8S300, a USB-C disconnect was guaranteed to happen, because the maximum USB Type-C port disconnect time for sources and sinks is 20ms max in the USB Type-C specification. However, in TPD8S300A, the CC OVP recovery time is 0.93ms typical. For TPD8S300A, the OVP FET will turn back ON much faster than a sinks minimum disconnect time, which is 10ms. So even if an IEC 61000-4-2 ESD strike causes an OVP in TPD8S300A, the new CC OVP FET recovery time of 0.93ms will not cause a disconnect on the USB Type-C port for a sink.

For a source port connected to a sink with a TPD8S300A, if an IEC 61000-4-2 ESD strike occurs that causes an OVP event, even an OVP recovery time of 0.93ms could cause a disconnect, because for source USB Type-C ports, they have a minimum disconnect time of 0ms in the USB Type-C specification. So the CC OVP FET in TPD8S300A would open up and hide the PD controllers RD for 0.93ms, causing a potential for a disconnect on the source USB Type-C port. To solve this problem, TPD8S300A turns on its dead battery RD resistor in an OVP event caused by an IEC 61000-4-2 ESD strike while the CC OVP FET is OFF. This makes it so even during this OVP event caused by IEC ESD, the source port connected to the sink port with TPD8S300A will always see an RD resistor. Therefore, even if the source port has an extremely low tSrcDisconnect time close to 0ms, it will remain connected because an RD resistor is always present on its CC pin.

8.3.6 3-mm × 3-mm WQFN Package

The TPD8S300A comes in a small, 3-mm × 3-mm WQFN package, greatly reducing the size of implementing a similar protection solution discretely. The WQFN package allows support for a wider range of PCB designs.

8.4 Device Functional Modes

Table 1 describes all of the functional modes for the TPD8S300A. The "X" in the below table are "do not care" conditions, meaning any value can be present within the absolute maximum ratings of the datasheet and maintain that functional mode. Also note the D1, D2, D3, and D4 pins are not listed, because these pins have IEC ESD protection diodes that are always present, regardless of whether the device is powered and regardless of the conditions on any of the other pins.

Table 1. Device Mode Table

Device Mode Table		Inputs					Outputs		
MODE		VPWR	C_CCx	C_SBUx	RPD_Gx	T _J	FLT	CC FETs	SBU FETs
Normal Operating Conditions	Unpowered, no dead battery support	<UVLO	X	X	Grounded	X	High-Z	OFF	OFF
	Unpowered, dead battery support	<UVLO	X	X	Shorted to C_CCx	X	High-Z	OFF	OFF
	Powered on	>UVLO	<OVP	<OVP	X, forced OFF	<TSD	High-Z	ON	ON
Fault Conditions	Thermal shutdown	>UVLO	X	X	X, forced OFF	>TSD	Low (Fault Asserted)	OFF	OFF
	CC over voltage condition	>UVLO	>OVP	X	X, forced OFF	<TSD	Low (Fault Asserted)	OFF	OFF
	SBU over voltage condition	>UVLO	X	>OVP	X, forced OFF	<TSD	Low (Fault Asserted)	OFF	OFF
	IEC ESD generated over voltage condition ⁽¹⁾	>UVLO	X	X	R _D ON if RPD_Gx is shorted to C_CCx	<TSD	Low (Fault Asserted)	OFF	OFF

- (1) This row describes the state of the device while still in OVP after the IEC ESD strike which put the device into OVP is over, and the voltages on the C_CCx and C_SBUx pins have returned to their normal voltage levels.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPD8S300A provides 4-channels of Short-to- V_{BUS} overvoltage protection for the CC1, CC2, SBU1, and SBU2 pins of the USB Type-C connector, and 8-channels of IEC ESD protection for the CC1, CC2, SBU1, SBU2, DP_T, DM_T, DP_B, DM_B pins of the USB Type-C connector. Care must be taken to insure that the TPD8S300A provides adequate system protection as well as insuring that proper system operation is maintained. The following application example explains how to properly design the TPD8S300A into a USB Type-C system.

9.2 Typical Application

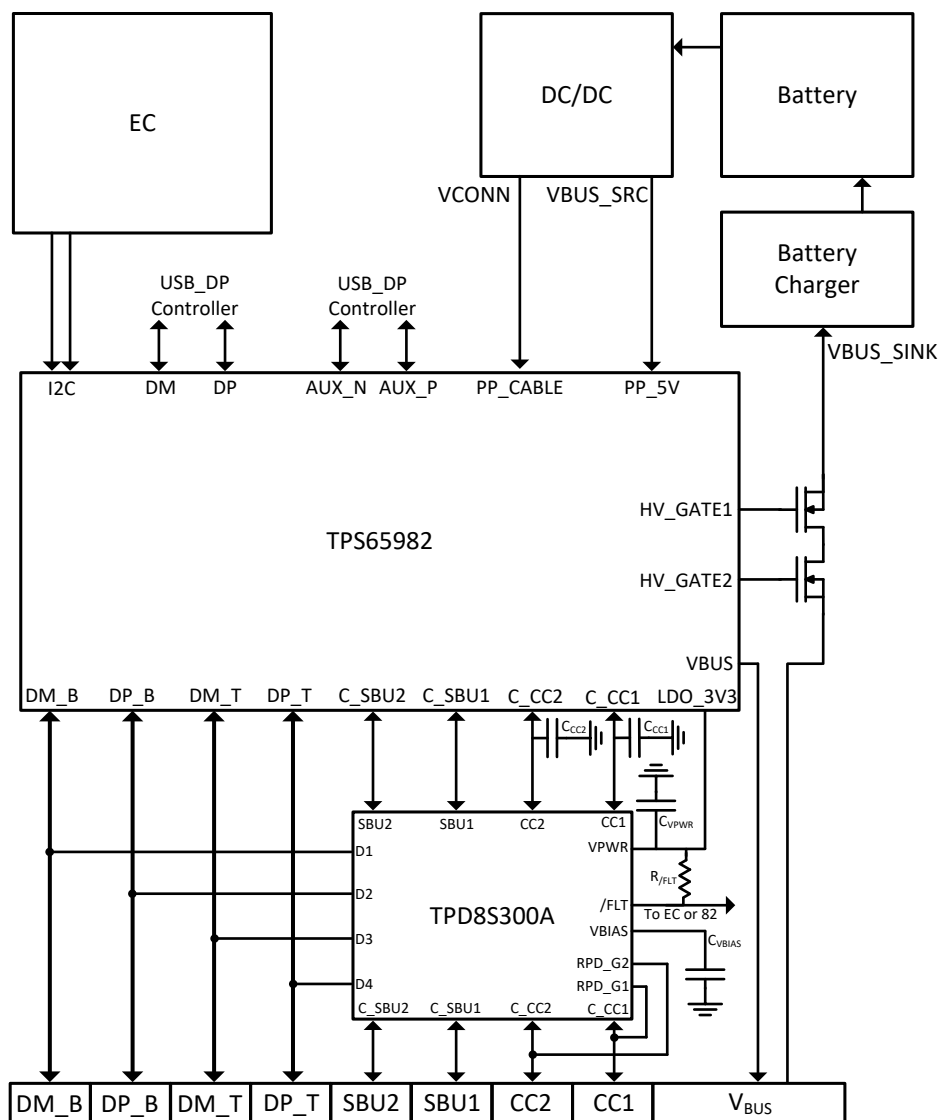


Figure 30. TPD8S300A Typical Application Diagram

Typical Application (continued)

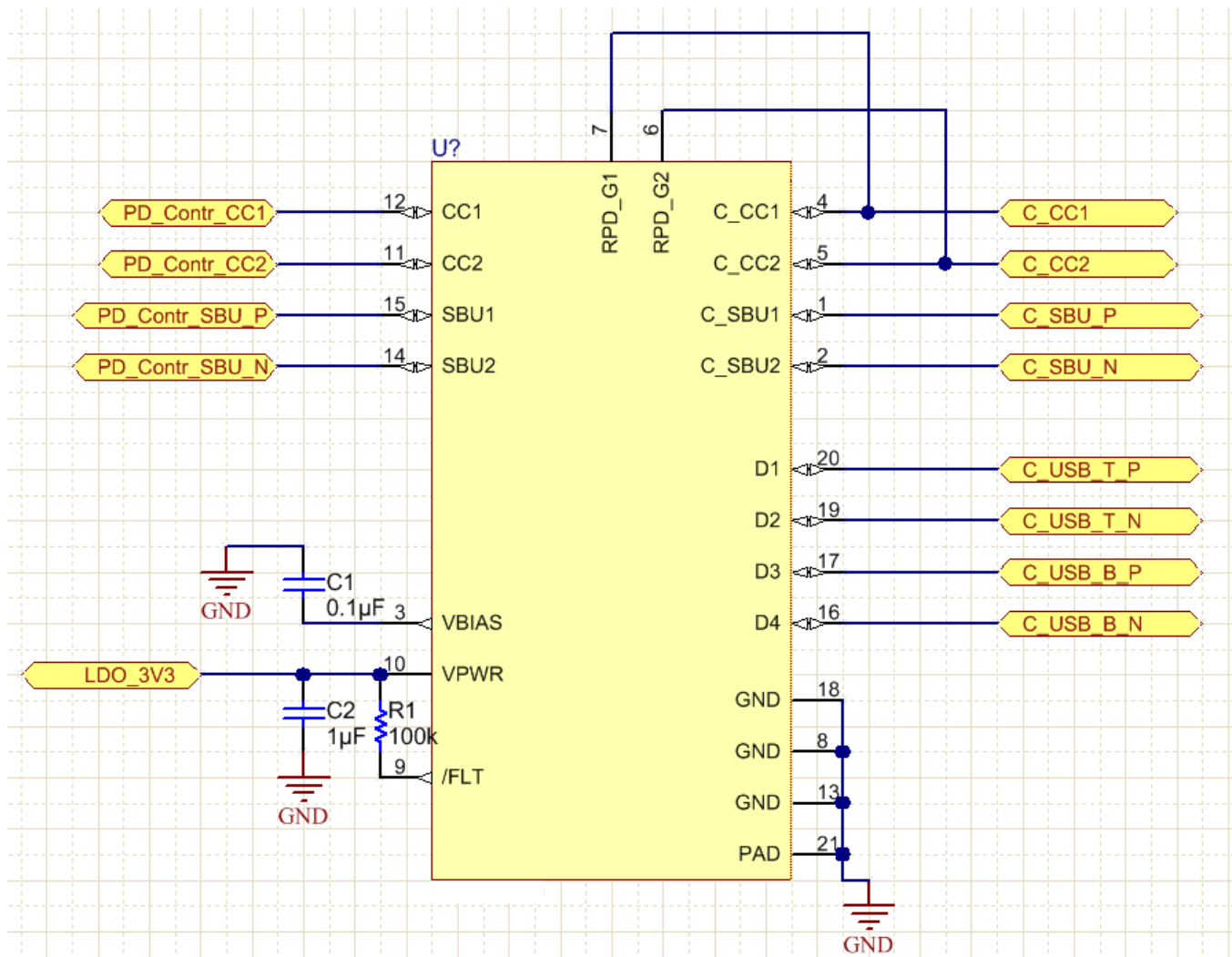


Figure 31. TPD8S300A Reference Schematic

9.2.1 Design Requirements

In this application example we study the protection requirements for a full-featured USB Type-C DRP Port, fully equipped with USB-PD, USB2.0, USB3.0, Display Port, and 100 W charging. The [TPS65982](#) is used to easily enable a full-featured port with a single chip solution. In this application, all the pins of the USB Type-C connector are utilized. Both the CC and SBU pins are susceptible to shorting to the V_{BUS} pin. With 100 W charging, V_{BUS} operates at 20 V, requiring the CC and SBU pins to tolerate $20-V_{DC}$. Additionally, the CC, SBU, and USB2.0 pins require IEC system level ESD protection. With these protection requirements present for the USB Type-C connector, the TPD8S300A is utilized. The TPD8S300A is a single chip solution that provides all the required protection for the low speed and USB2.0 pins in the USB Type-C connector.

Table 2 lists the TPD8S300A design parameters.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{BUS} nominal operating voltage	20 V
Short-to- V_{BUS} tolerance for the CC and SBU pins	24 V
VBIAS nominal capacitance	0.1 μ F

Table 2. Design Parameters (continued)

DESIGN PARAMETER	EXAMPLE VALUE
Dead battery charging	100 W
Maximum ambient temperature requirement	85°C

9.2.2 Detailed Design Procedure

9.2.2.1 VBIAS Capacitor Selection

As noted in the [Recommended Operating Conditions](#) table, a minimum of 35- V_{BUS} rated capacitor is required for the VBIAS pin, and a 50- V_{BUS} capacitor is recommended. The VBIAS capacitor is in parallel with the central IEC diode clamp integrated inside the TPD8S300A. A forward biased hiding diode connects the VBIAS pin to the C_CCx and C_SBUx pins. Therefore, when a Short-to- V_{BUS} event occurs at 20 V, 20- V_{BUS} minus a forward biased diode drop is exposed to the VBIAS pin. Additionally, during the short-to- V_{BUS} event, ringing can occur almost double the settling voltage of 20 V, allowing a potential 40 V to be exposed to the C_CCx and C_SBUx pins. However, the internal IEC clamps limit the voltage exposed to the C_CCx and C_SBUx pins to around 30 V. Therefore, at least 35- V_{BUS} capacitor is required to insure the VBIAS capacitor does not get destroyed during Short-to- V_{BUS} events.

A 50-V, X7R capacitor is recommended, however. This is to further improve the derating performance of the capacitors. When the voltage across a real capacitor is increased, its capacitance value derates. The more the capacitor derates, the greater than 2x ringing can occur in the short-to- V_{BUS} RLC circuit. 50-V X7R capacitors have great derating performance, allowing for the best short-to- V_{BUS} performance of the TPD8S300A.

Additionally, the VBIAS capacitor helps pass IEC 61000-4-2 ESD strikes. The more capacitance present, the better the IEC performance. So the less the VBIAS capacitor derates, the better the IEC performance. [Table 3](#) shows real capacitors recommended to achieve the best performance with the TPD8S300A.

Table 3. Design Parameters

CAPACITOR SIZE	PART NUMBER
0402	CC0402KRX7R9BB104
0603	GRM188R71H104KA93D

9.2.2.2 Dead Battery Operation

For this application, we want to support 100-W dead battery operation; when the laptop is out of battery, we still want to charge the laptop at 20 V and 5 A. This means that the USB PD Controller must receive power in dead battery mode. The TPS65982 has its own built in LDO in order to supply the TPS65982 power from V_{BUS} in a dead battery condition. The TPS65982 can also provide power to its flash during this condition through its LDO_3V3 pin.

The OVP FETs of the TPD8S300A remain OFF when it is unpowered in order to insure in a dead battery situation proper protection is still provided to the PD controller in the system, in this case the TPS65982. However, when the OVP FETs are OFF, this isolates the TPS65982s dead battery resistors from the USB Type-C ports CC pins. A USB Type-C power adaptor must see the RD pull-down dead battery resistors on the CC pins or it does not provide power on V_{BUS} . Since the TPS65982s dead battery resistors are isolated from the USB Type-C connector's CC pins, the built-in, dead battery resistors of the TPD8S300A must be connected. Short the RPD_G1 pin to the C_CC1 pin, and short the RPD_G2 pin to the C_CC2 pin.

Once the power adaptor sees the dead battery resistors of the TPD8S300A, it applies 5 V on the V_{BUS} pin. This provides power to the TPS65982, turning the PD controller on, and allowing the battery to begin to charge. However, this application requires 100 W charging in dead battery mode, so V_{BUS} at 20 V and 5 A is required. USB PD negotiation is required to accomplish this, so the TPS65982 needs to be able to communicate on the CC pins. This means the TPD8S300A needs to be turned on in dead battery mode as well so the TPS65982s PD controller can be exposed to the CC lines. To accomplish this, it is critical that the TPD8S300A is powered by the TPS65982s internal LDO, the LDO_3V3 pin. This way, when the TPS65982 receives power on V_{BUS} , the TPD8S300A is turned on simultaneously.

It is critical that the TPS65982's dead battery resistors are also connected to its CC pins for dead battery operation. Short the TPS65982s RPD_G1 pin to its C_CC1 pin, and its RPD_G2 pin to its C_CC2 pin. It is critical that the TPS65982s dead battery resistors are present; once the TPD8S300A receives power, turns on its OVP FETs and then removes its dead battery RD resistor, TPS65982's RD pull-down resistors must be present on the CC line in order to guarantee the power adaptor stays connected. If RD is not present the power adaptor will eventually interpret this as a disconnect and remove V_{BUS} .

Also, it is important that the TPS65982's dead battery resistors are present so it properly boots up in dead battery operation with the correct voltages on its CC pins.

Once this process has occurred, the TPS65982 can start negotiating with the power adaptor through USB PD for higher power levels, allowing 100-W operation in dead battery mode.

For more information on the TPD8S300A dead battery operation, see the [CC Dead Battery Resistors Integrated for Handling the Dead Battery Use Case in Mobile Devices](#) section of the datasheet.

9.2.2.3 CC Line Capacitance

USB PD has a specification for the total amount of capacitance that is required for proper USB PD BMC operation on the CC lines. The specification from section 5.8.6 of the [USB PD Specification](#) is given below in [Table 4](#).

Table 4. USB PD cReceiver Specification

NAME	DESCRIPTION	MIN	MAX	UNIT	COMMENT
cReceiver	CC receiver capacitance	200	600	pF	The DFP or UFP system shall have capacitance within this range when not transmitting on the line

Therefore, the capacitance on the CC lines must stay in between 200 pF and 600 pF when USB PD is being used. Therefore, the combination of capacitances added to the system by the TPS65982, the TPD8S300A, and any external capacitor must fall within these limits. [Table 5](#) shows the analysis involved in choosing the correct external CC capacitor for this system, and shows that an external CC capacitor is required.

Table 5. CC Line Capacitor Calculation

CC Capacitance	MIN	MAX	UNIT	COMMENT
CC line target capacitance	200	600	pF	From the USB PD Specification section
TPS65982 capacitance	70	120	pF	From the TPS65982 Datasheet
TPD8S300A capacitance	60	120	pF	From the Electrical Characteristics table.
Proposed capacitor GRM033R71E221KA01D	110	330	pF	CAP, CERM, 220 pF, 25 V, ±10%, X7R, 0201 (For min and max, assume ±50% capacitance change with temperature and voltage derating to be overly conservative)
TPS65982 + TPD8S300A + GRM033R71E221KA01D	240	570	pF	Meets USB PD cReceiver specification

9.2.2.4 Additional ESD Protection on CC and SBU Lines

If additional IEC ESD protection is desired to be placed on either the CC or SBU lines, it is important that high-voltage ESD protection diodes be used. The maximum DC voltage that can be seen in USB PD is $21 \cdot V_{BUS}$, with 21.5 V allowed during voltage transitions. Therefore, an ESD protection diode must have a reverse stand off voltage higher than 21.5 V in order to guarantee the diode does not breakdown during a short-to- V_{BUS} event and have large amounts of current flowing through it indefinitely, destroying the diode. A reverse stand off voltage of 24 V is recommended to give margin above 21.5 V in case USB Type-C power adaptors are released in the market which break the USB Type-C specification.

Furthermore, due to the fact that the Short-to- V_{BUS} event applies a DC voltage to the CC and SBU pins, a deep-snap-back diode cannot be used unless its minimum trigger voltage is above 42 V. During a Short-to- V_{BUS} event, RLC ringing of up to 2x the settling voltage can be exposed to CC and SBU, allowing for up to 42 V to be exposed. Furthermore, if any capacitor derates on the CC or SBU line, greater than 2x ringing can occur. Since this ringing is hard to bound, it is recommended to not use deep-snap-back diodes. If the deep-snap-back diode triggers during the short-to- V_{BUS} hot-plug event, it begins to operate in its conduction region. With a $20 \cdot V_{BUS}$ source present on the CC or SBU line, this allows the diode to conduct indefinitely, destroying the diode.

9.2.2.5 \overline{FLT} Pin Operation

Once a Short-to- V_{BUS} occurs on the C_CCx or C_SBUx pins, the \overline{FLT} pin is asserted in 20 μ s (typical) so the PD controller can be notified quickly. If V_{BUS} is being shorted to CC or SBU, it is recommended to respond to the event by forcing a detach in the USB PD controller to remove V_{BUS} from the port. Although the USB Type-C port using the TPD8S300A is not damaged, as the TPD8S300A provides protection from these events, the other device connected through the USB Type-C Cable or any active circuitry in the cable can be damaged. Although shutting the V_{BUS} off through a detach does not guarantee it stops the other device or cable from being damaged, it can mitigate any high current paths from causing further damage after the initial damage takes place. Additionally, even if the active cable or other device does have proper protection, the short-to- V_{BUS} event may corrupt a configuration in an active cable or in the other PD controller, so it is best to detach and reconfigure the port.

9.2.2.6 How to Connect Unused Pins

If either the RPD_Gx pins or any of the Dx pins are unused in a design, they must be connected to GND.

9.2.3 Application Curves

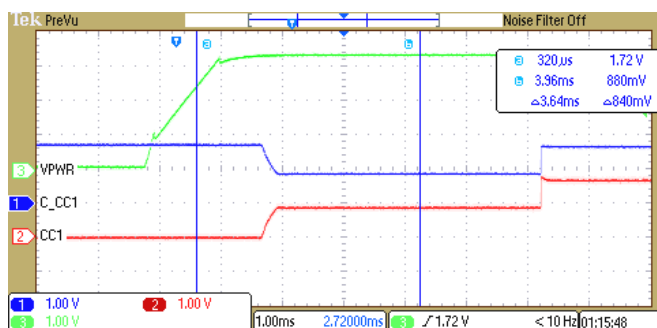


Figure 32. TPD8S300A Turning On in Dead Battery Mode with R_D on CC1

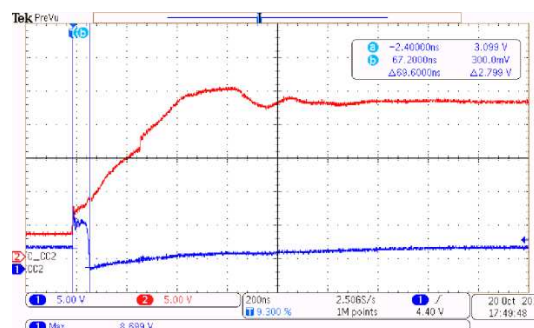


Figure 33. TPD8S300A Protecting the TPS65982 During a Short-to- V_{BUS} Event

10 Power Supply Recommendations

The V_{PWR} pin provides power to all the circuitry in the TPD8S300A. It is recommended a 1- μ F decoupling capacitor is placed as close as possible to the VPWR pin. If USB PD is desired to be operated in dead battery conditions, it is critical that the TPD8S300A share the same power supply as the PD controller in dead battery boot-up (such as sharing the same dead battery LDO). See the [CC Dead Battery Resistors Integrated for Handling the Dead Battery Use Case in Mobile Devices](#) section for more details.

11 Layout

11.1 Layout Guidelines

Proper routing and placement is important to maintain the signal integrity the USB2.0, SBU, CC line signals. The following guidelines apply to the TPD8S300A:

- Place the bypass capacitors as close as possible to the V_{PWR} pin, and ESD protection capacitor as close as possible to the V_{BIAS} pin. Capacitors must be attached to a solid ground. This minimizes voltage disturbances during transient events such as short-to- V_{BUS} and ESD strikes.
- The USB2.0 and SBU lines must be routed as straight as possible and any sharp bends must be minimized.

Standard ESD recommendations apply to the C_CC1, C_CC2, C_SBU1, C_SBU2, D1, D2, D3, and D4 pins as well:

- The optimum placement for the device is as close to the connector as possible:
 - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
 - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TPD8S300A and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
 - Electric fields tend to build up on corners, increasing EMI coupling.
- It is best practice to not via up to the D1, D2, D3, and D4 pins from a trace routed on another layer. Rather, it is better to via the trace to the layer with the Dx pin, and to continue that trace on that same layer. See the [ESD Protection Layout Guide](#) application report, section 1.3 for more details.

11.2 Layout Example

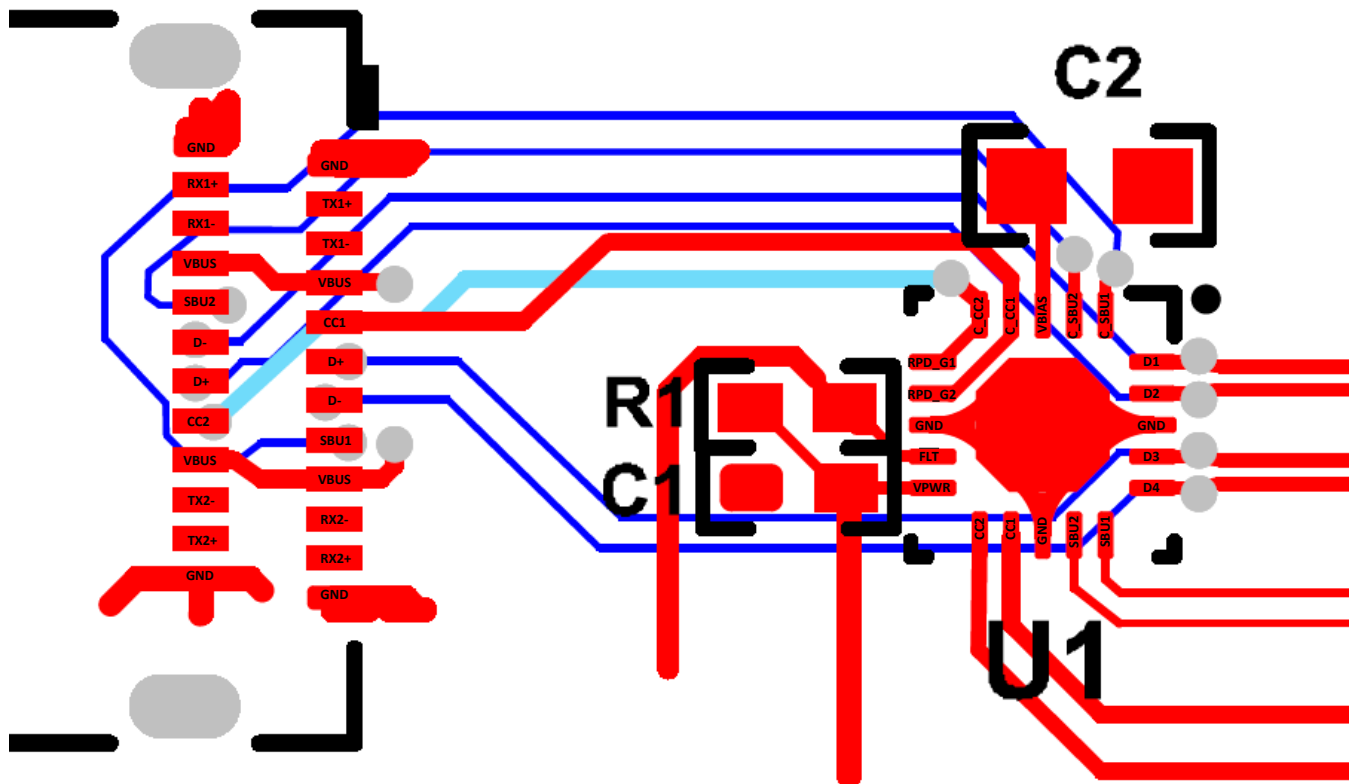


Figure 34. TPD8S300A Typical Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

[TPD6S300 Evaluation Module User's Guide](#)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.

USB Type-C is a trademark of USB Implementers Forum.

All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD8S300ARUKR	ACTIVE	WQFN	RUK	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	8S30A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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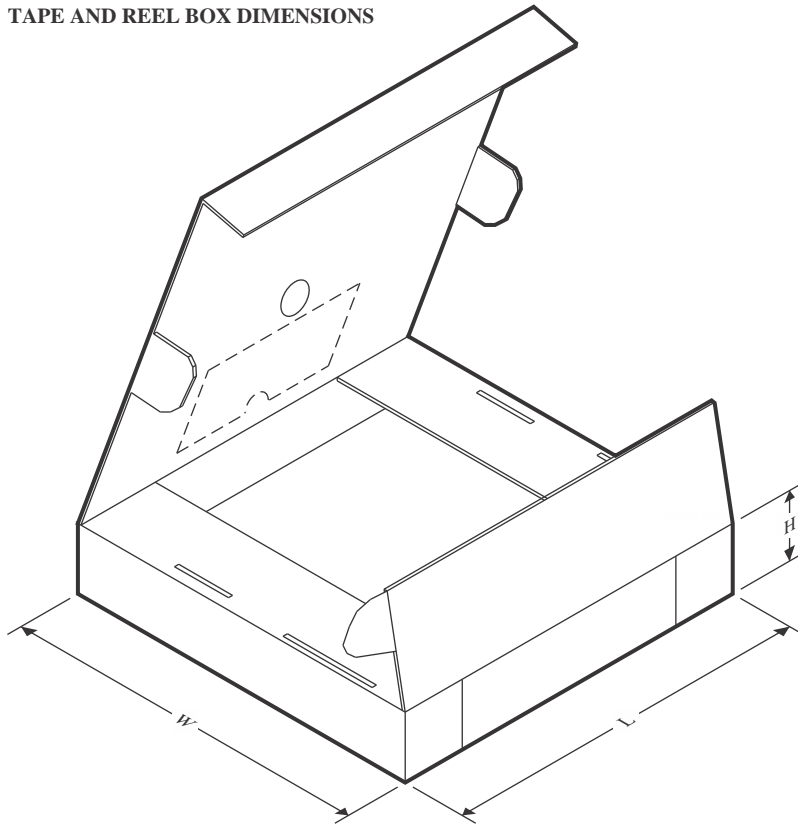
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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD8S300ARUKR	WQFN	RUK	20	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD8S300ARUKR	WQFN	RUK	20	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

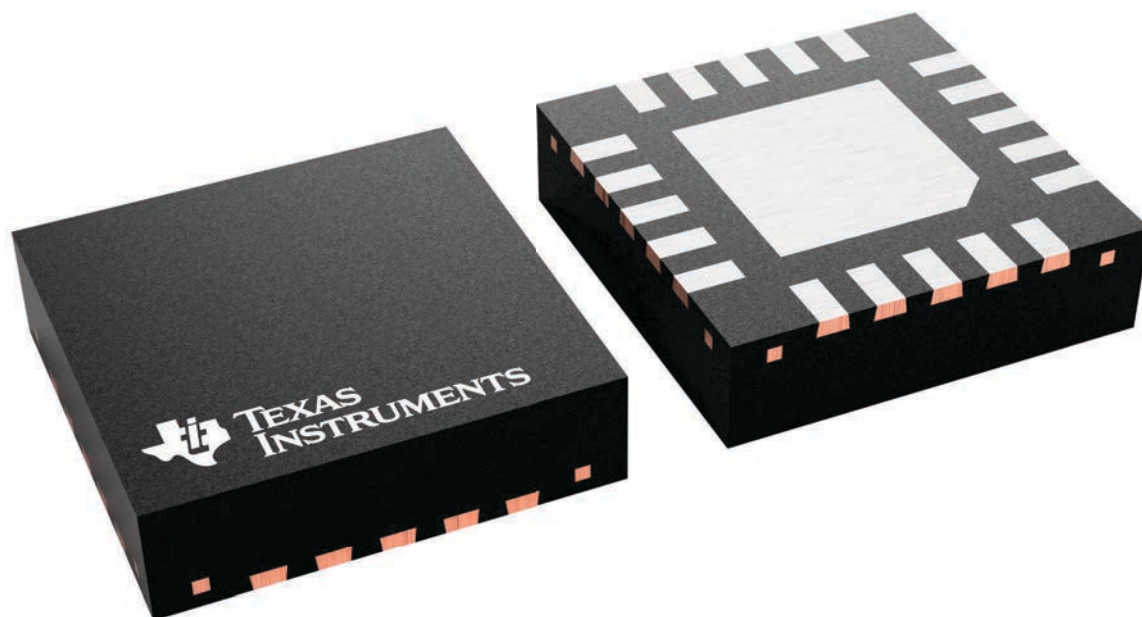
RUK 20

WQFN - 0.8 mm max height

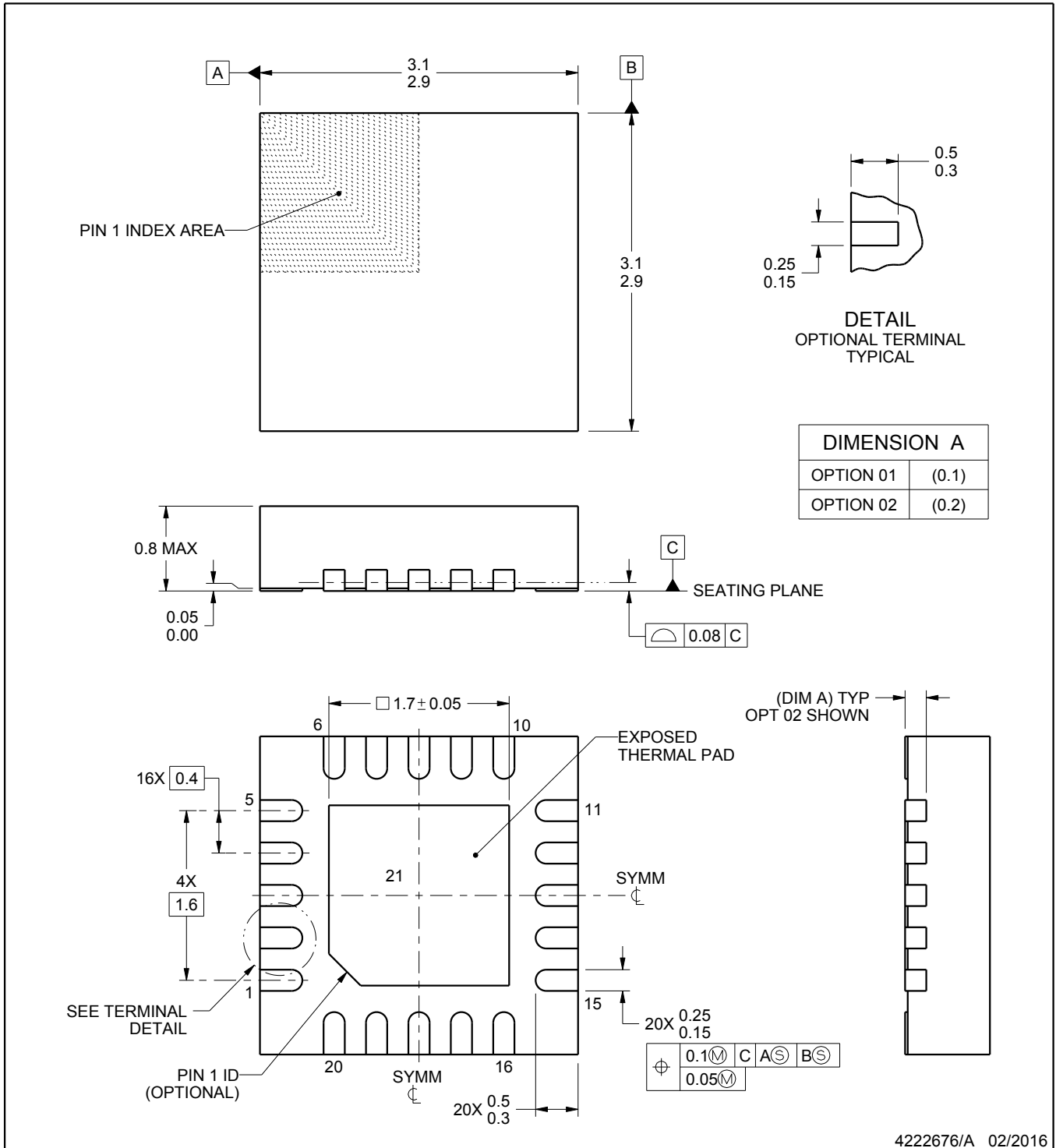
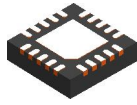
3 x 3, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229651/A



4222676/A 02/2016

NOTES:

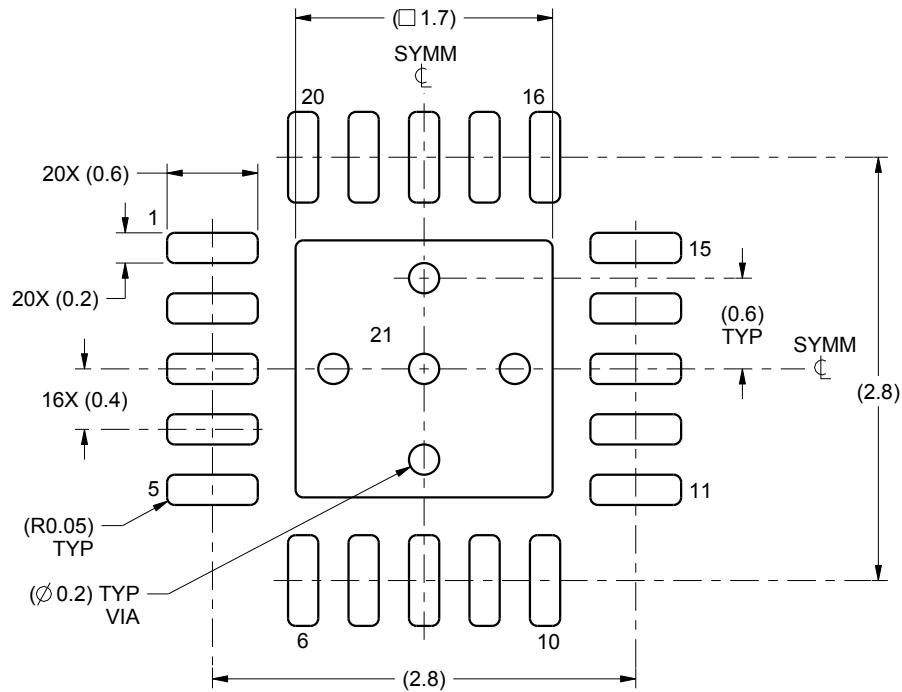
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

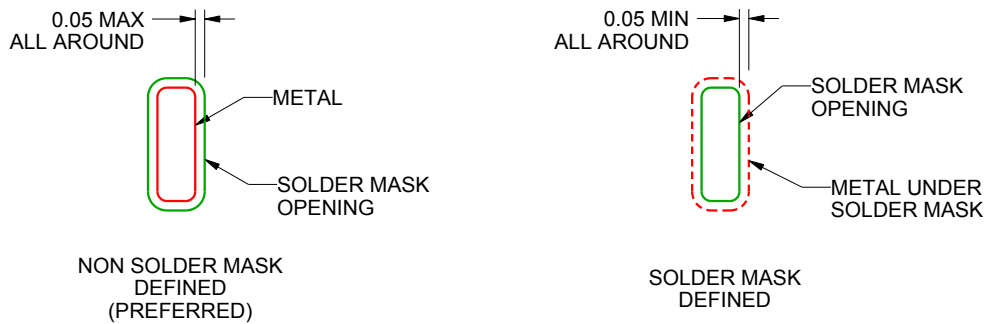
RUK0020B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4222676/A 02/2016

NOTES: (continued)

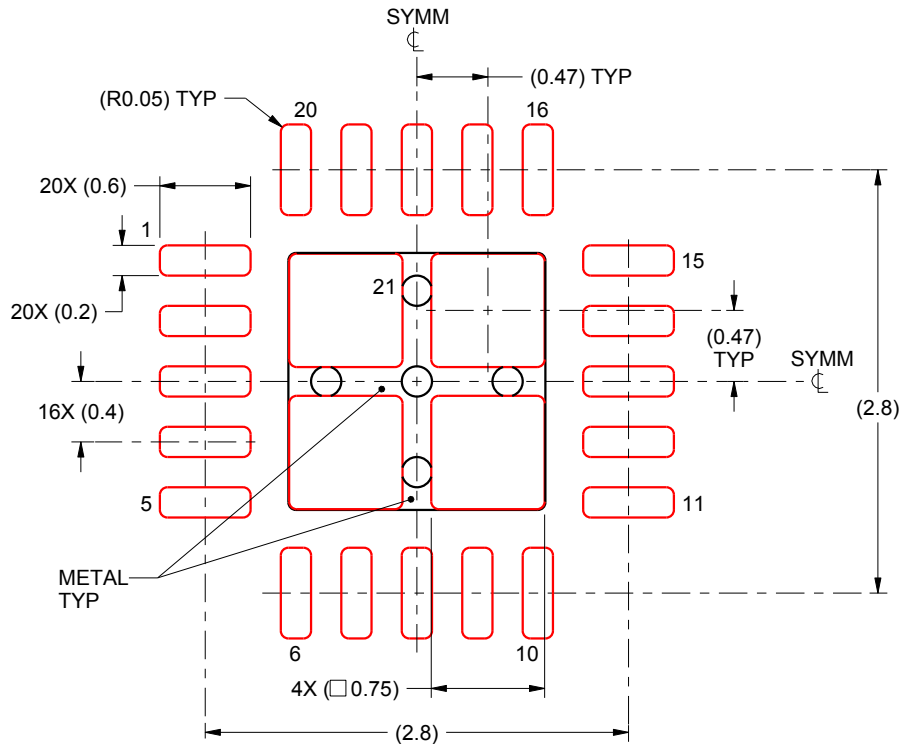
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sl原因271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RUK0020B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 21:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4222676/A 02/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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