8V – 60V_{IN}, 10V – 50V_{OUT}, 50 – 140W ZVS Buck-Boost Regulator

Product Description

The PI3740-00 is a high-efficiency, wide input and output range DC-DC ZVS Buck-Boost Regulator. This high-density System-in-Package (SiP) integrates controller, power switches, and support components. The integration of a high-performance Zero-Voltage Switching (ZVS) topology within the PI3740-00 increases point-of-load performance, providing best-in-class power efficiency.

The PI3740-00 requires an external inductor, resistive divider and minimal capacitors to form a complete DC-DC switching mode buck-boost regulator.

Device	Output Voltage	
	Set	Range
PI3740-00	12V	10 – 50V

The ZVS architecture also enables high-frequency operation while minimizing switching losses and maximizing efficiency. The high switching frequency operation reduces the size of the external filtering components, improves power density and enables fast dynamic response to line and load transients.

Features & Benefits

- Up to 96% efficiency
- 50 – 140W continuous output power
- Parallel-capable with single-wire current sharing
- External frequency synchronization / interleaving
- High-side current sense amplifier
- General-purpose amplifier
- Lighting / constant current mode (LGH)
- Input over / undervoltage lockout (OVLO / UVLO)
- Output overvoltage protection (OVP)
- Overtemperature protection (OTP)
- Fast and slow current limits
- –40 to 115°C operating range (T_J), -LGIZ
- –55 to 115°C operating range (T_J), -LGMZ
- Excellent light-load efficiency

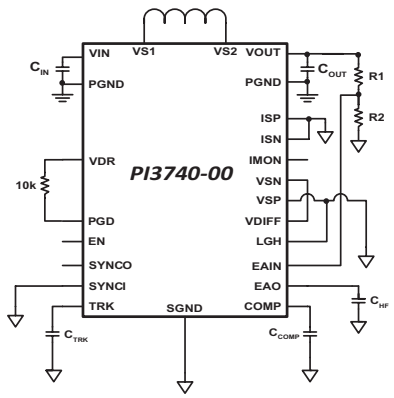
Applications

- Battery Charging and Conditioning, Telecom, Networking, Lighting
- Computing, Communications, Industrial, Automotive Accessories
- 12, 24, 48 and 60V DC–DC Applications

Package Information

- 10 x 14 x 2.56mm LGA SiP

Typical Application



Contents

Order Information

Part Number	Description	Package	Transport Media
PI3740-00-LGIZ	V_{IN} 8 – 60V, V_{OUT} 10 – 50V –40 to 115°C Temperature Range	10 x 14mm 108-pin LGA	TRAY
PI3740-00-LGMZ	V_{IN} 8 – 60V, V_{OUT} 10 – 50V –55 to 115°C Temperature Range		

Absolute Maximum Ratings

Note: Stresses beyond these limits may cause permanent damage to the device. Operation at these conditions or conditions beyond those listed in the Electrical Specifications table is not guaranteed. All voltage nodes are referenced to PGND unless otherwise noted.

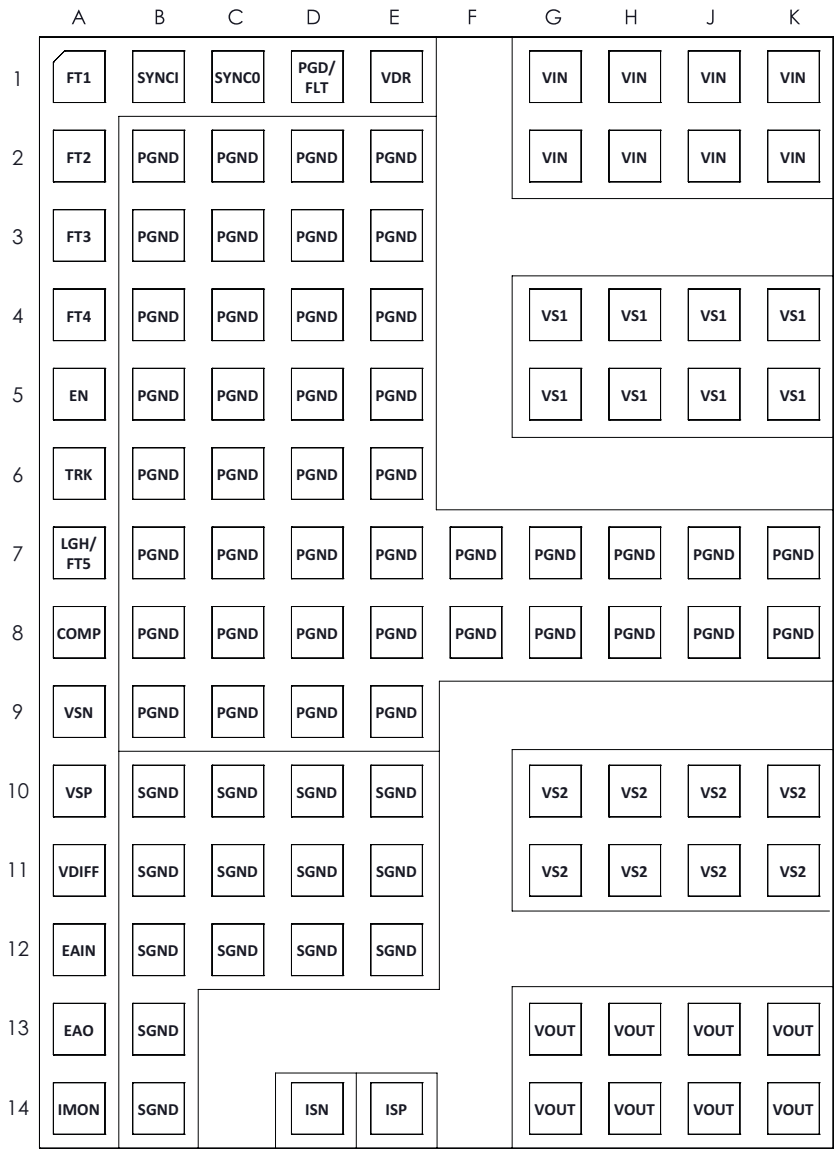
Location	Name	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
1 – 2, G – K	V_{IN}	75V	–0.7V	40A [b]	40A [b]
4 – 5, G – K	VS1	75V	$-0.7V_{DC}$ [a]	40A [b]	18A [b]
10 – 11, G – K	VS2	75V	$-0.7V_{DC}$ [a]	40A [b]	18A [b]
13 – 14, G – K	V_{OUT}	75V	$-0.7V_{DC}$	40A [b]	40A [b]
1E	VDR	5.5V	–0.3V	30mA	200mA
1D	PGD	5.5V	–0.3V	20mA	20mA
1C	SYNCO	5.5V	–0.3V	5mA	5mA
1B	SYNCI	5.5V	–0.3V	5mA	5mA
1A	FT1	5.5V	–0.3V	5mA	5mA
2A	FT2	5.5V	–0.3V	5mA	5mA
3A	FT3	5.5V	–0.3V	5mA	5mA
4A	FT4	5.5V	–0.3V	10mA	10mA
5A	EN	5.5V	–0.3V	5mA	5mA
6A	TRK	5.5V	–0.3V	50mA	50mA
7A	LGH	5.5V	–0.3V	5mA	5mA
8A	COMP	5.5V	–0.3V	5mA	5mA
9A	VSN	5.5V	–1.5V	5mA	5mA
10A	VSP	5.5V	–1.5V	5mA	5mA
11A	VDIFF	5.5V	–0.5V	5mA	5mA
12A	EAIN	5.5V	–0.3V	5mA	5mA
13A	EAO	5.5V	–0.3V	5mA	5mA
14A	IMON	5.5V	–0.3V	5mA	5mA
14D	ISN [c]	75V	$-2V_{DC}$	5mA	5mA
14E	ISP [c]	75V	$-2V_{DC}$	5mA	5mA
10 – 14, B + 10 – 12, C – E	SGND	0.3V	–0.3V	200mA	200mA
2 – 9, B – E + 7 – 8, F – K	PGND	N/A	N/A	18A [b]	18A [b]

[a] Transient VS1 voltages are guaranteed by design when the specified 420nH ±10% inductor is used.
[b] Non-Operating Test Mode Limits.
[c] The ISP pin to ISN pin has a maximum differential limit of $+5.5V_{DC}$ and $-0.5V_{DC}$.

Pin Description

Pin Number	Pin Name	Description
1–2, G–K	VIN	Input voltage and sense node for UVLO, OVLO and feed forward compensation.
4–5, G–K	VS1	Input side switching node and ZVS sense node for power switches.
10–11, G–K	VS2	Output side switching node and ZVS sense node for power switches.
13–14, G–K	VOUT	Output voltage and sense node for power switches, V_{OUT} feed forward compensation, V_{OUT_OV} and internal signals.
1E	VDR	Internal 5.1V supply for gate drivers and internal logic. May be used as reference or low power bias supply for up to 2mA. Must be impedance limited by the user.
1D	PGD	Fault & Power Good indicator. PGD pulls low when the regulator is not operating or if EAIN is less than 1.4V.
1C	SYNCO	Synchronization output. Outputs a high signal for ½ of the programmed switching period at the beginning of each switching cycle, for synchronization of other regulators.
1B	SYNCI	Synchronization input. When a falling edge synchronization pulse is detected, the PI3740-00 will delay the start of the next switching cycle until the next falling edge sync pulse arrives, up to a maximum delay of two times the programmed switching period. If the next pulse does not arrive within two times the programmed switching period, the controller will leave sync mode and start a switching cycle automatically. Connect to SGND when not in use.
1A	FT1	For factory use only. Connect to SGND or leave floating in application.
2A	FT2	For factory use only. Connect to SGND or leave floating in application.
3A	FT3	For factory use only. Connect to SGND in application.
4A	FT4	For factory use only. Connect to SGND in application.
5A	EN	Regulator Enable control. Asserted high or left floating – regulator enabled; Asserted low, regulator output disabled.
6A	TRK	Soft-start and track input. An external capacitor must be connected between TRK pin and SGND to decrease the rate of output rise during soft start. Recommended value is 47nF for 1.6ms rise.
7A	LGH	Input for constant current lighting amplifier. Connect to SGND if not in use.
8A	COMP	Error amp compensation dominant pole. Connect a capacitor of 4700pF by default between COMP and SGND to set the control loop dominant pole.
9A	VSN	General purpose amplifier inverting input.
10A	VSP	General purpose amplifier non-inverting input.
11A	VDIFF	General Purpose amplifier output. When unused connect VDIFF to VSN and VSP to SGND.
12A	EAIN	Error amplifier inverting input and sense for PGD. Connect by resistive divider to the output.
13A	EAO	Error amp output: External connection for additional compensation and current sharing. Add 56pF capacitor from EAO to SGND.
14A	IMON	High side current sense amplifier output.
14D	ISN	High side current sense amplifier negative input.
14E	ISP	High side current sense amplifier positive input.
10 – 14, B + 10 – 12, C – E	SGND	Signal ground. Internal logic and analog ground for the regulator. SGND and PGND are star connected within the regulator package.
2 – 9, B – E + 7 – 8, F – K	PGND	Power ground. V_{IN}, V_{OUT}, VS1 and VS2 power returns. SGND and PGND are star connected within the regulator package.

Package Pin-Out



BB 10x14mm SiP

TOP VIEW THROUGH THE PRODUCT

Large Pin Blocks

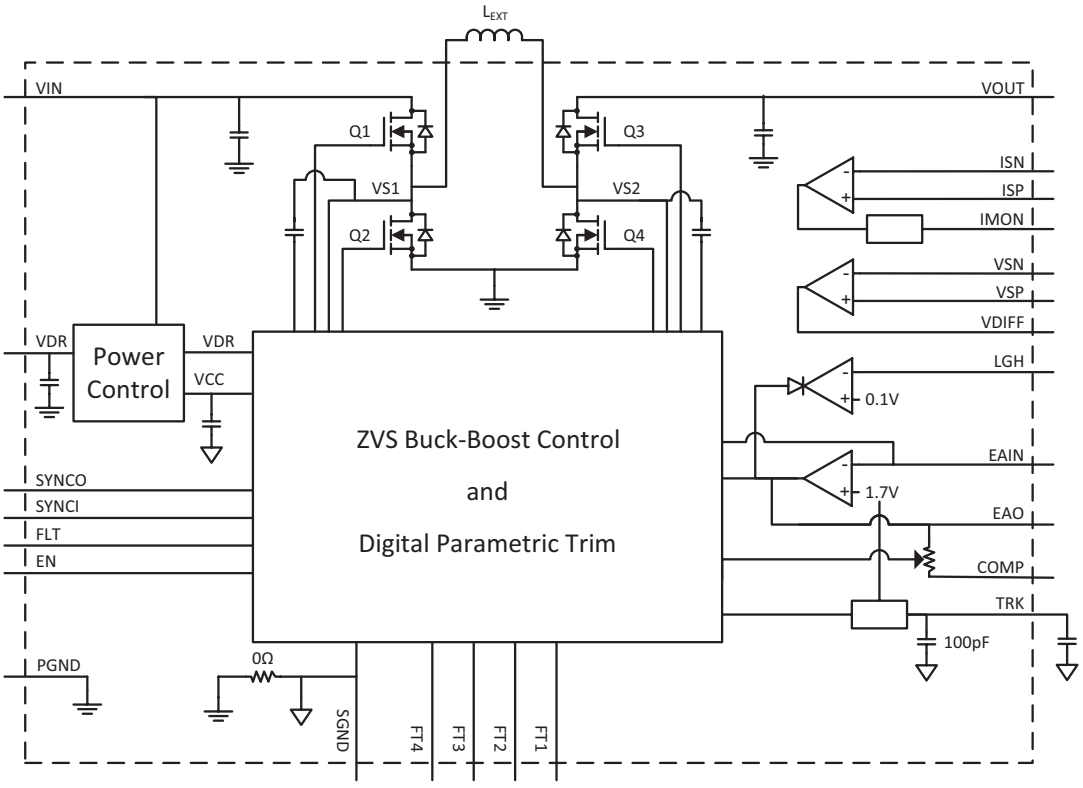
Pin Block Name	Group of pins
VIN	G1 – 2, H1 – 2, J1 – 2, K1 – 2
VS1	G4 – 5, H4 – 5, J4 – 5, K4 – 5
PGND	B2 – 9, C2 – 9, D2 – 9, E2 – 9, F7 – 8, G7 – 8, H7 – 8, J7 – 8, K7 – 8
VS2	G10 – 11, H10 – 11, J10 – 11, K10 – 11
VOUT	G13 – 14, H13 – 14, J13 – 14, K13 – 14
SGND	B10 – 14, C10 – 12, D10 – 12, E10 – 12

Storage and Handling Information

Storage Temperature		–65 to 150°C
Internal Operating Temperature	-LGIZ	–40 to 115°C
	-LGMZ	–55 to 115°C
Soldering Temperature for 20 seconds		245°C
MSL Rating		3
ESD Rating [d]		2.0kV HBM; 1.0kV CDM

[d] JS-200-2014, JESD22-A114F.

Block Diagram



PI3740-00 Electrical Characteristics

Specifications apply for the conditions –40°C < T_J < 115°C for -LGIZ, –55°C < T_J < 115°C for -LGMZ,
V_{IN} = 24V, V_{OUT} = 12V, L_{EXT} = 420nH [e], external C_{IN} = 6 x 2.2µF, external C_{OUT} = 8 x 10µF, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Specifications						
Input Voltage	V_{IN_DC}		8	24	60	V
Input Current During Output Short (Fault Condition Duty Cycle)	I_{IN_SHORT}	[f]		3.75		mA
Input Quiescent Current	I_{Q_VIN}	Enabled (no load)		5		mA
Input Quiescent Current	I_{Q_VIN}	Disabled		2		mA
Input Voltage Slew Rate	V_{IN_SR}	[f]			1	V / µs
Internal Input Capacitance	C_{IN}	25°C, V_{IN} = 48V		0.5		µF
V_{IN} UVLO Threshold Rising	$V_{IN\_UVLO\_START}$		6.4	6.9	7.2	V
V_{IN} UVLO Hysteresis	$V_{IN\_UVLO\_HYS}$			0.5		V
V_{IN} OVLO Threshold Rising	$V_{IN\_OVLO\_START}$		61.0	64.5	68.2	V
V_{IN} OVLO Hysteresis	$V_{IN\_OVLO\_HYS}$			2.66		V
Output Specifications						
EAIN Voltage Total Regulation	V_{EAIN_DC}		1.667	1.7	1.734	V
Output Voltage Range	V_{OUT_DC}		10	12	50	V
Output Current Range	I_{OUT_DCR}	[g]	0		[g]	A
Output Current Steady State	I_{OUT_DC}	V_{IN} = 8 – 16V, V_{OUT} ≤ 12V, T_{CASE} = 25°C [g]	5.0			A
		V_{IN} = 16 – 24V, V_{OUT} ≤ 12V, T_{CASE} = 25°C [g]	6.5			
Output Power Steady State	P_{OUT_DC}	V_{IN} = 8 – 60V, V_{OUT} = 12 – 36V, T_{CASE} = 25°C [g]	60			W
		V_{IN} = 16 – 28V, V_{OUT} = 24 – 36V, T_{CASE} = 25°C [g]	123			
Maximum Array Size	$N_{PARALLEL}$				3	Modules
Output Current, Array of 2	$I_{OUT\_DC\text{-}ARRAY2}$	Total array capability, see applications section for details	0		1.77 • I_{OUT_DC}	A
Output Current, Array of 3	$I_{OUT\_DC\text{-}ARRAY3}$	Total array capability, see applications section for details	0		2.54 • I_{OUT_DC}	
Line Regulation	ΔV_{OUT} (ΔV_{IN})	at 25°C, 8V < V_{IN} < 60V		0.10		%
Load Regulation	ΔV_{OUT} (ΔI_{OUT})	at 25°C, I_{OUT} above 5% of the typical full load		0.10		%
Output Ripple	V_{OUT_AC}	I_{OUT} = 7.0A, V_{IN} = 24V, V_{OUT} = 12V, T_{CASE} = 25°C C_{OUT_EX} = 8 x 10µF, 50V, X7R, 20MHz BW		96		mV_{P-P}
Internal Output Capacitance	C_{OUT}	25°C, V_{OUT} = 24V		0.75		µF
V_{OUT} Overvoltage Threshold	V_{OUT_OVT}	Rising V_{OUT} threshold to detect open loop	50.8	53.4	56	V
V_{OUT} Overvoltage Hysteresis	V_{OUT_OVH}			1.0		V
VDR						
VDR Supply Voltage	VDR	Generated internally	4.9	5.1	5.36	V
External Loading	I_{VDR}	See Application Description for details	0		2	mA

[e] See Inductor Pairing section.
[f] Assured to meet performance specification by design, test correlation, characterization, and/or statistical process control.
[g] Output current capability varies with input & output voltage. See rated ouput current / power curves on page 11.

PI3740-00 Electrical Characteristics (Cont.)

Specifications apply for the conditions –40°C < T_J < 115°C for -LGIZ, –55°C < T_J < 115°C for -LGMZ,
V_{IN} = 24V, V_{OUT} = 12V, L_{EXT} = 420nH [e], external C_{IN} = 6 x 2.2µF, external C_{OUT} = 8 x 10µF, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Current Sense Amplifier (Dedicated to monitor Input or Output Current)						
ISP Pin Bias Current (Sink)		V_{OUT} = 10V, Flows to SGND	90	150	260	µA
ISN Pin Bias Current		V_{OUT} = 10V		0		µA
Common Mode Input Range			8		60	V
IMON Source Current			1	1.8	3	mA
IMON Sink Current			1	1.6	2.6	mA
IMON Output at No Load				10		mV
Full Scale Error		40mV input	–4		4	%
Bandwidth		[f]		40		kHz
Settling Time for Full Scale Step		1%		20		µs
Gain	A_{V_CS}	15mV measured across 5mΩ shunt		20		V / V
General Purpose Amplifier						
Open Loop Gain		[e]	96	120	140	dB
Small Signal Gain-Bandwidth		[e]	5	7	12	MHz
Offset			–1		1	mV
Common Mode Input Range			–0.1		2.5	V
Differential Mode Input Range					2	V
Maximum Output Voltage		IDIFF = –1mA			VDR – 0.2V	V
Minimum Output Voltage		No Load			20	mV
Capacitive Load for Stable Operation		[f]	0		100	pF
Slew Rate				10		V / µs
Output Current			–1		1	mA
Current Amplifier (LGH)						
Reference			95	100	105	mV
Input Offset				0.5		mV
Gain-Bandwidth Product			3			MHz
Internal Feedback Capacitance				20		pF

[e] See Inductor Pairing section.
[f] Assured to meet performance specification by design, test correlation, characterization, and/or statistical process control.
[g] Output current capability varies with input & output voltage. See rated ouput current / power curves on page 11.

PI3740-00 Electrical Characteristics (Cont.)

Specifications apply for the conditions –40°C < T_J < 115°C for -LGIZ, –55°C < T_J < 115°C for -LGMZ,
V_{IN} = 24V, V_{OUT} = 12V, L_{EXT} = 420nH [e], external C_{IN} = 6 x 2.2µF, external C_{OUT} = 8 x 10µF, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Transconductance Error Amplifier						
Reference	V_{REF}	EAIN = EAO, 25°C	1.688	1.7	1.712	V
		EAIN = EAO	1.667	1.7	1.734	
Input Range	V_{EAIN}	Note V_{EAIN_OV} below	0		VDR	V
Maximum Output Voltage			3.35	3.6	4.0	V
Minimum Output Voltage				0.05	0.15	V
Transconductance		Factory Set		7.6		mS
Zero Resistor		Factory Set		5		kΩ
EAO Output Current Sourcing		V_{EAO} = 50mV, V_{EAIN} = 0V		400		µA
EAO Output Current Sinking		V_{EAO} = 2V, V_{EAIN} = 5V		400		µA
Open Loop Gain		R_{OUT} > 1MΩ [f]	70	80		dB
Input Capacitance				56		pF
Output Capacitance				1		pF
Control and Protection						
Switching Frequency	F_{SW}			1		MHz
V_{EAO} Pulse Skip Threshold	V_{EAO_PST}	V_{EAO} to SGND		0.4		V
Control Node Range	V_{RAMP}		0		3.3	V
V_{EAO} Overload Threshold	V_{EAO_OL}	V_{EAO} to SGND	3.175	3.3	3.425	V
Overload Timeout	T_{OL}	V_{EAO} > V_{EAO_OL}		1		ms
Overload Due to EAO limit	I_{OUT_EAOLIM}	Module shuts down after 1ms of overload and restarts after 30ms		7.7		A
V_{EAIN} Output Overvoltage Threshold	V_{EAIN_OV}	V_{EAIN} > V_{EAIN_OV}	1.94	2.04	2.14	V
Overtemperature Fault Threshold	T_{OTP}	[f]		125		°C
Overtemperature Restart Hysteresis	T_{OPT_HYS}	[f]		30		°C
V_{OUT} Negative Fault Threshold			–0.45	–0.25	–0.15	V
Soft Start and Tracking Function						
TRK Active Range		Nominal	0		1.7	V
TRK Disable Threshold			20	45	70	mV
TRK Internal Capacitance				56		pF
Soft Start Charge Current			30	50	70	µA
Soft Start Discharge Current		V_{TRK} = 0.5V		9		mA
Soft Start Time	t_{SS}	Ext C_{SS} = 47nF		1.6		ms

[e] See Inductor Pairing section.
[f] Assured to meet performance specification by design, test correlation, characterization, and/or statistical process control.
[g] Output current capability varies with input & output voltage. See rated ouput current / power curves on page 11.

PI3740-00 Electrical Characteristics (Cont.)

Specifications apply for the conditions –40°C < T_J < 115°C for -LGIZ, –55°C < T_J < 115°C for -LGMZ,
V_{IN} = 24V, V_{OUT} = 12V, L_{EXT} = 420nH[e], external C_{IN} = 6 x 2.2µF, external C_{OUT} = 8 x 10µF, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Enable						
Enable High Threshold	EN_{IH}		0.9	1	1.1	V
Enable Low Threshold	EN_{IL}		0.7	0.8	0.9	V
Enable Threshold Hysteresis	EN_{HYS}		100	200	300	mV
Enable Pin Bias Current		V_{EN} = 0V or V_{EN} = 2V		±50		µA
Enable Pull-Up Voltage		Floating		2.0		V
Fault Restart Delay Time	t_{FR_DLY}			30		ms
Digital Signals						
SYNCI High Threshold		VDR = 5.1V		1/2 VDR		V
SYNCO High	$SYNCO_{OH}$		VDR – 0.5		VDR	V
SYNCO Low	$SYNCO_{OL}$	$I_{SYNCOUT}$ = 1mA			0.5	V
PGD High Leakage	PGD_{ILH}	V_{PGD} = VDR			10	µA
PGD Output Low	PGD_{OL}	I_{PGD} = 4mA			0.4	V
PGD EAIN Low Rise			1.41	1.45	1.48	V
PGD EAIN Low Fall			1.36	1.41	1.46	V
PGD EAIN Threshold Hysteresis				35		mV
PGD EAIN High			1.94	2.04	2.14	V

[e] See Inductor Pairing section.
[f] Assured to meet performance specification by design, test correlation, characterization, and/or statistical process control.
[g] Output current capability varies with input & output voltage. See rated ouput current / power curves on page 11.

PI3740-00 Performance Characteristics T_{PCB} = 25°C [h]

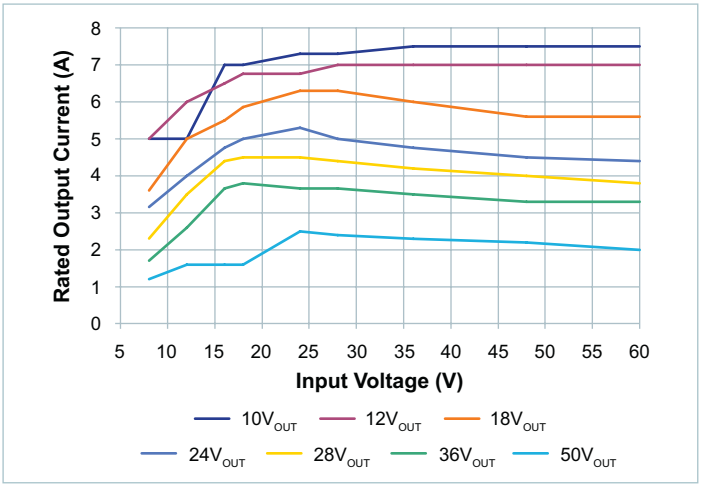


Figure 1 — *Output current of PI3740-00*

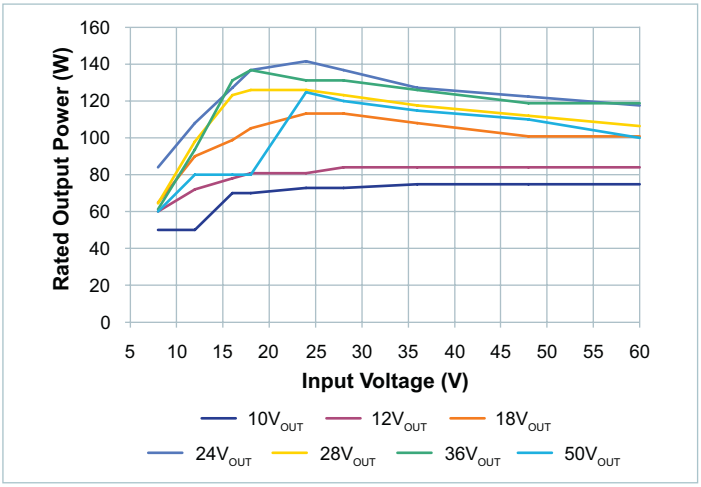


Figure 2 — *Output power of PI3740-00*

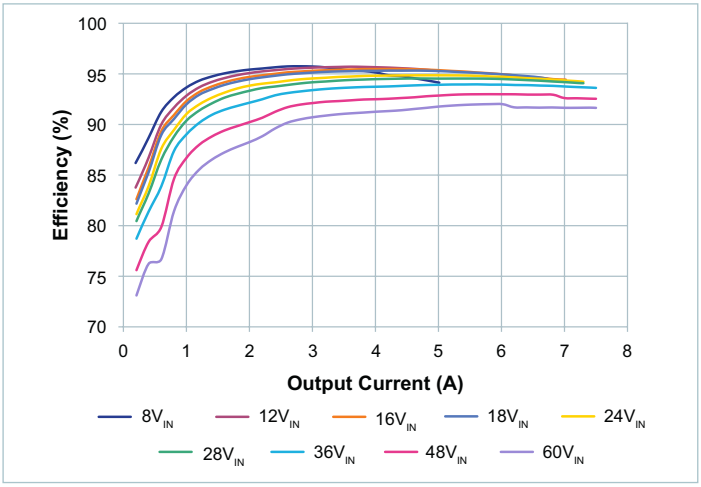


Figure 3 — *$10V_{OUT}$ efficiency*

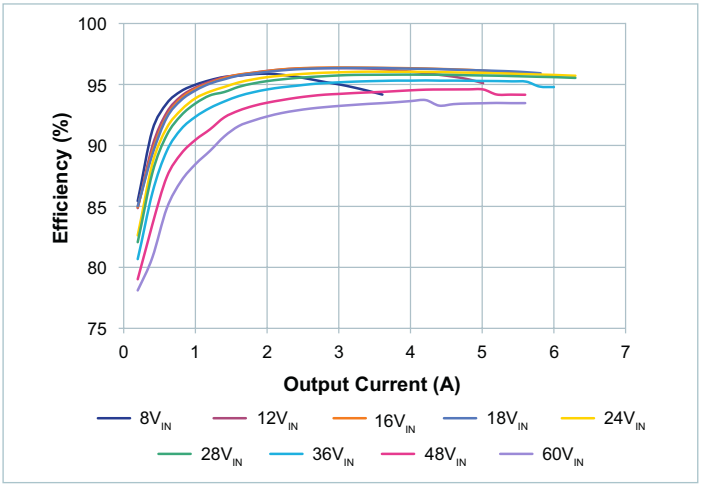


Figure 5 — *$18V_{OUT}$ efficiency*

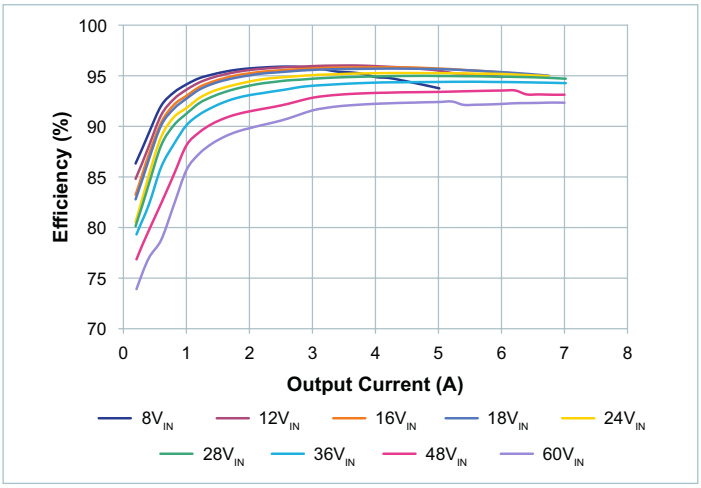


Figure 4 — *$12V_{OUT}$ efficiency*

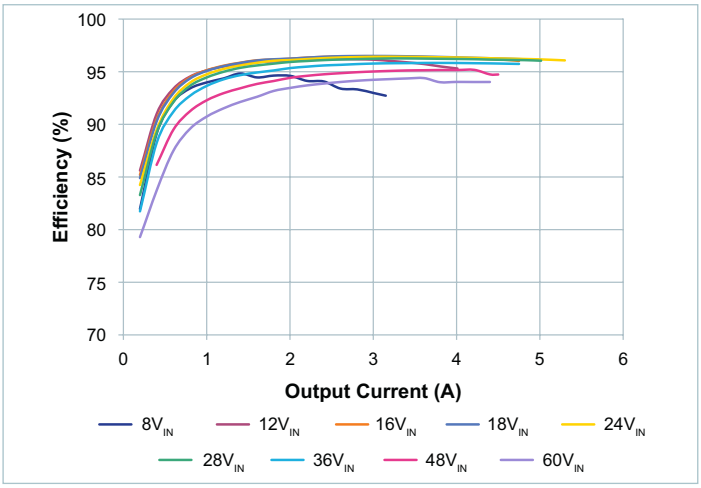


Figure 6 — *$24V_{OUT}$ efficiency*

[h] Note: Testing was performed using a 3 x 3in, four 2oz copper layers, FR4 evaluation board platform.

PI3740-00 Performance Characteristics T_{PCB} = 25°C (Cont.) [h]

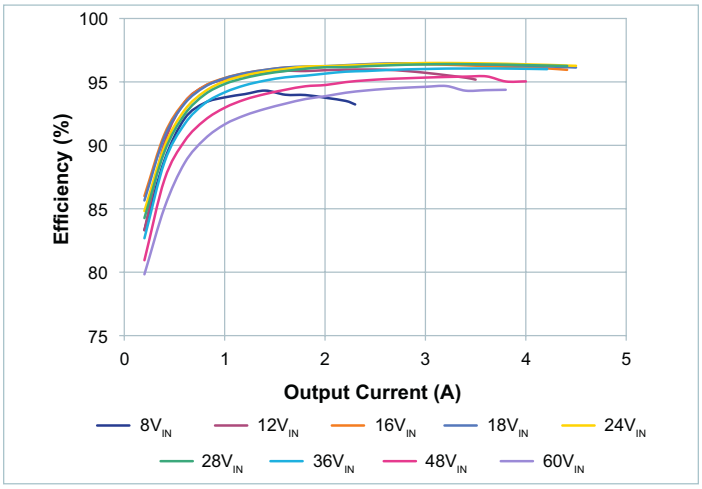


Figure 7 — *28V_{OUT} efficiency*

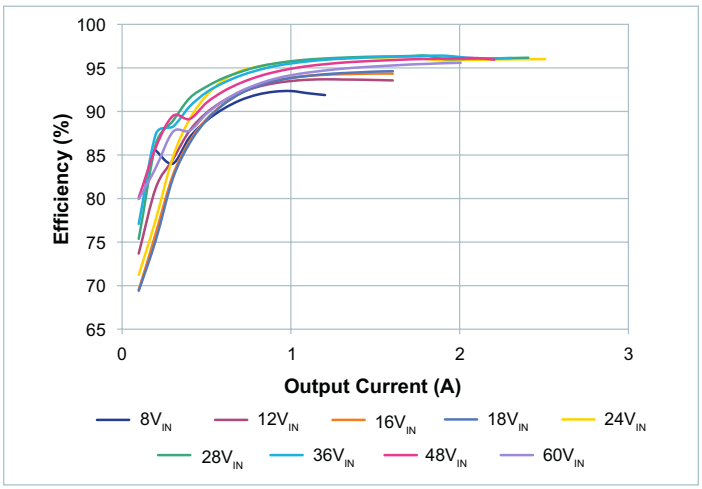


Figure 9 — *50V_{OUT} efficiency*

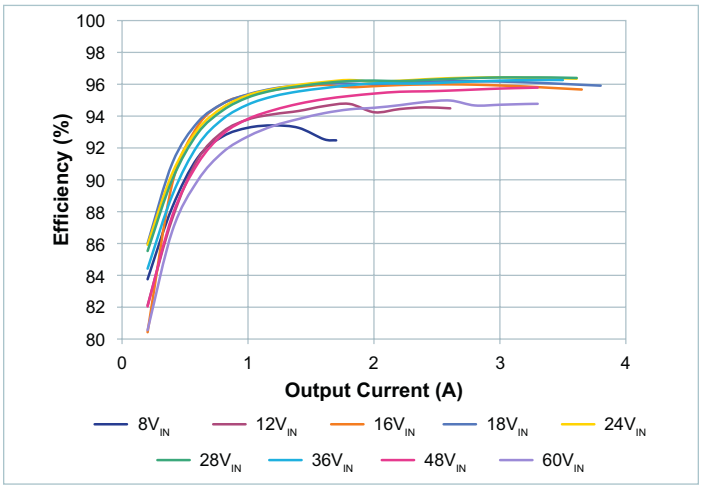


Figure 8 — *36V_{OUT} efficiency*

[h] Note: Testing was performed using a 3 x 3in, four 2oz copper layers, FR4 evaluation board platform.

PI3740-00 Performance Characteristics T_{PCB} = 25°C (Cont.) [h]

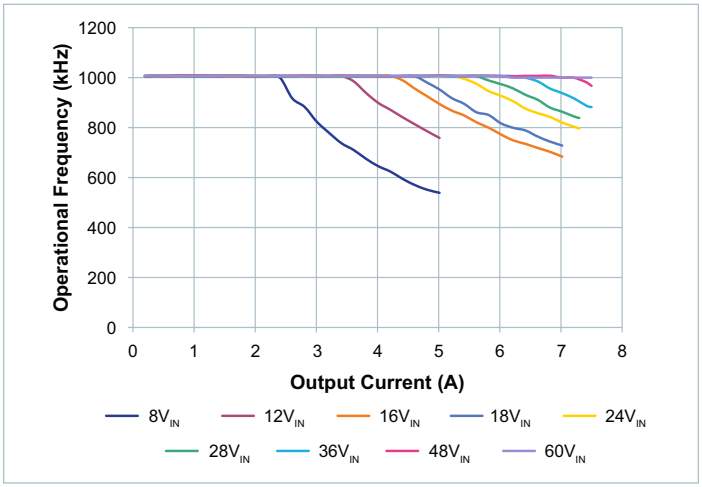


Figure 10 — *Switching frequency vs. output current at $10V_{OUT}$*

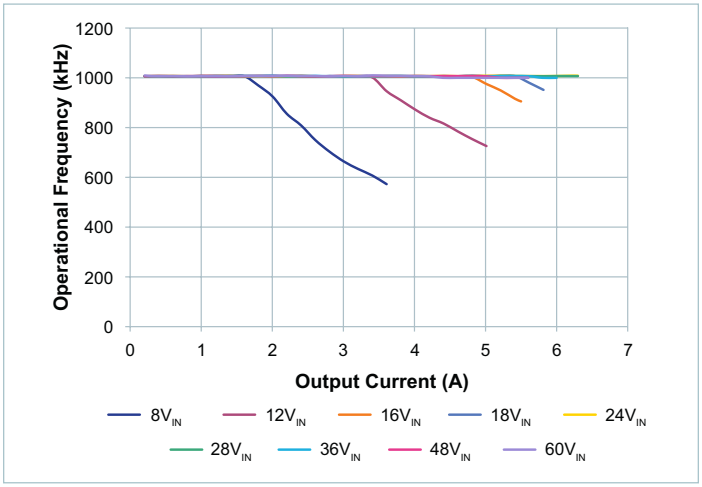


Figure 12 — *Switching frequency vs. output current at $18V_{OUT}$*

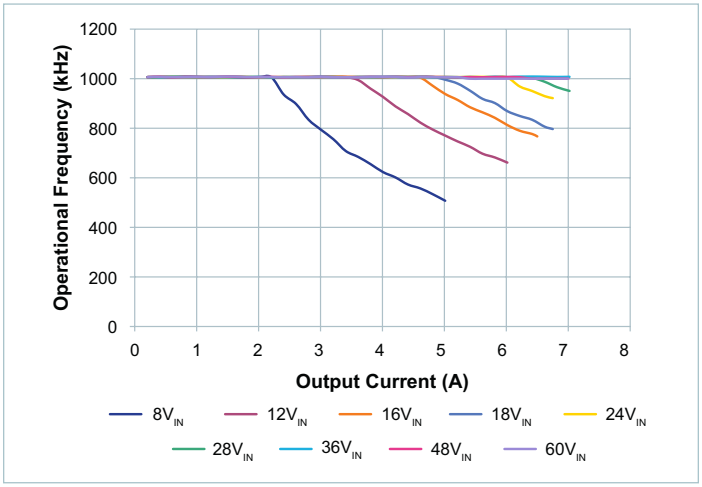


Figure 11 — *Switching frequency vs. output current at $12V_{OUT}$*

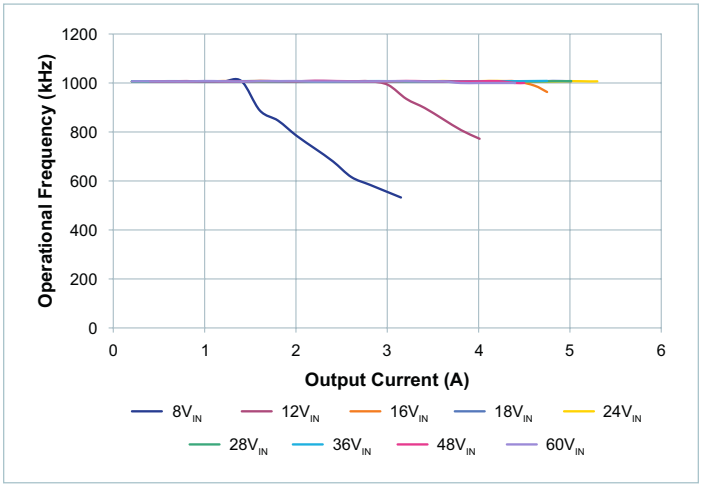


Figure 13 — *Switching frequency vs. output current at $24V_{OUT}$*

[h] Note: Testing was performed using a 3 x 3in, four 2oz copper layers, FR4 evaluation board platform.

PI3740-00 Performance Characteristics T_{PCB} = 25°C (Cont.) [h]

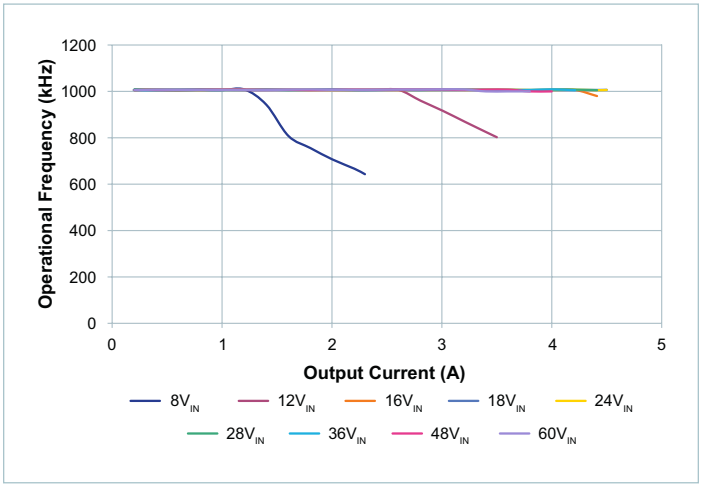


Figure 14 — *Switching frequency vs. output current at $28V_{OUT}$*

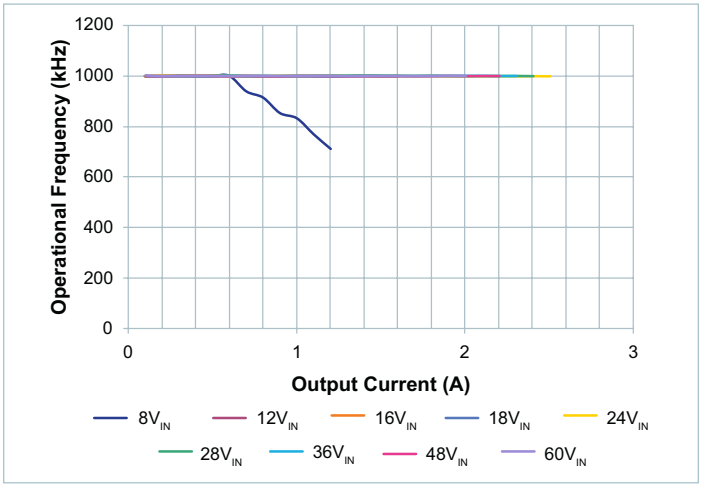


Figure 16 — *Switching frequency vs. output current at $50V_{OUT}$*

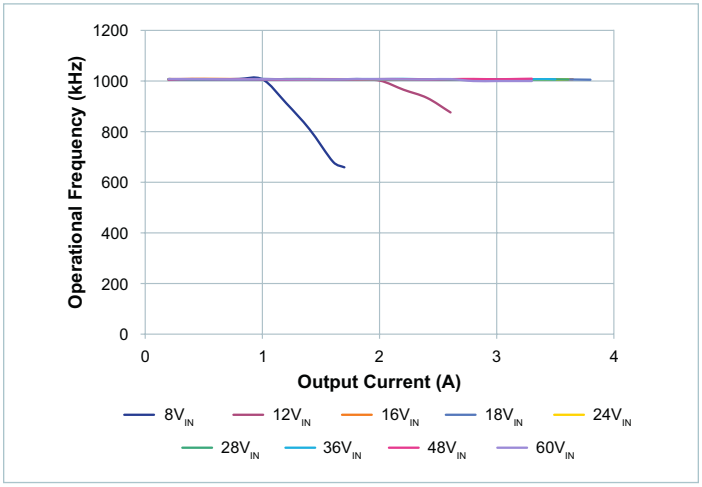


Figure 15 — *Switching frequency vs. output current at $36V_{OUT}$*

[h] Note: Testing was performed using a 3 x 3in, four 2oz copper layers, FR4 evaluation board platform.

PI3740-00 Performance Characteristics T_{PCB} = 25°C (Cont.)

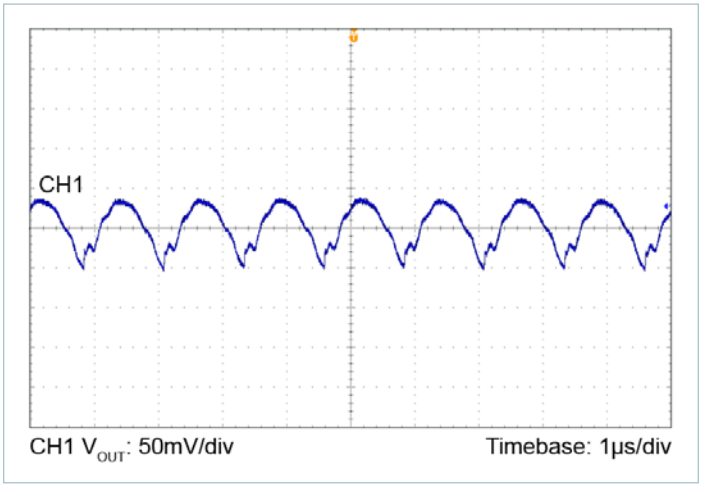


Figure 17 — *Output voltage ripple at $24V_{IN}$ to $10V_{OUT}$, 7.3A; C_{OUT} = 8 x 10µF ceramic*

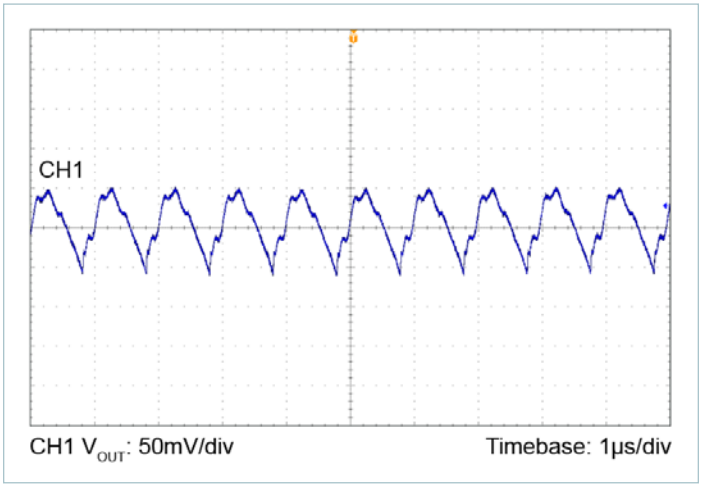


Figure 19 — *Output voltage ripple at $24V_{IN}$ to $18V_{OUT}$, 6.3A; C_{OUT} = 8 x 10µF ceramic*

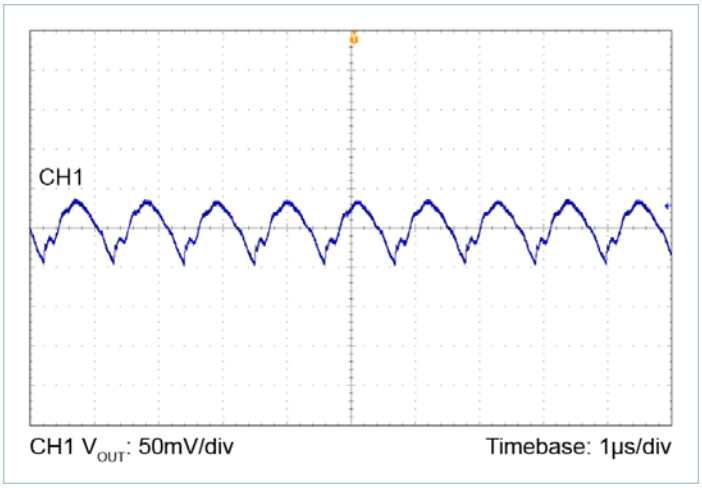


Figure 18 — *Output voltage ripple at $24V_{IN}$ to $12V_{OUT}$, 6.75A; C_{OUT} = 8 x 10µF ceramic*

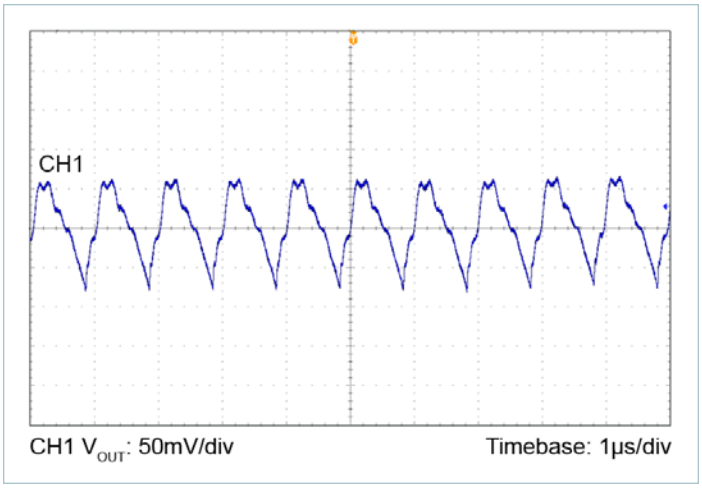


Figure 20 — *Output voltage ripple at $24V_{IN}$ to $24V_{OUT}$, 5.3A; C_{OUT} = 8 x 10µF ceramic*

PI3740-00 Performance Characteristics T_{PCB} = 25°C (Cont.)

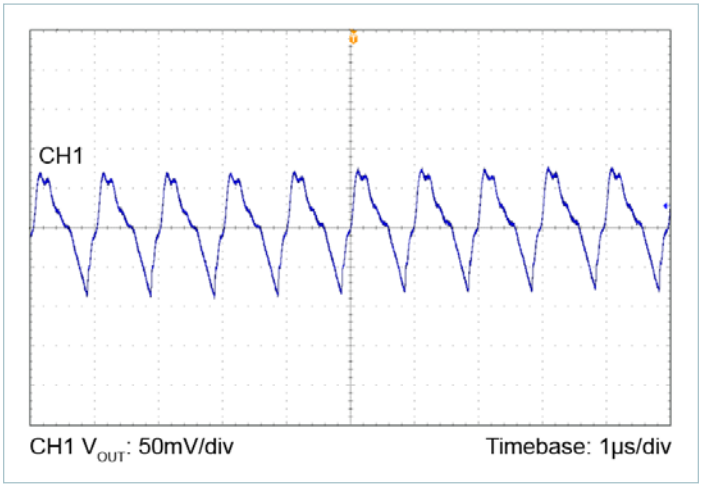


Figure 21 — *Output voltage ripple at $24V_{IN}$ to $28V_{OUT}$, 4.5A; C_{OUT} = 8 x 10µF ceramic*

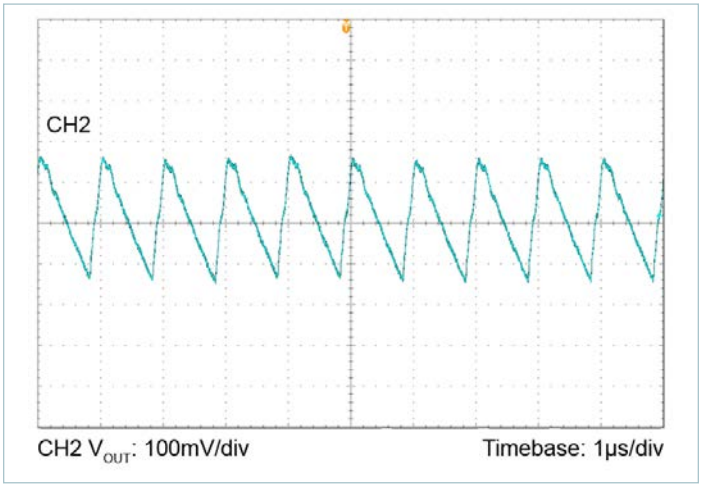


Figure 23 — *Output voltage ripple at $24V_{IN}$ to $50V_{OUT}$, 2.50A; C_{OUT} = 8 x 2.2µF ceramic*

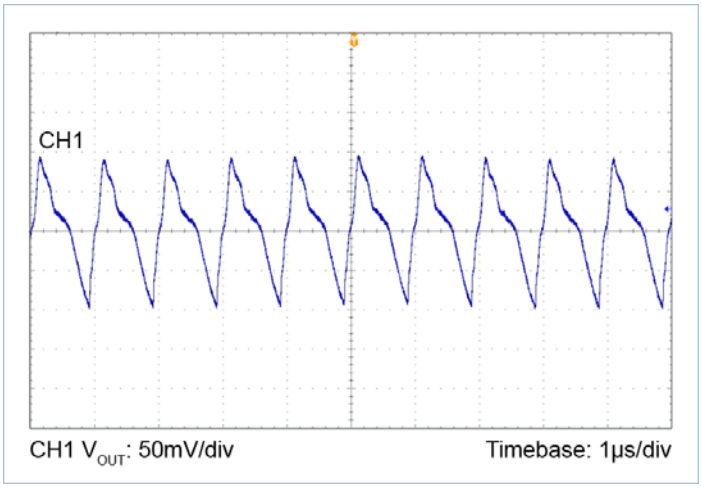


Figure 22 — *Output voltage ripple at $24V_{IN}$ to $36V_{OUT}$, 3.65A; C_{OUT} = 8 x 10µF ceramic*

PI3740-00 Performance Characteristics T_{PCB} = 25°C (Cont.)

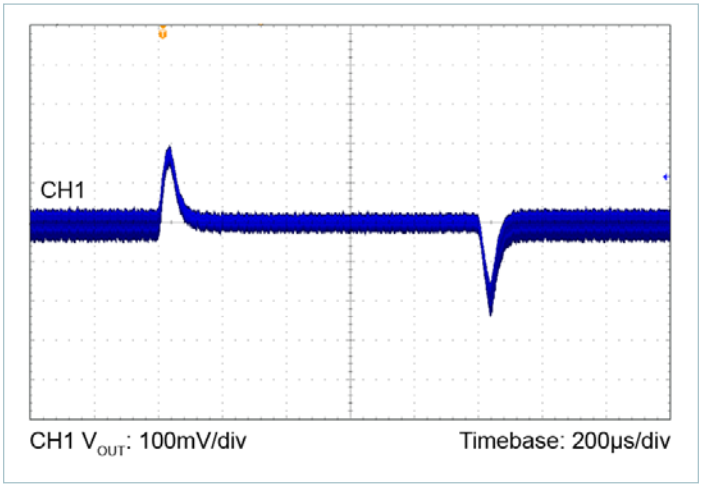


Figure 24 — *$24V_{IN}$ to $10V_{OUT}$, C_{OUT} = 8 x 10µF ceramic 3.5 – 7.0A load step, 0.1A/µs*

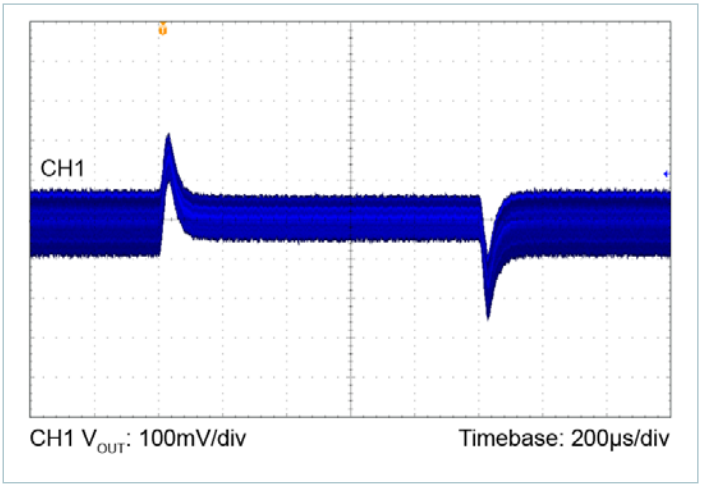


Figure 27 — *$24V_{IN}$ to $28V_{OUT}$, C_{OUT} = 8 x 10µF ceramic 2.25 – 4.5A load step, 0.1A/µs*

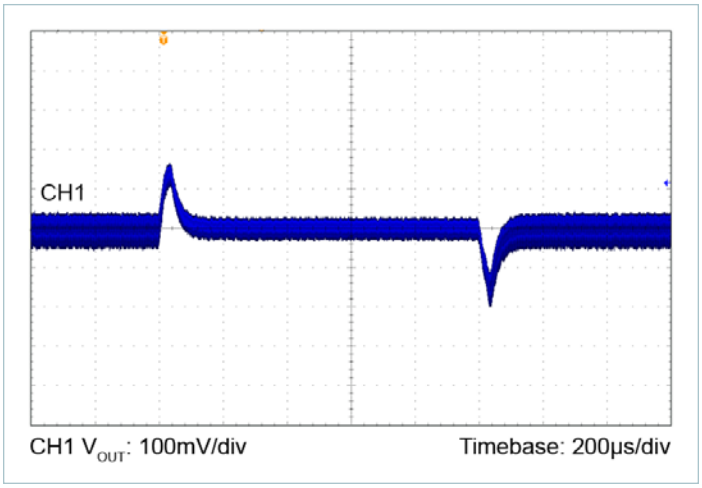


Figure 25 — *$24V_{IN}$ to $12V_{OUT}$, C_{OUT} = 8 x 10µF ceramic 3.38 – 6.75A load step, 0.1A/µs*

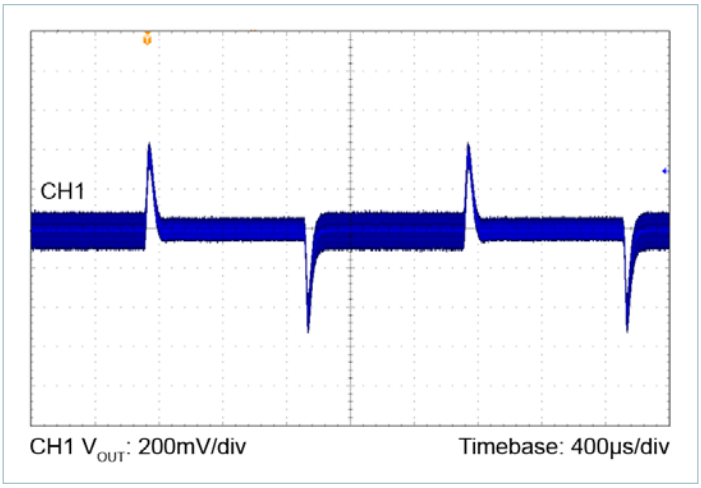


Figure 28 — *$24V_{IN}$ to $36V_{OUT}$, C_{OUT} = 8 x 10µF ceramic 1.5– 3.0A load step, 0.1A/µs*

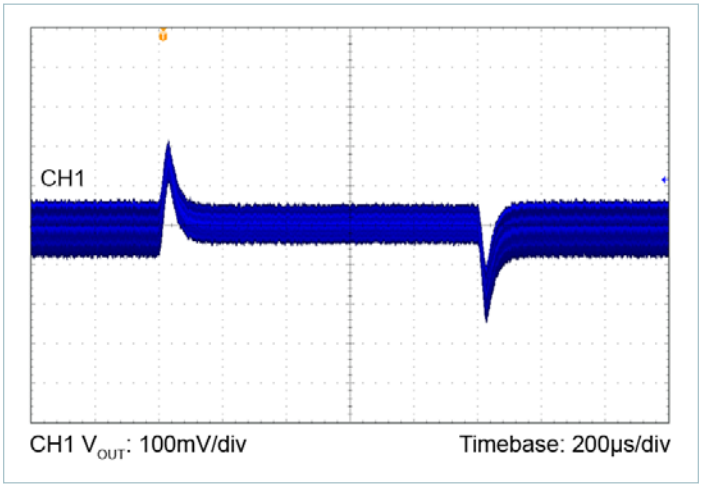


Figure 26 — *$24V_{IN}$ to $24V_{OUT}$, C_{OUT} = 8 x 10µF ceramic 2.5 – 5.0A load step, 0.1A/µs*

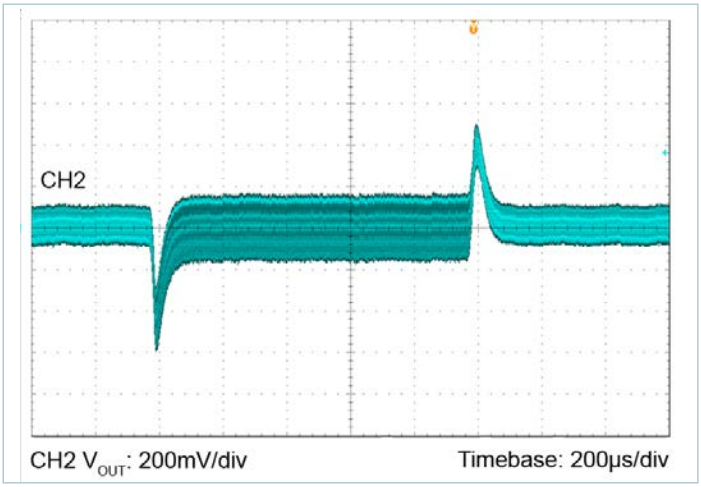


Figure 29 — *$24V_{IN}$ to $50V_{OUT}$, C_{OUT} = 8 x 2.2µF ceramic 2.5 – 1.25A load step, 0.1A/µs*

PI3740-00 Performance Characteristics T_{PCB} = 25°C (Cont.)

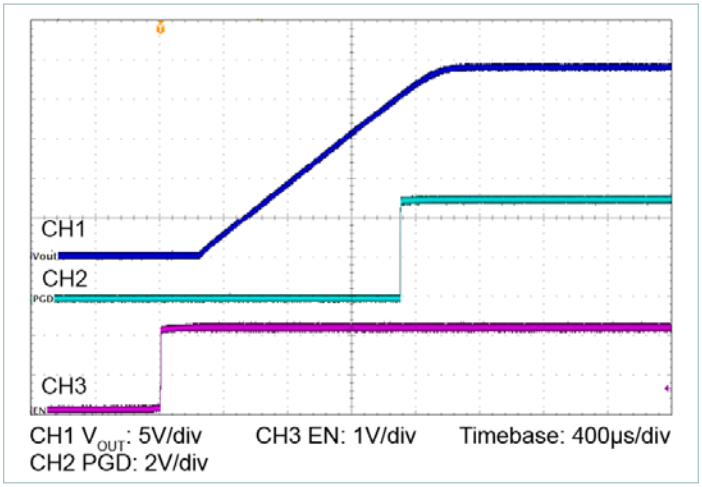


Figure 30 — *Start up with $8V_{IN}$ to $24V_{OUT}$ at 2.4A, Ext C_{SS} = 47nF*

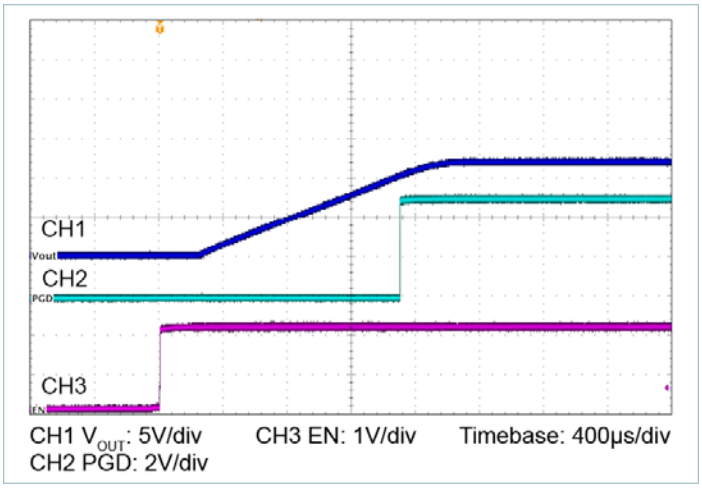


Figure 31 — *Start up with $8V_{IN}$ to $12V_{OUT}$ at 5A, Ext C_{SS} = 47nF*

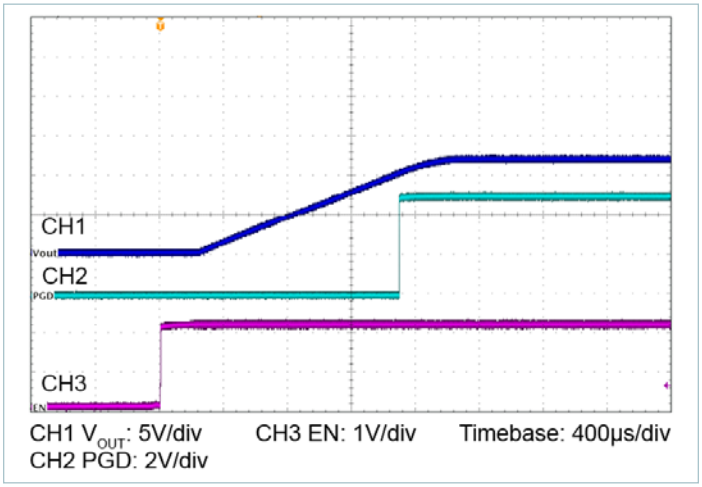


Figure 32 — *Start up with $24V_{IN}$ to $12V_{OUT}$ at 6A, Ext C_{SS} = 47nF*

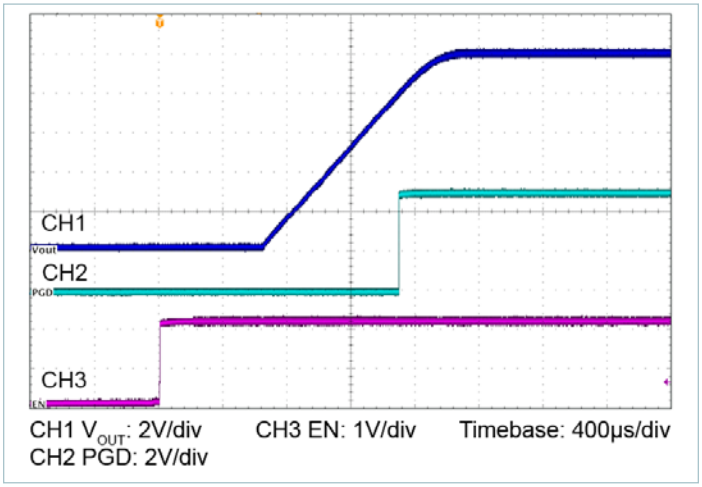


Figure 33 — *Start up with $24V_{IN}$ to $10V_{OUT}$ at 6.5A, Ext C_{SS} = 47nF*

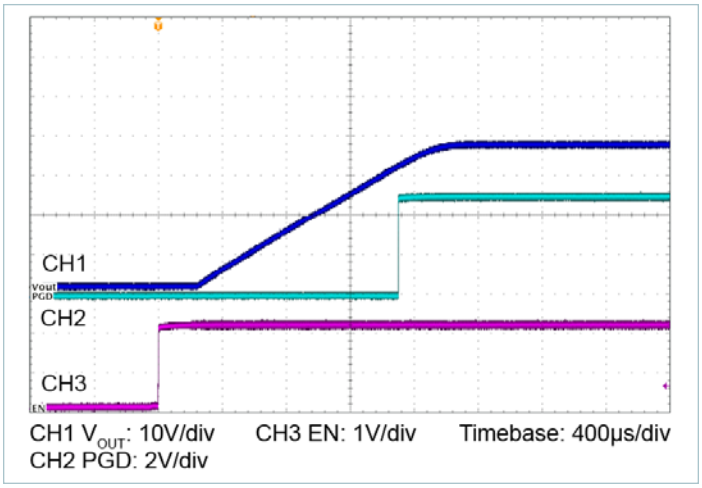


Figure 34 — *Start up with $8V_{IN}$ to $36V_{OUT}$ at 1.7A, Ext C_{SS} = 47nF*

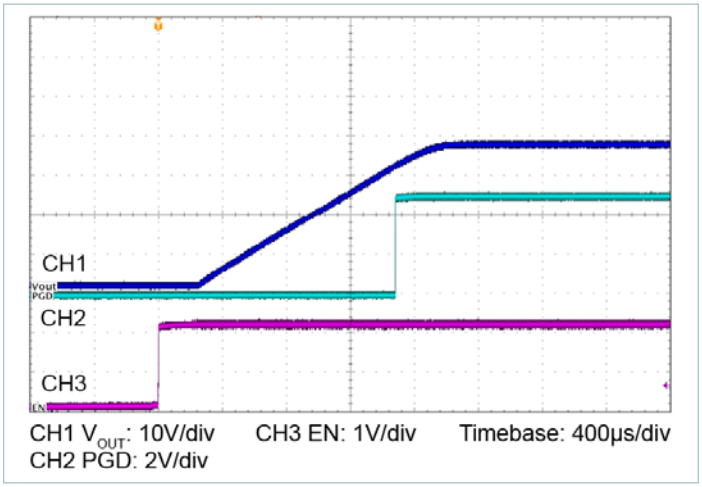


Figure 35 — *Start up with $24V_{IN}$ to $36V_{OUT}$ at 2A, Ext C_{SS} = 47nF*

MTBF

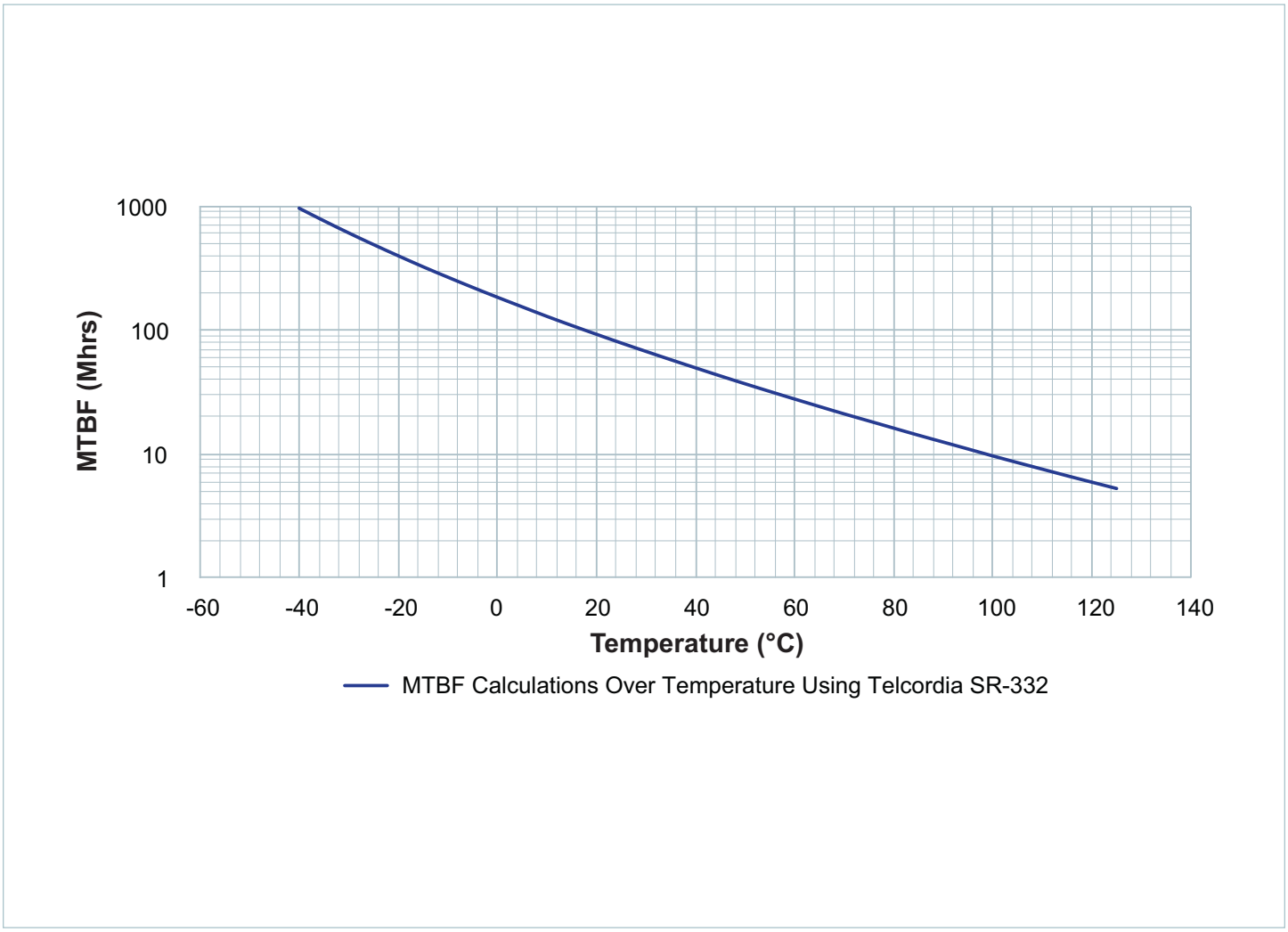


Figure 36 — *PI3740-00 calculated MTBF Telcordia SR-332 GB*

Functional Description

The PI3740-00 is a highly integrated ZVS Buck-Boost regulator. The PI3740-00 has an adjustable output voltage that is set with a resistive divider. Performance and maximum output current are characterized with a specific external power inductor as defined in the electrical specifications, and in the inductor pairing section.

For basic operation, Figure 37 shows the minimum connections and components required.

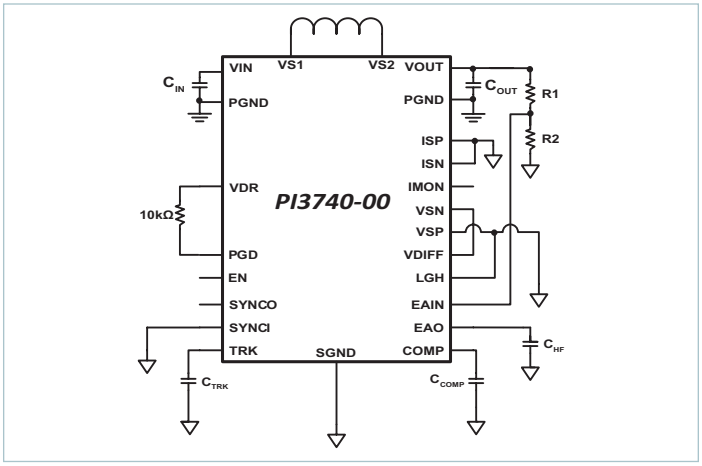


Figure 37 — *PI3740-00 with required components*

Enable

The EN pin of the regulator is referenced to SGND and permits the user to turn the regulator on or off. The EN polarity is a positive logic assertion. If the EN pin is left floating or asserted high, the regulator output is enabled. Pulling the EN pin below $0.8V_{DC}$ with respect to SGND will discharge the TRK pin until the output reaches zero or the EN pin is released. When the converter is disabled via the EN pin or due to a fault mode, the internal gate driver high side charge pumps are enabled as long as there is enough input voltage for the internal VDR supply voltage to be available. The return path for this charge pump supply is through the output. If the output load is disconnected or high impedance, the output capacitors will float up to about 3.4V maximum, sourced by 960µA of leakage current. This pre-biased condition poses no issue for the converter. The 960µA leakage current may be safely bypassed to SGND. A simple application circuit is available to bypass this current in a non-dissipative manner. Please contact Applications Engineering for details.

Switching Frequency Synchronization

The SYNCI input allows the user to synchronize the controller switching frequency to the falling edge of an external clock referenced to SGND. The external clock can synchronize the unit between 50% and 110% of the preset switching frequency (F_{SW}). The SYNCI pin should be connected to SGND when not in use, and should never be left floating.

Soft Start and Tracking

The PI3740-00 provides a soft start and tracking feature using the TRK pin. Programmable Soft Start requires an external capacitor from the TRK pin to SGND in addition to the internal 56pF soft-start capacitor to set the start-up ramp period equal to t_{SS}. The recommended value is 47nF. The PI3740-00 internal reference and regulated output will proportionally follow the TRK ramp when it is below $1.7V_{DC}$. When the ramp is greater than $1.7V_{DC}$, the internal reference will remain at $1.7V_{DC}$ while the TRK ramp rises and clamps at $2.5V_{DC}$. If the TRK pin goes below the disable threshold, the regulator will finish the current switching cycle and then stop switching.

Remote Sensing Differential Amplifier

A general purpose operational amplifier is provided to assist with differential remote sensing and/or level shifting of the output voltage. The VDIFF pin can be connected to the transconductance error amplifier input EAIN pin, or with proper configuration can also be connected to the EAO pin to drive the modulator directly. If unused, connect in unity gain with VSP connected to SGND.

Power Good

The PI3740-00 PGD pin functions as a power good indicator and pulls low when the regulator is not operating or if EAIN is less than 1.4V.

Output Current Limit Protection

PI3740-00 has three methods implemented to protect from output short circuit or over current condition.

Slow Current Limit protection: prevents the regulator load from sourcing current higher than the maximum rated regulator current. If the output current exceeds the V_{OUT} Slow Current Limit (V_{OUT_SCL}) a slow current limit fault is initiated and the regulator is shutdown, which eliminates output current flow. After the Fault Restart Delay (t_{FR_DLY}), a soft-start cycle is initiated. This restart cycle will be repeated indefinitely until the excessive load is removed.

Fast Current Limit protection: monitors the external inductor current pulse-by-pulse to prevent the output from supplying saturation current. If the regulator senses a high inductor current pulse, it will initiate a fault and stop switching. After the Fault Restart Delay (t_{FR_DLY}), a soft-start cycle is initiated. This restart cycle will be repeated indefinitely until the excessive load is removed.

Overload Timeout protection: If the regulator is providing greater than the maximum output power for longer than the Overload Timeout delay (T_{OL}), it will initiate a fault and stop switching. After Fault Restart Delay (t_{FR_DLY}), a soft-start cycle is initiated. This restart cycle will be repeated indefinitely until the overload load is removed.

Input Undervoltage Lockout

If V_{IN} falls below the input Undervoltage Lockout (UVLO) threshold, the PI3740-00 will complete the current cycle and stop switching. The system will restart once the input voltage is reestablished.

Input Overvoltage Lockout

If V_{IN} rises above the input Overvoltage Lockout (OVLO) threshold, the PI3740-00 will complete the current cycle and stop switching. The system will restart once the input voltage is reestablished and after the Fault Restart Delay.

Output Overvoltage Protection

The PI3740-00 is equipped with two methods of detecting an output overvoltage condition. To prevent damage to input voltage-sensitive devices, if the output voltage exceeds 20% of its set regulated value as measured by the EAIN pin (V_{EAIN_OV}), the regulator will complete the current cycle, stop switching and issue an OVP fault. Also if the output voltage of the regulator exceeds the V_{OUT} Overvoltage Threshold (V_{OUT_OVT}) then the regulator will complete the current cycle, stop switching and issue an OVP fault. The system will resume operation once the output voltage falls below the OVP threshold and after Fault Restart Delay.

Overtemperature Protection

The PI3740-00 features an overtemperature protection (OTP), which will not engage until after the product is operated above the maximum rated temperature. The OTP circuit is only designed to protect against catastrophic failure due to excessive temperatures and should not be relied upon to ensure the device stays within the recommended operating temperature range. Thermal shutdown terminates switching and discharges the soft-start capacitor. As the temperature falls the PI3740-00 will restart, and this will always occur before the product returns to rated temperature range.

Pulse Skip Mode (PSM)

PI3740-00 features a hysteretic Pulse Skip Mode to achieve high efficiency at light loads. The regulator is setup to skip pulses if V_{EAO} falls below the Pulse Skip Threshold (V_{EAO_PST}). Depending on conditions and component values, this may result in single pulses or several consecutive pulses followed by skipped pulses. Skipping cycles significantly reduces gate drive power and improves light load efficiency. The regulator will leave Pulse Skip Mode once the control node rises above the Pulse Skip Mode threshold (V_{EAO_PST}).

Variable Frequency Operation

The PI3740-00 is preprogrammed to a fixed, maximum, base operating frequency. The frequency is selected with respect to the required power stage inductor to operate at peak efficiency across line and load variations. The switching frequency period will stretch as needed during each cycle to accommodate low line and or high load conditions. By stretching the switching frequency period, thus decreasing the switching frequency, the ZVS operation is preserved throughout the input line voltage range maintaining optimum efficiency.

IMON Amplifier

The PI3740-00 provides a differential amplifier with a level shifted, SGND referenced output, the IMON Pin, which is useful for sensing input or output current on high voltage rails. A fixed gain of 20:1 is provided over a large common mode range. When using the amplifier, the ISN pin must be referenced to the common mode voltage of the ISP pin for proper operation. See Absolute Maximum Ratings for more information. If not in use, the ISN and ISP pins should be connected to SGND and the IMON pin left floating.

Application Description

Output Voltage Trim

The output voltage can be adjusted by feeding back a portion of the desired output through a voltage divider to the error amplifier's input (see Figure 37). Equation 1 can be used to determine resistor values needed for the voltage divider.

$$R1 = R2 \bullet \left(\frac{V_{OUT}}{1.7} - 1 \right) \qquad (1)$$

The R2 value is selected by the user; a 1.65kΩ resistor value is recommended.

If, for example, a 12V output is needed, the user can select a 1.65kΩ (1%) resistor for R2 and use Equation 1 to calculate R1. Once R1 value is calculated, the user should select the nearest resistor value available. In this example, R1 is 9.997kΩ so a 10.0kΩ should be selected.

Soft Start Adjustment and Tracking

The TRK pin offers a means to increase the regulator's soft-start time or to track with additional regulators. The soft-start slope is controlled by an external capacitor and a fixed charge current to provide the startup ramp. The following equation can be used to calculate the proper capacitor for a desired soft-start time:

$$C_{TRK} = \frac{(t_{TRK} \bullet I_{SS})}{1.7} - 56 \bullet 10^{-12} \qquad (2)$$

Where t_{TRK} is the desired soft-start time and I_{SS} is the TRK pin source current (see Electrical Characteristics for limits).

The PI3740-00 allows the tracking of multiple like regulators. Two methods of tracking can be chosen: proportional or direct tracking. Proportional tracking will force all connected regulators to startup and reach regulation at the same time (see Figure 38 (a)). To implement proportional tracking, simply connect all devices TRK pins together.

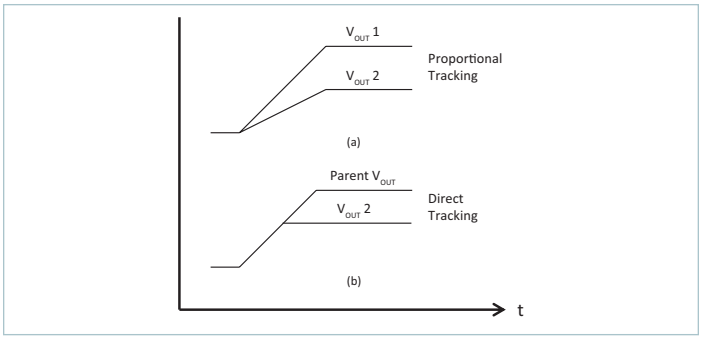


Figure 38 — *PI3740-00 tracking methods*

For Direct Tracking, choose the regulator with the highest output voltage as the parent and connect the parent to the TRK pin of the other regulators through a divider (Figure 39) with the same ratio as the child's feedback divider (see Output Voltage Trim). The TRK pin should not be driven without 1kΩ minimum series resistance.

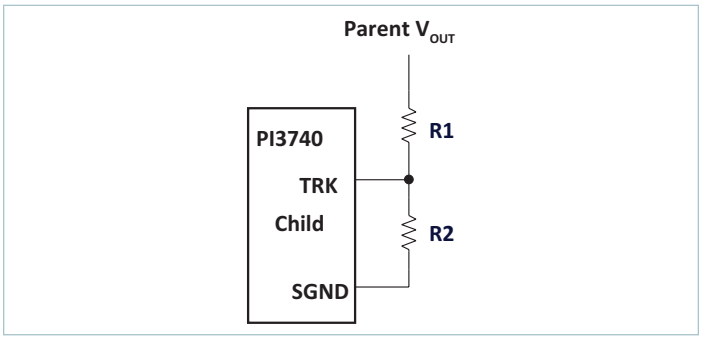


Figure 39 — *Voltage divider connections for direct tracking*

All connected regulators' soft-start slopes will track with this method. Direct tracking timing is demonstrated in Figure 38 (b). All tracking regulators should have their Enable (EN) pins connected together for proper operation.

Inductor Pairing

The PI3740-00 utilizes an external inductor. This inductor has been optimized for maximum efficiency performance. **Product specifications are guaranteed by use of the specific, approved inductor(s) listed in the inductor pairing table. Use of any other inductor shall void product specifications and warranty.**

Table 1 details the specific inductor value and part number utilized for PI3740-00.

Device	Inductor (nH)	Inductor Part Number	Manufacturer
PI3740-00	420	HCV1206-R42-R	Eaton
		PA5119.421NLT	Pulse

Table 1 — *PI3740-00 inductor pairing*

Filter Considerations

The PI3740-00 requires low impedance ceramic input capacitors (X7R/X5R or equivalent) to ensure proper start up and high frequency decoupling for the power stage. The PI3740-00 will draw nearly all of the high frequency current from the low impedance ceramic capacitors when the main high side MOSFET(s) are conducting. During the time the MOSFET(s) are off, the input capacitors are replenished from the source. Table 2 shows the recommended input and output capacitors to be used for the PI3740-00. Divide the total RMS current by the number of ceramic capacitors used to calculate the individual capacitor's RMS current. Table 3 includes the recommended input and output ceramic capacitor. It is very important to verify that the voltage supply source as well as the interconnecting line are stable and do not oscillate.

Input Filter case 1; Inductive source and local, external, input decoupling capacitance with negligible ESR (i.e., ceramic type)

The voltage source impedance can be modeled as a series R_{LINE} L_{LINE} circuit. The high performance ceramic decoupling capacitors will not significantly damp the network because of their low ESR; therefore in order to guarantee stability the following conditions must be verified:

$$R_{LINE} > \frac{L_{LINE}}{\left(C_{IN\_INT} + C_{IN\_EXT}\right) \bullet \left|r_{EQ\_IN}\right|} \qquad (3)$$

$$R_{LINE} << \left|r_{EQ\_IN}\right| \qquad (4)$$

Where r_{EQ_IN} can be calculated by dividing the lowest line voltage by the full load input current. It is critical that the line source impedance be at least an octave lower than the converter's dynamic input resistance, Equation 4. However, R_{LINE} cannot be made arbitrarily low otherwise Equation 3 is violated and the system will show instability, due to under-damped RLC input network.

Input Filter case 2; Inductive source and local, external input decoupling capacitance with significant R_{CIN_EXT} ESR (i.e., electrolytic type)

In order to simplify the analysis in this case, the voltage source impedance can be modeled as a simple inductor L_{LINE}. Notice that the high performance ceramic capacitors C_{IN_INT} within the PI3740-00 should be included in the external electrolytic capacitance value for this purpose. The stability criteria will be:

$$\left|r_{EQ\_IN}\right| > R_{C_{IN\_EXT}} \qquad (5)$$

$$\frac{L_{LINE}}{C_{IN\_INT} \bullet R_{C_{IN\_EXT}}} < \left|r_{EQ\_IN}\right| \qquad (6)$$

Equation 6 shows that if the aggregate ESR is too small – for example by using very high quality input capacitors (C_{IN_EXT}) – the system will be under-damped and may even become destabilized. Again, an octave of design margin in satisfying Equation 5 should be considered the minimum.

Note: When applying an electrolytic capacitor for input filter damping the ESR value must be chosen to avoid loss of converter efficiency and excessive power dissipation in the electrolytic capacitor.

C_{INPUT} (see Table 3)	C_{OUTPUT} (see Table 3)
5 X 2.2µF	8 X 10µF or 2.2µF

Table 2 — *Minimum recommended input and output capacitance*

Part Number	Description	MFG Description
GRM32ER72A225KA35 (or equivalent)	2.2µF Capacitor, X7R 20% 100V, 1210	Murata
GRM32ER71H106KA12 (or equivalent)	10µF Capacitor X7R 20% 50V, 1210	Murata

Table 3 — *Capacitor manufacturer part numbers*

V_{OUT} (V)	V_{IN} (V)	I_{OUT} (A)	C_{INPUT} Ripple Current (I_{RMS})	C_{OUTPUT} Ripple Current (I_{RMS})	Input Ripple (mV_{P-P})	Output Ripple C_{OUT} = 10µF (mV_{P-P})	Output Ripple C_{OUT} = 2.2µF (mV_{P-P})
10	8	5.01	5.27	5.70	468	120	333
10	12	5.01	4.50	4.80	285	82	198
10	16	6.02	4.70	5.30	296	88	206
10	18	7.02	5.28	5.95	351	114	244
10	24	7.02	4.66	5.68	274	88	201
10	28	7.42	4.60	5.88	270	90	204
10	36	7.42	4.04	5.73	232	84	183
10	48	6.82	3.30	5.50	200	62	171
10	60	6.02	2.63	5.30	183	62	163
12	8	5.01	6.00	6.20	540	154	375
12	12	6.02	5.80	6.17	432	118	300
12	16	6.62	5.50	6.00	354	119	245
12	18	6.82	5.60	6.15	352	111	244
12	24	7.02	5.00	6.00	290	96	206
12	28	7.02	4.75	5.87	260	89	190
12	36	7.02	4.30	6.00	247	84	193
12	48	6.22	3.45	5.80	220	75	186
12	60	5.21	2.70	5.41	188	64	170
18	8	3.61	5.43	5.51	416	150	310
18	12	5.01	5.71	6.20	372	201	288
18	16	5.41	5.53	5.90	309	125	225
18	18	5.82	5.70	6.00	311	119	223
18	24	6.22	5.73	6.45	319	115	227
18	28	6.22	5.50	6.50	316	116	228
18	36	5.62	4.80	6.35	285	114	217
18	48	5.01	3.90	6.00	257	110	203
18	60	4.21	3.05	5.60	221	107	181
24	8	3.01	6.20	5.54	490	193	319
24	12	4.01	5.50	5.60	312	198	258
24	16	4.61	5.43	5.74	274	134	215
24	18	5.01	5.80	6.00	306	139	229
24	24	5.01	5.80	6.26	330	144	232
24	28	5.01	5.70	6.30	330	146	233
24	36	4.61	5.00	6.20	300	146	222
24	48	4.21	4.20	6.05	282	142	209
24	60	3.61	3.30	5.50	248	136	186

V_{OUT} (V)	V_{IN} (V)	I_{OUT} (A)	C_{INPUT} Ripple Current (I_{RMS})	C_{OUTPUT} Ripple Current (I_{RMS})	Input Ripple (mV_{P-P})	Output Ripple C_{OUT} = 10µF (mV_{P-P})	Output Ripple C_{OUT} = 2.2µF (mV_{P-P})
28	8	2.30	5.50	4.71	390	176	240
28	12	3.61	5.62	5.75	320	230	260
28	16	4.41	5.63	5.88	277	158	230
28	18	4.41	5.80	5.90	300	156	228
28	24	4.61	6.00	6.20	240	164	239
28	28	4.41	5.70	6.20	334	166	233
28	36	4.21	5.20	6.15	315	168	225
28	48	3.61	4.10	5.70	281	162	200
28	60	3.21	3.40	5.36	255	152	184
36	8	1.70	6.00	4.06	357	175	195
36	12	2.41	5.40	4.85	280	170	206
36	16	3.41	5.62	5.47	266	188	217
36	18	3.61	5.85	5.64	290	192	228
36	24	3.61	5.89	5.68	332	196	230
36	28	3.61	5.79	5.77	337	200	231
36	36	3.61	5.44	5.90	337	208	232
36	48	3.21	4.50	5.60	314	196	212
36	60	2.61	3.47	5.00	264	174	180
50	8	1.80	8.30	5.50	740	N/A	444
50	12	2.40	7.07	5.49	425	N/A	336
50	16	2.80	6.36	5.52	306	N/A	340
50	18	3.00	6.55	5.70	322	N/A	360
50	24	2.60	5.87	5.00	319	N/A	316
50	28	2.50	5.56	4.93	320	N/A	312
50	36	2.50	5.20	5.00	323	N/A	316
50	48	2.40	4.60	4.96	300	N/A	324
50	60	2.50	4.20	5.34	342	N/A	332

Table 4 — *Typical input and output ripple current / voltage with the recommended input and output capacitor recommended in Tables 1 and 2.*

PI3740-00 Maximum C_{OUT} Capability at Start Up

If the output capacitance (C_{OUT}) exceeds the Max Output Capacitance (C_{OUT_MAX}) listed in Figure 40 (full resistive start-up load) or Figure 41 (no start-up load), the external C_{SS} needs to be adjusted to a higher value than the recommended C_{SS}=47nF.

Under this condition, the external C_{SS} should be adjusted to a minimum of 1.3 • 47nF • (C_{OUT}/C_{OUT_MAX}) for successful start up. The ratio of 1.3 is recommended margin. In addition, excessive C_{SS} may also cause issue if there is still residual charge before the module attempts to start up.

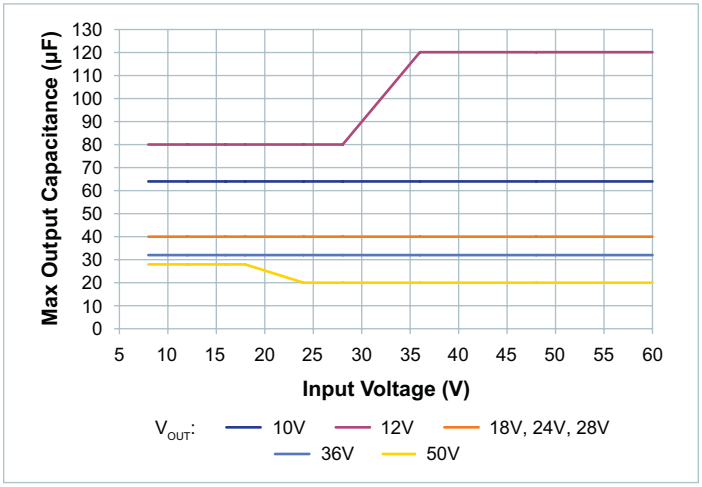


Figure 40 — *Max output capacitance with full resistive start-up load with external C_{SS} = 47nF*

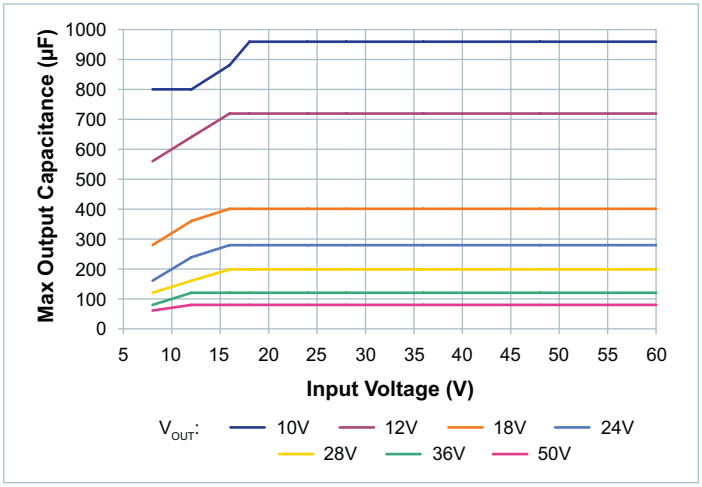


Figure 41 — *Max output capacitance with no start-up load with external C_{SS} = 47nF*

Thermal Design

Figure 42 (a) shows a thermal impedance model that can predict the maximum temperature of the highest temperature component for a given operating condition. This model assumes that all customer PCB connections are at one temperature, which is PCB equivalent Temperature T_{PCB} °C. The model can be simplified as shown in Figure 42 (b).

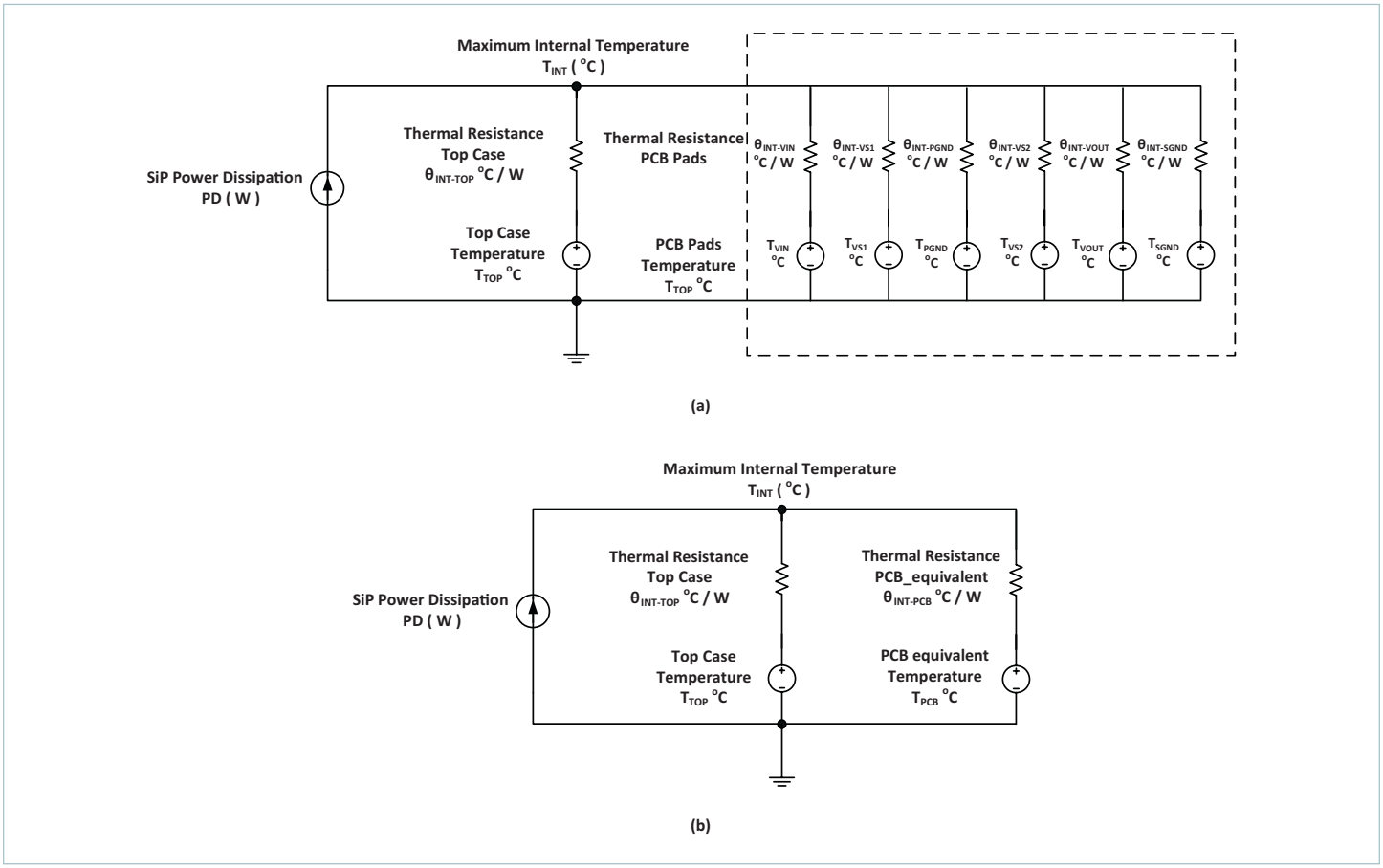


Figure 42 — *PI3740-00 SiP thermal model (a) and its simplified version (b).*

Where the symbol in Figure 42 is defined as the following:

$\theta_{INT\text{-}TOP}$	is defined as the thermal impedance from the hottest component junction inside the SiP to the top side of the package.
$\theta_{INT\text{-}PCB}$	is defined as the thermal impedance from the hottest component junction inside the SiP to the circuit board it is mounted on, assuming all customer PCB connections at one temperature.
$\theta_{INT\text{-}VIN}$	is defined as the thermal impedance from the hottest component junction inside the SiP to the circuit board it is mounted on at the V_{IN} pad.
$\theta_{INT\text{-}VS1}$	is defined as the thermal impedance from the hottest component junction inside the SiP to the circuit board it is mounted on at the VS1 pad.
$\theta_{INT\text{-}PGND}$	is defined as the thermal impedance from the hottest component junction inside the SiP to the circuit board it is mounted on at the PGND pad.
$\theta_{INT\text{-}VS2}$	is defined as the thermal impedance from the hottest component junction inside the SiP to the circuit board it is mounted on at the VS2 pad.
$\theta_{INT\text{-}VOUT}$	is defined as the thermal impedance from the hottest component junction inside the SiP to the circuit board it is mounted on at the V_{OUT} pad.
$\theta_{INT\text{-}SGND}$	is defined as the thermal impedance from the hottest component junction inside the SiP to the circuit board it is mounted on at the SGND pad.

The following equation can predict the junction temperature based on the heat load applied to the SiP and the known ambient conditions with the simplified thermal circuit model:

$$T_{INT} = \frac{PD + \frac{T_{TOP}}{\theta_{INT\text{-}TOP}} + \frac{T_{PCB}}{\theta_{INT\text{-}PCB}}}{\frac{1}{\theta_{INT\text{-}TOP}} + \frac{1}{\theta_{INT\text{-}PCB}}} \qquad (7)$$

Device	Thermal Impedance							Thermal Impedance with the simplified version	
	$\theta_{INT\text{-}TOP}$ (°C / W)	$\theta_{INT\text{-}VIN}$ (°C / W)	$\theta_{INT\text{-}VS1}$ (°C / W)	$\theta_{INT\text{-}PGND}$ (°C / W)	$\theta_{INT\text{-}VS2}$ (°C / W)	$\theta_{INT\text{-}VOUT}$ (°C / W)	$\theta_{INT\text{-}SGND}$ (°C / W)	$\theta_{INT\text{-}TOP}$ (°C / W)	$\theta_{INT\text{-}PCB}$ (°C / W)
PI3740-00	41	3.9	8.1	6.8	10	4.9	57	41	1.2

Table 5 — *PI3740-00 SiP thermal impedance*

Thermal Design Inductor

Figure 43 (a) shows a thermal impedance model that can predict the maximum hot-spot temperature of the inductor for a given operating condition. This model assumes that all customer PCB connections are at one temperature, which is PCB equivalent Temperature T_{PCB} °C. If the inductor top and bottom are not mounted to a heat sink, the simplified model is parallel combination of all resistances that connect to the PCB. The model can be simplified as shown in Figure 43 (b).

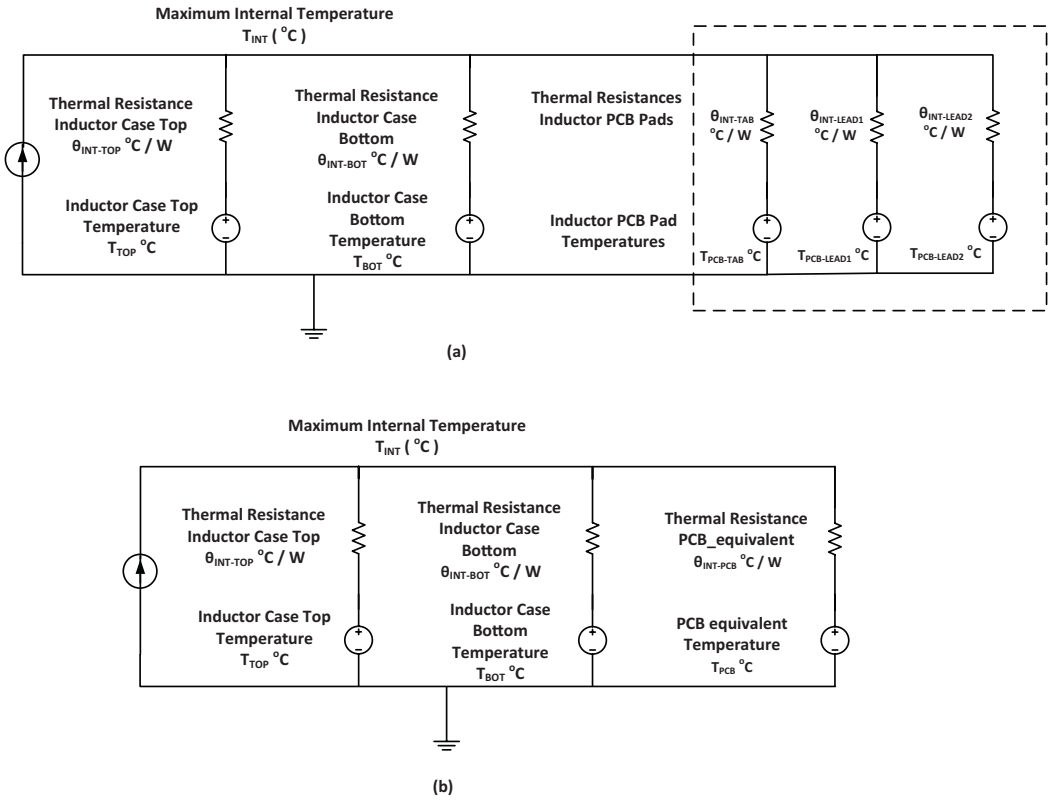


Figure 43 — *PI3740-00 inductor thermal impedance model*

Where the symbol in Figure 43 is defined as the following:

$\theta_{INT-TOP}$	is defined as the thermal impedance from the hot spot to the top surface of the core.
$\theta_{INT-PCB}$	is defined as the thermal impedance from the hot spot to the circuit board it is mounted on, assuming all customer PCB connections are at one temperature.
$\theta_{INT-BOT}$	is defined as the thermal impedance from the hot spot to the bottom surface of the core.
$\theta_{INT-TAB}$	is defined as the thermal impedance from the hot spot to the metal mounting tab on the core body.
$\theta_{INT-LEAD1}$	is defined as the thermal impedance from the hot spot to one of the mounting leads. Since the leads are the same thermal impedance, there is no need to specify by explicit pin number
$\theta_{INT-LEAD2}$	is defined as the thermal impedance from the hot spot to the other mounting lead

The following equation can predict the junction temperature based on the heat load applied to the inductor and the known ambient conditions with the simplified thermal circuit model:

$$T_{HOT\ SPOT} = \frac{PD + \frac{T_{TOP}}{\theta_{INT\text{-}TOP}} + \frac{T_{PCB}}{\theta_{INT\text{-}PCB}}}{\frac{1}{\theta_{INT\text{-}TOP}} + \frac{1}{\theta_{INT\text{-}PCB}}} \qquad (8)$$

Device	Thermal Impedance					Thermal Impedance with the simplified version		
	$\theta_{INT\text{-}TOP}$ (°C / W)	$\theta_{INT\text{-}BOT}$ (°C / W)	$\theta_{INT\text{-}TAB}$ (°C / W)	$\theta_{INT\text{-}LEAD1}$ (°C / W)	$\theta_{INT\text{-}LEAD2}$ (°C / W)	$\theta_{INT\text{-}TOP}$ (°C / W)	$\theta_{INT\text{-}BOT}$ (°C / W)	$\theta_{INT\text{-}PCB}$ (°C / W)
Inductor	30	15	440	61	61	30	15	28

Table 6 — *PI3740-00 inductor thermal impedance*

An estimation of SiP power loss to total loss percentage is shown in the following charts.

PI3740-00 Percentage of SiP Loss to Total Loss

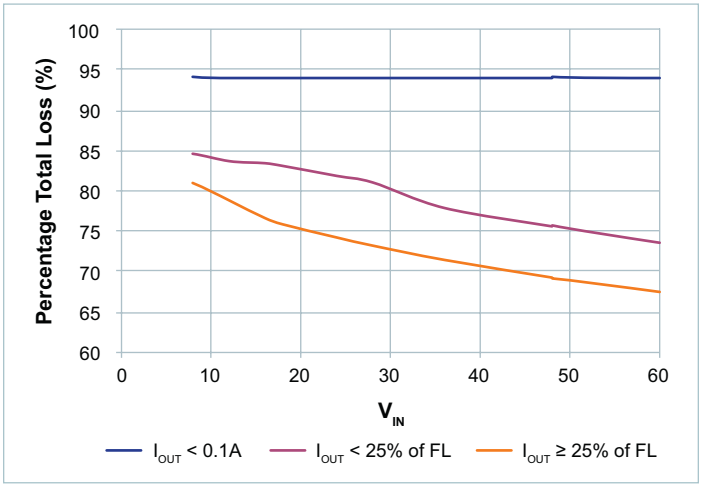


Figure 44 — *V_{OUT} = 10V*

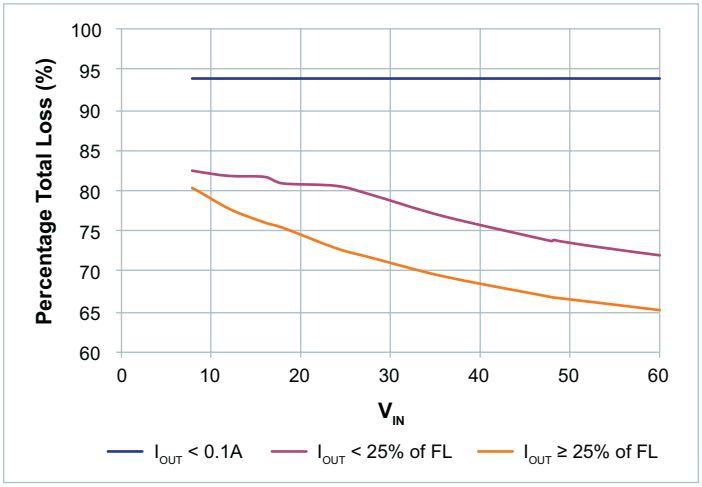


Figure 45 — *V_{OUT} = 12V*

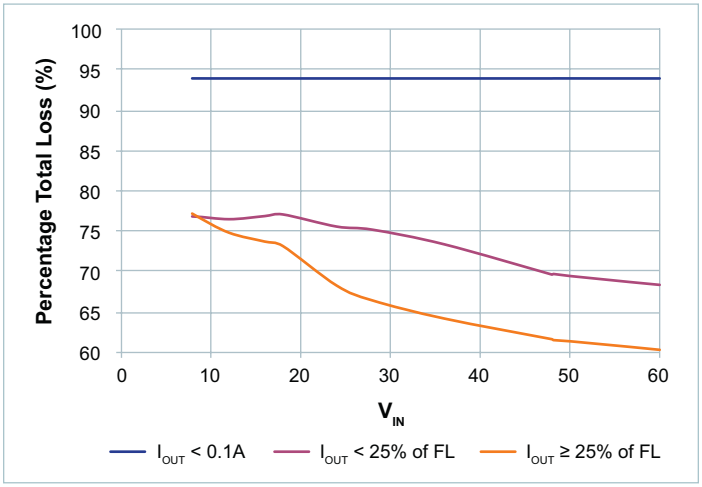


Figure 46 — *V_{OUT} = 18V*

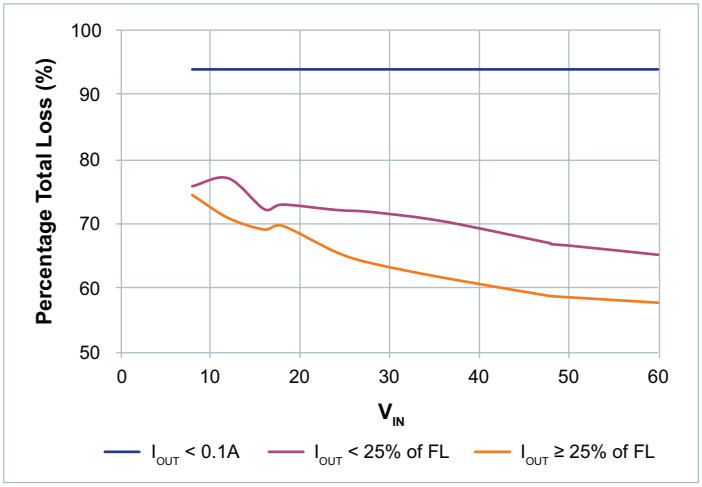


Figure 47 — *V_{OUT} = 24V*

PI3740-00 Percentage of SiP Loss to Total Loss (Cont.)

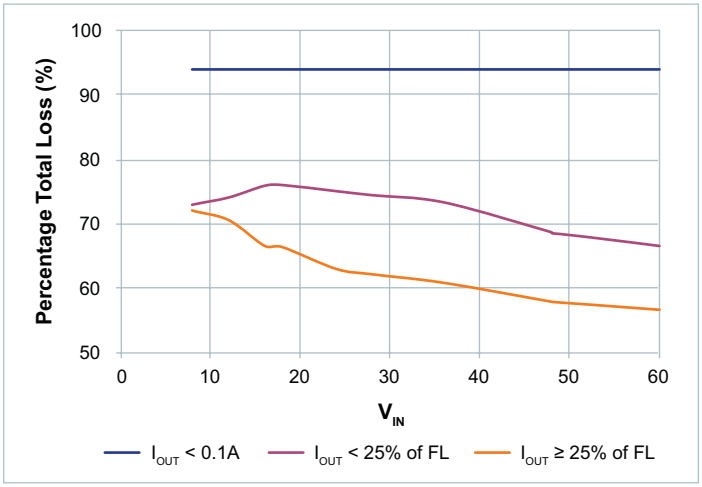


Figure 48 — V_{OUT} = 28V

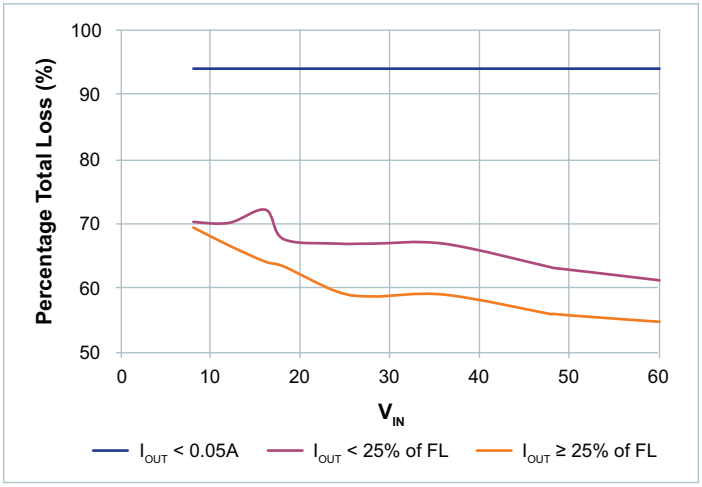


Figure 49 — V_{OUT} = 36V

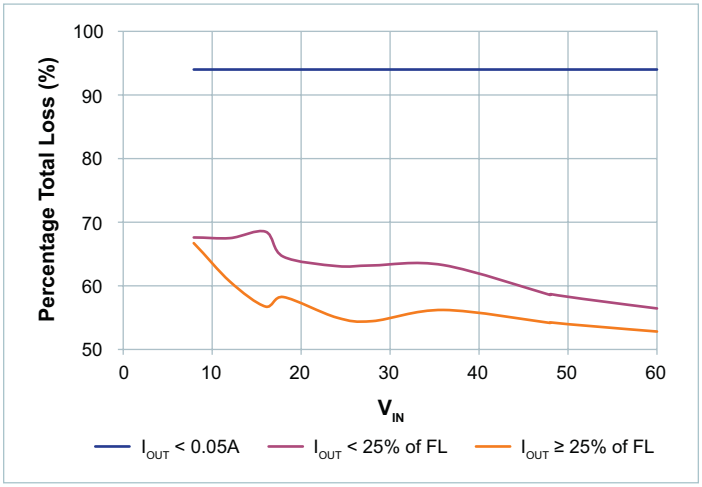


Figure 50 — V_{OUT} = 50V

Evaluation Board Thermal De-rating

Thermal de-rating curves are provided that are based on component temperature changes versus load current, input voltage and no air flow. It is recommended to use these curves as a guideline for proper thermal de-rating. These curves represent the entire system and are inclusive to both the Vicor SiP and the external inductor. Maximum thermal operation is limited by either the MOSFETs or inductor depending upon line and load conditions.

All thermal testing was performed using a 3 x 3in, four 2oz copper layers, FR4 evaluation board platform. Thermal measurements were made on the four internal MOSFETS and the external inductor.

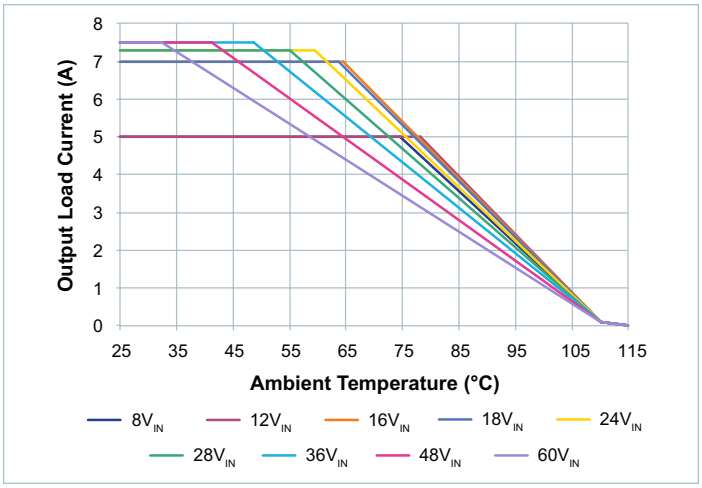


Figure 51 — *Thermal de-rating for PI3740-00 evaluation board at V_{OUT} = 10V, 0LFM*

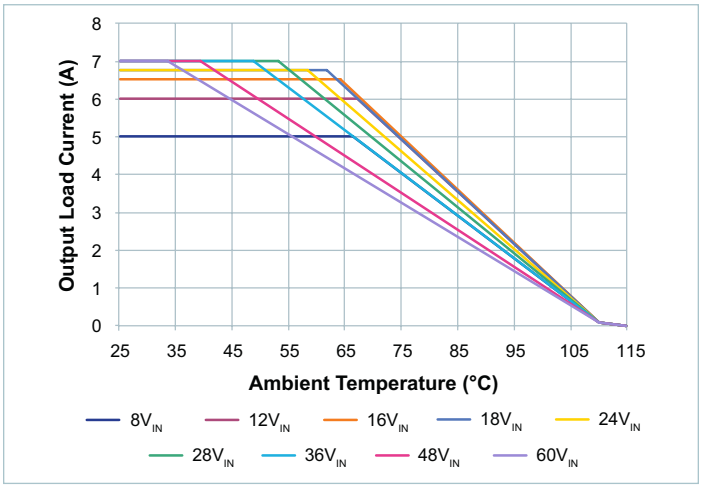


Figure 52 — *Thermal de-rating PI3740-00 evaluation board at V_{OUT} = 12V, 0LFM*

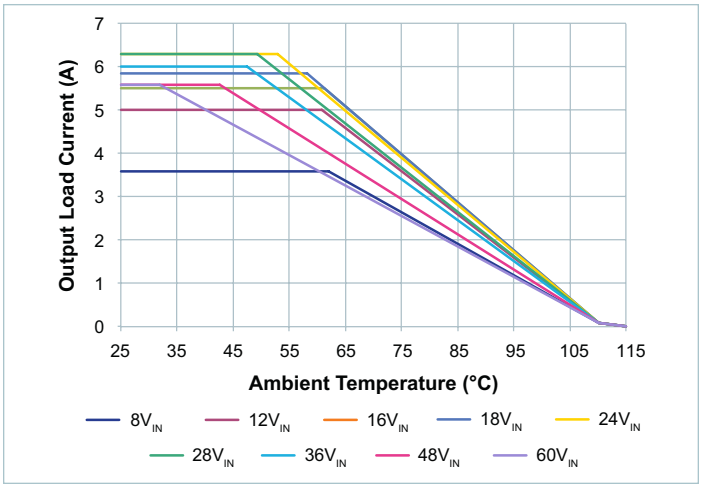


Figure 53 — *Thermal de-rating for PI3740-00 evaluation board at V_{OUT} = 18V, 0LFM*

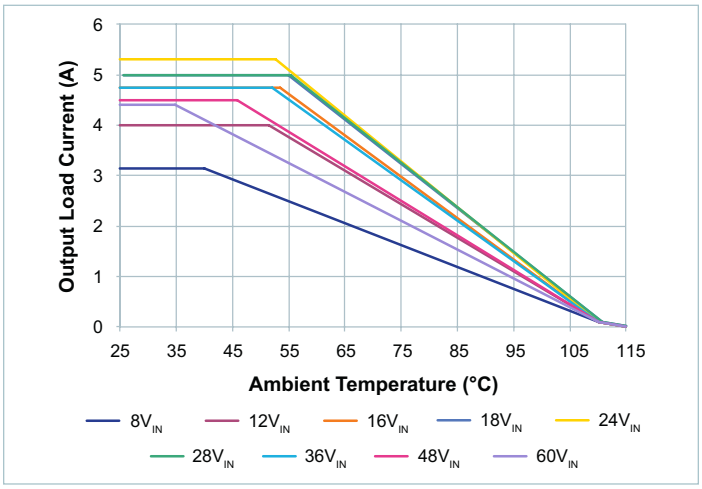


Figure 54 — *Thermal de-rating for PI3740-00 evaluation board at V_{OUT} = 24V, 0LFM*

Evaluation Board Thermal De-rating (Cont.)

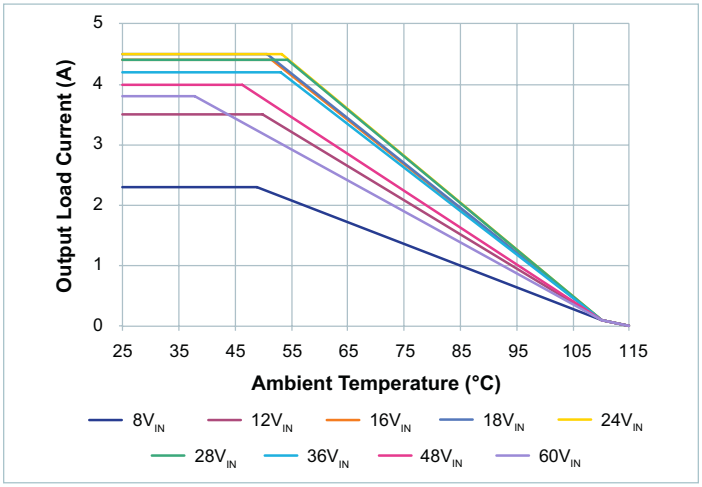


Figure 55 — *Thermal de-rating PI3740-00 evaluation board at V_{OUT} = 28V, 0LFM*

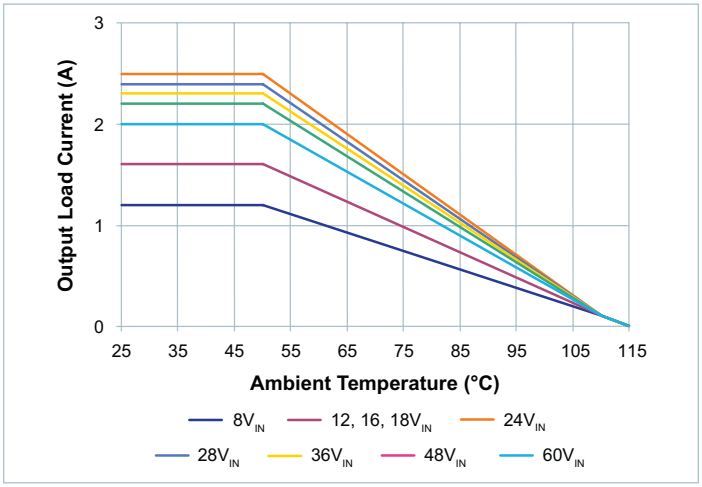


Figure 57 — *Thermal de-rating for PI3740-00 evaluation board at V_{OUT} = 50V, 0LFM*

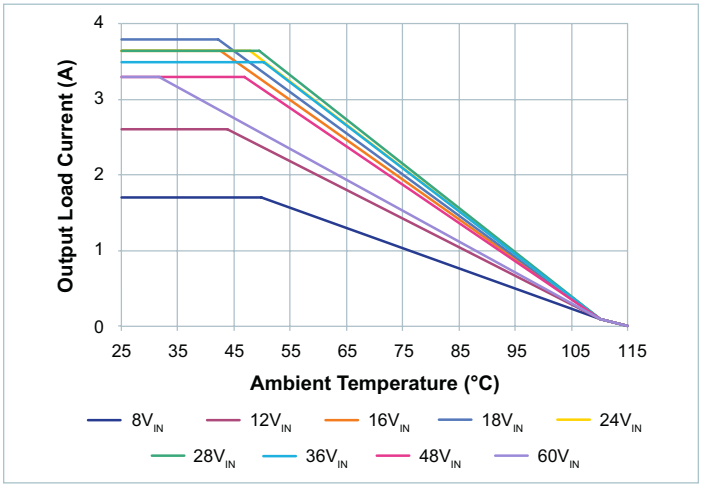


Figure 56 — *Thermal de-rating for PI3740-00 evaluation board at V_{OUT} = 36V, 0LFM*

Parallel Operation

PI3740-00 can be connected in parallel to increase the output capability of a single output rail. When connecting modules in parallel, each EAO, TRK, and EN pin should be connected together. Current sharing will occur automatically in this manner so long as each inductor is the same value. EAIN pins should remain separated, each with an REA1 and REA2, to reject noise differences between different modules' SGND pins. Up to three modules may be connected in parallel. The modules current sharing accuracy is determined by the inductor tolerance (±10%) and to a lesser extent, timing variation (±1.5%). Current sharing may be considered independent of synchronization and/or interleaving. Modules do not have to be interleaved or synchronized to share current. The following equation determines the output capability of N modules (up to three) to be determined:

$$I_{array} = I_{mod} + \left(I_{mod} \bullet (N-1) \bullet 0.77\right) \qquad (9)$$

Where:

I_{array} is the maximum output current of the array

I_{mod} is the maximum output per module

N is the number of modules

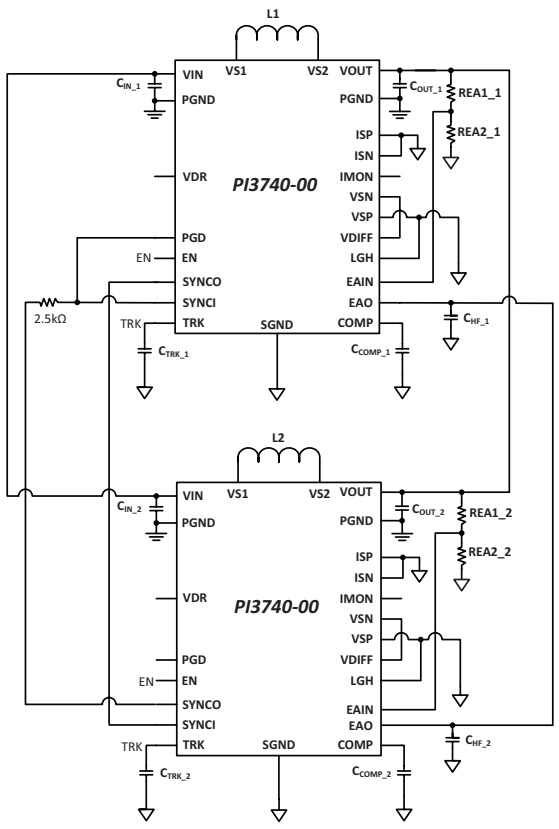


Figure 58 — *PI3740-00 parallel operation*

Synchronization

PI3740-00 units may be synchronized to an external clock by driving the SYNCI pin. The synchronization frequency must not be higher than 110% of the programmed maximum value F_{SW}. This is the switching frequency during DCM of operation. The minimum synchronization frequency is F_{SW} / 2. In order to ensure proper power delivery during synchronization, the user should refer to the switching frequency vs. output current curves for the load current, output voltage and input voltage operating point. The synchronization frequency should not be lower than that determined by the curve or reduced output power will result. The power reduction is approximately the ratio between required frequency and synchronizing frequency. If the required frequency is 1MHz and the sync frequency is 600kHz, the user should expect a 40% reduction in output capability.

Interleaving

Interleaving is primarily done to reduce output ripple and the required number of output capacitors by introducing phase current cancellation. The PI3740-00 has a fixed delay that is proportional to to the maximum value of F_{SW} shown in the datasheet. When connecting two units as showin in
Figure 58, they will operate at 180 degrees out of phase when the converters switching frequency is equal to F_{SW}. If the converter enters CrCM and the switching frequency is lower than F_{SW}, the phase delay will no longer be 180 degrees and ripple cancellation will begin to decay. Interleaving when the switching frequency is reduced to lower than 80% of the programmed maximum value is not recommended. Operation over high-boost ratios such as 8V in to 36V out or narrow buck ratios like 28V in to 24V is not recommended for interleaving.

Small-Signal Models CV-CC Modes

Small-Signal Model – Constant Voltage Mode

The PI3740-00 product is a variable frequency CrCM / DCM ZVS Buck-Boost Regulator. The small-signal model for this powertrain is that of a voltage controlled current source which has a trans-conductance that varies depending on the operating mode. When the converter is operating at its programmed frequency, it is in discontinuous mode. As the load increases to the point at which the boundary between discontinuous and continuous modes is reached, the powertrain changes frequency to remain in critical conduction mode. This mode of operation allows the PI3740-00 product family to have a very simple compensation scheme, as the control to output transfer function always has a slope of –1. In addition, when critical conduction is reached, the voltage controlled current source becomes more ideal with a higher output equivalent resistance with less variation.

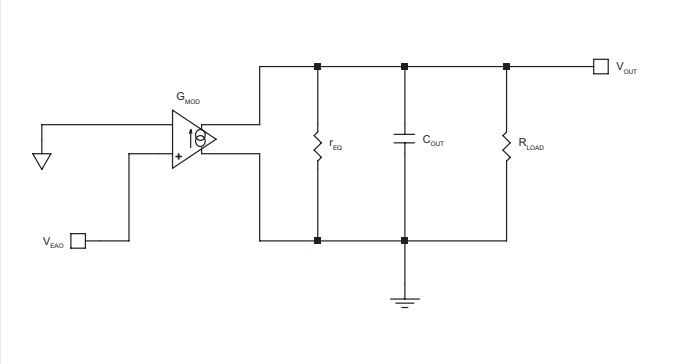


Figure 59 — *PI3740-00 small-signal model control-output*

The Control-Output transfer function (also known as the small-signal modulator gain) has a single pole response determined by the parallel combination of Rload and r_{EQ} and the output capacitor C_{OUT}. Equation 10 determines the frequency of the modulator pole:

$$Fpmod = \frac{1}{2 \bullet \pi \bullet \left(\frac{R_{LOAD} \bullet r_{EQ}}{R_{LOAD} + r_{EQ}} \right) \bullet C_{OUT}} \qquad (10)$$

Error Amplifier

The small signal model of the error amplifier and compensator is shown in Figure 60. The error amplifier is a wide bandwidth Trans-Conductance Amplifier (TCA). It is capable of sourcing and sinking ±400µA. Here it is important to note that the external components are C_{COMP}, C_{HF}, R1 and R2. R_{ZI} is pre-programmed by the factory and is internal to the PI3740-00 SiP.

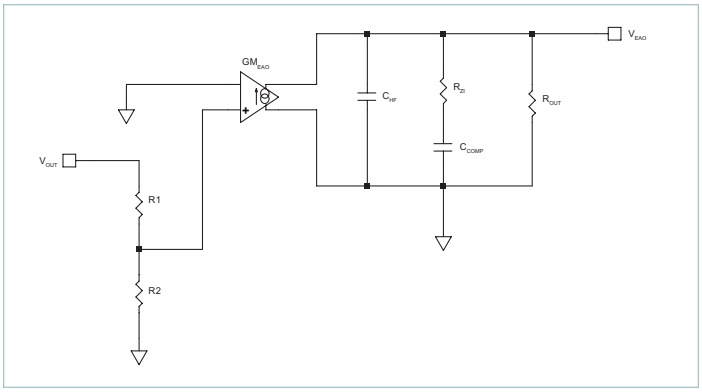


Figure 60 — *PI3740-00 error amplifier model*

When the amplifier is configured as shown in Figure 60, it forms a Type II amplifier configuration with poles and zeros determined by:

$$Fplf = \frac{1}{2 \bullet \pi \bullet (R_{ZI} + R_{OUT}) \bullet (C_{COMP} + C_{HF})} \qquad (11)$$

$$Fzmb = \frac{1}{2 \bullet \pi \bullet (R_{ZI} // R_{OUT}) \bullet C_{COMP}} \qquad (12)$$

$$Fphf = \frac{C_{HF} + C_{COMP}}{2 \bullet \pi \bullet (R_{ZI} // R_{OUT}) \bullet C_{COMP} \bullet C_{HF}} \qquad (13)$$

Lighting Mode (LGH)

The Lighting (LGH) mode allows the PI3740-00 product to be able to operate in constant current mode (CC) so that it can support a wide range of applications that require the ability to regulate current or voltage. Primary applications are LED lighting, battery / super-capacitor charging and high peak current pulse transient load applications. The PI3740-00 product family can operate in dual modes, either as a constant voltage (CV) regulator or a constant current (CC) regulator. Both modes can be utilized in a single system. The PI3740-00 has a separate current amplifier, called LGH, and built in 100mV lighting reference that has its output connected to the EAO pin internally. If the current through an external shunt starts to develop 100mV at the LGH pin, the LGH amplifier will take over regulation by pulling down on the EAO output until the current is in regulation according to the designed shunt value. The LGH amplifier is a sink only trans-conductance amplifier (TCA). It does not source current. In the event of an open LED string or open-current signal, the voltage loop can be set to regulate the output voltage to a safe or desired value in CV mode.

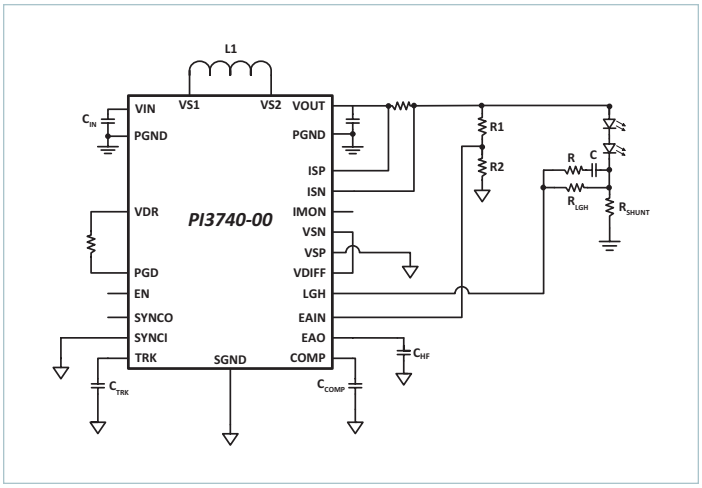


Figure 61 — *Lighting configuration using CC mode*

When using the CC mode, it is important to set R1 and R2 appropriately to avoid voltage loop interaction with the current loop. In this case, the voltage setting at the EAIN pin should be set so that the error between it and the 1.7V reference is sufficient to force the EAO to be open loop and source current always. When not using the LGH amplifier, the LGH pin should be connected to SGND.

The LGH amplifier is able to sink more current than the error amplifier can source, thus avoiding arbitration issues when transitioning back and forth from LGH mode to voltage mode. The equation for setting the source current for EAO is shown in Equation 14.

$$I_{EAO} = (V_{EAIN} - V_{REF}) \bullet G_{MEA} > 400\mu A \qquad (14)$$

LGH Amplifier Small-Signal Model

A small signal model of the LGH amplifier is shown in Figure 62.

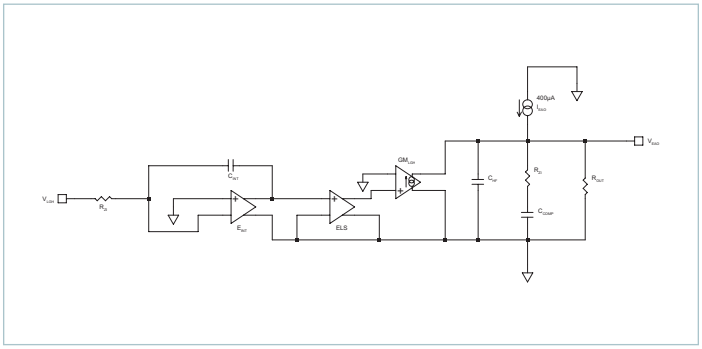


Figure 62 — *LGH amplifier small-signal model*

The LGH amplifier consists of three distinct stages. The first is a wide-bandwidth integrator stage, followed by a fixed gain level shift circuit. Finally, the level shift circuit drives a trans-conductance (TCA) amplifier with an open collector sink only output stage. Since the LGH output is internally connected to the output of the voltage error amplifier, the compensation components show up in the model and are used by both stages, depending on which one is in use. Only one stage should be in use at a time. When using LGH or if the LGH input rises above the internal reference, the voltage error amplifier acts as a 400µA current source pull up for the EAO pin.

The integrator pole is determined by the external input resistor R_{LGH} and the internal C_{INT}, which is 20pF. Assuming R_{LGH} = 100kΩ and E_{INT} = 100000:

$$F_{PE_{INT}} = \frac{1}{2 \bullet \pi \bullet (R_{LGHT} \bullet C_{INT} \bullet E_{INT})} = 0.795Hz \qquad (15)$$

Figure 60 shows a small signal model of the modulator gain when using the application circuit shown in Figure 61 with two high current LED's in series. R_{LED} is the series combination of the AC resistance of each LED. R_{SHUNT} is used to sense the current through the LED string. Equation 16 defines the pole of transfer function.

$$F_{PLED} = \frac{1}{2 \bullet \pi \bullet ((R_{LED} + R_{SHUNT}) // r_{EQ} \bullet C_{OUT}} \qquad (16)$$

When regulating in CC mode, it will be necessary to add a compensating zero to avoid loss of phase margin caused by the integrator stage of the LGH amplifier. A simple approach is to add a series R–C in parallel with R_{LGH} as shown in the lighting application diagram in Figure 61. The capacitor will be chosen to work with R_{LGH} to add a zero approximately 1.2kHz before the zero provided by the GM_{LGH} transfer function (the trans-conductance stage of the LGH amplifier). The external added resistor will form a high frequency pole to roll the gain off at higher frequency. Note that it is very important to understand the AC resistance of the LED's that are being used. Please consult the LED manufacturer for details. For a series string, you should add the individual LED resistances and combine them into one lumped value to simplify the analysis.

VDR Bias Regulator

The VDR internal bias regulator is a ZVS switching regulator that resides internal to the PI3740-00 SiP. It is intended primarily to power the internal controller and driver circuitry. The power capability of this regulator is sized only for the PI3740-00, with adequate reserve for the application it was intended for. It may be used as a pull-up source for open-collector applications and for other very low power uses with the following restrictions:

- The total external loading on VDR must be less than 2mA.
- No direct connection is allowed. Any noise source that can disturb the VDR voltage can also affect the internal controller operation. A series impedance is required between the VDR pin and any external circuitry.
- All loads must be locally decoupled using a 0.1µF ceramic capacitor. This capacitor must be connected to the VDR output through a series resistor no smaller than 1kΩ, which forms a low-pass filter.

PI3740-00 Modulator Gain / Output Resistance T_{PCB} = 25°C

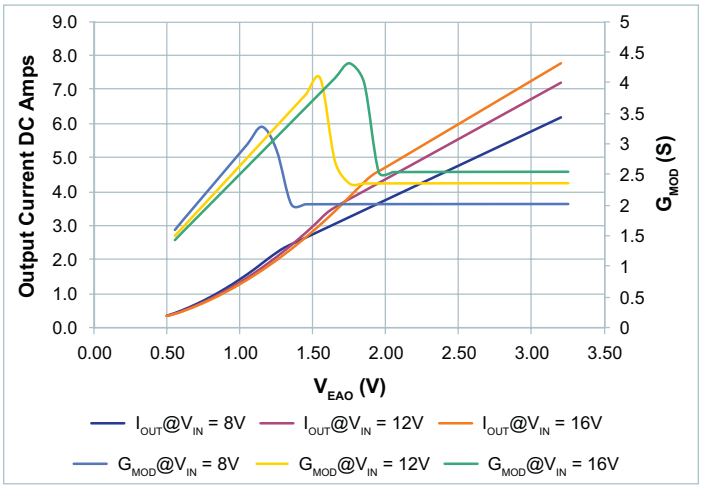


Figure 63 — *G_{MOD} vs output current vs. V_{EAO}, V_{OUT} = 10V; 8 – 16V_{IN}*

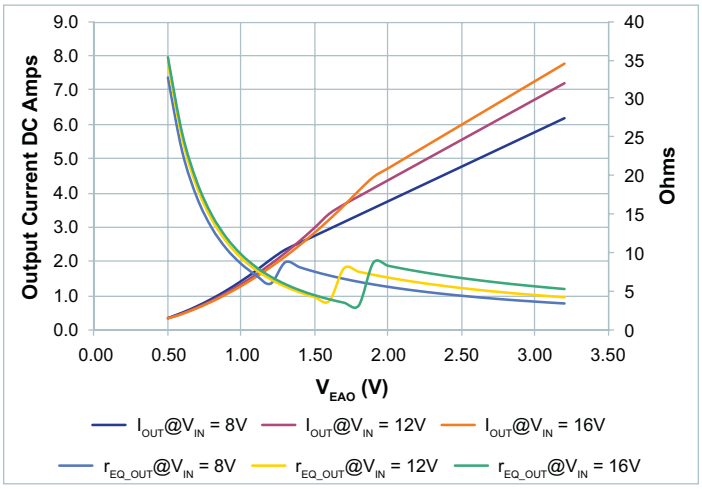


Figure 66 — *r_{EQ_OUT} vs. output current vs. V_{EAO}, V_{OUT} = 10V; 8 – 16V_{IN}*

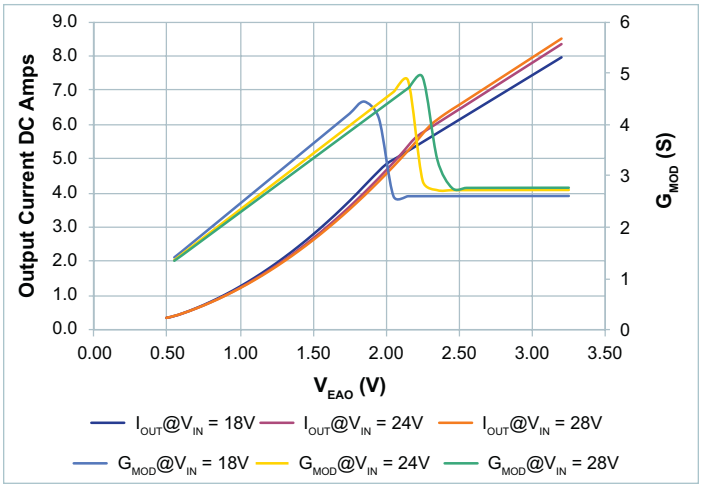


Figure 64 — *G_{MOD} vs output current vs. V_{EAO}, V_{OUT} = 10V; 18 – 28V_{IN}*

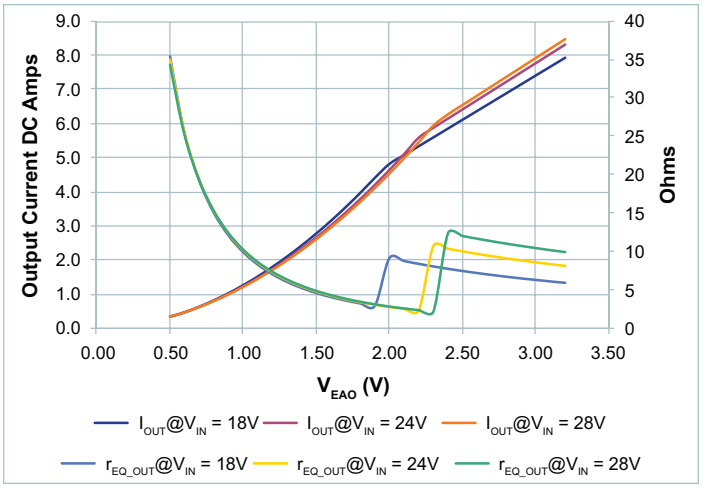


Figure 67 — *r_{EQ_OUT} vs. Output Current vs. V_{EAO}, V_{OUT} = 10V; 18 – 28V_{IN}*

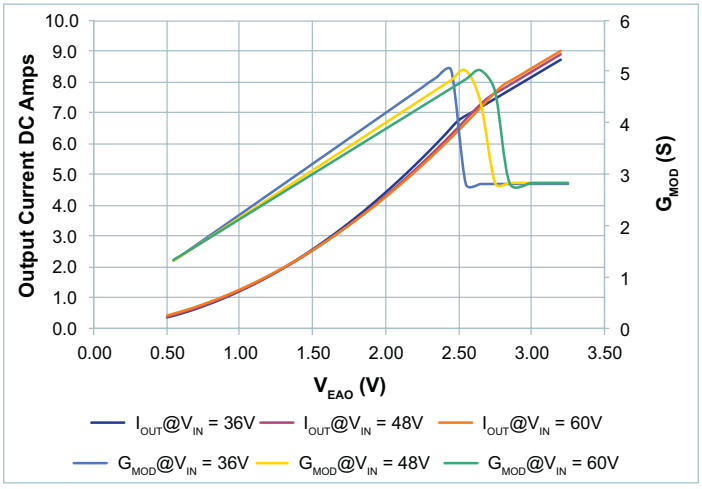


Figure 65 — *G_{MOD} vs output current vs. V_{EAO}, V_{OUT} = 10V; 36 – 60V_{IN}*

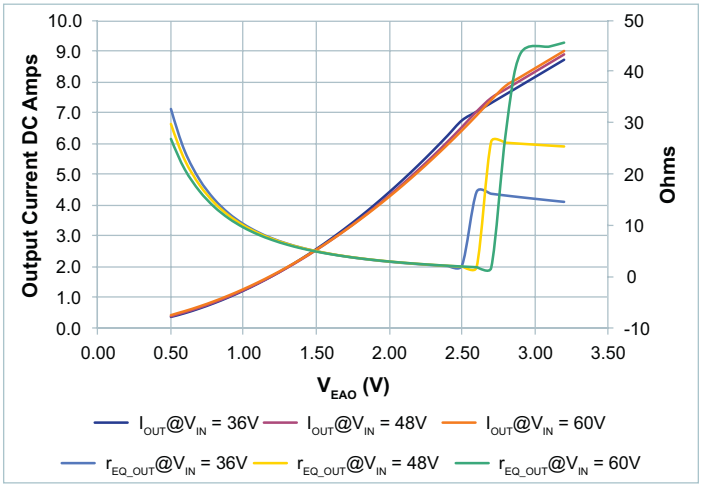


Figure 68 — *r_{EQ_OUT} vs. output current vs. V_{EAO}, V_{OUT} = 10V; 36 – 60V_{IN}*

PI3740-00 Modulator Gain / Output Resistance T_{PCB} = 25°C (Cont.)

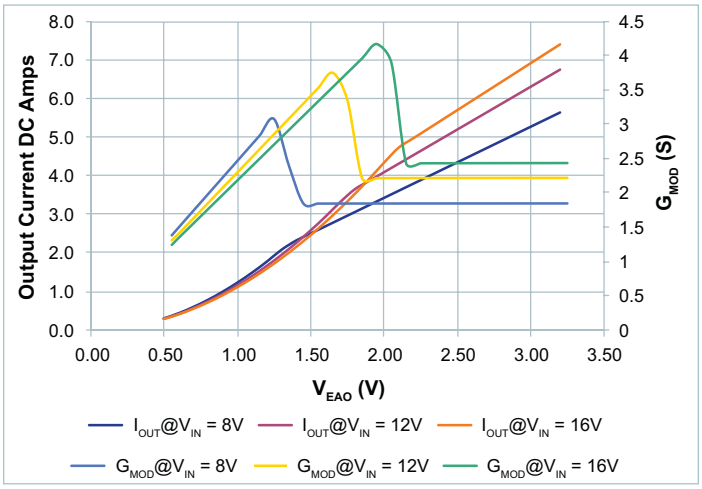


Figure 69 — *G_{MOD} vs output current vs. V_{EAO}, V_{OUT} = 12V; 8 – 16V_{IN}*

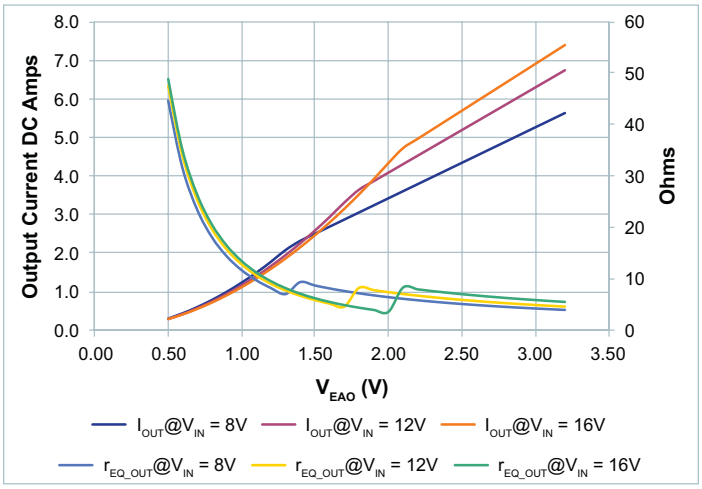


Figure 72 — *r_{EQ_OUT} vs. output current vs. V_{EAO}, V_{OUT} = 12V; 8 – 16V_{IN}*

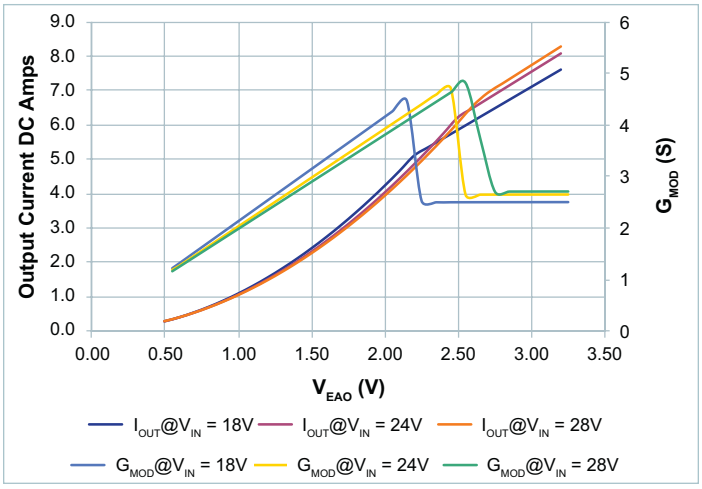


Figure 70 — *G_{MOD} vs output current vs. V_{EAO}, V_{OUT} = 12V; 18 – 28V_{IN}*

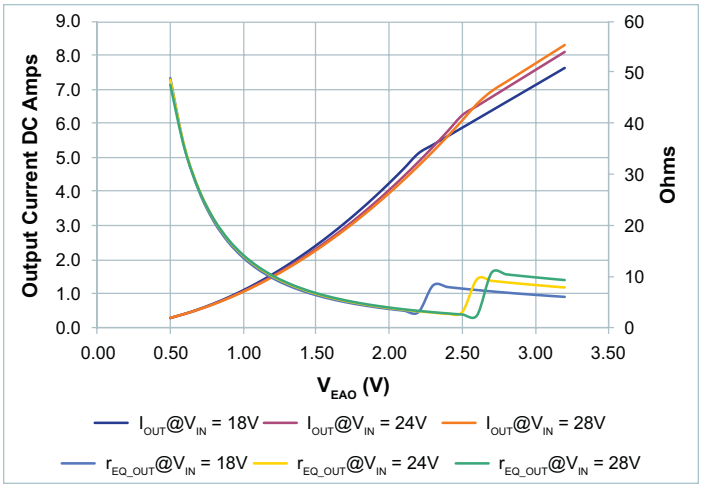


Figure 73 — *r_{EQ_OUT} vs. output current vs. V_{EAO}, V_{OUT} = 12V; 18 – 28V_{IN}*

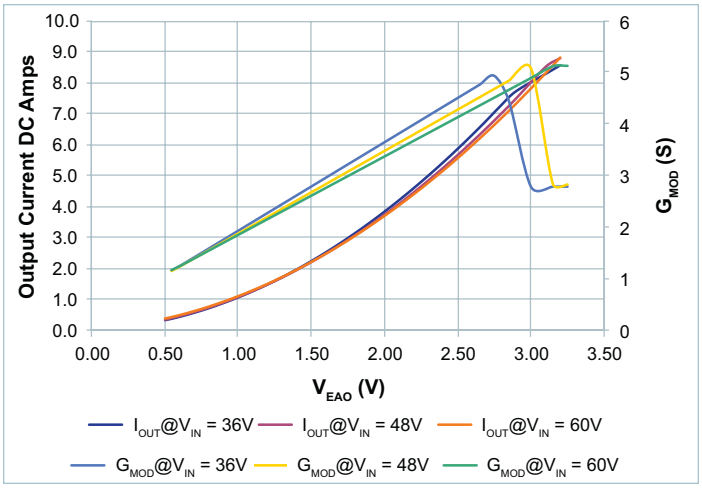


Figure 71 — *G_{MOD} vs output current vs. V_{EAO}, V_{OUT} = 12V; 36 – 60V_{IN}*

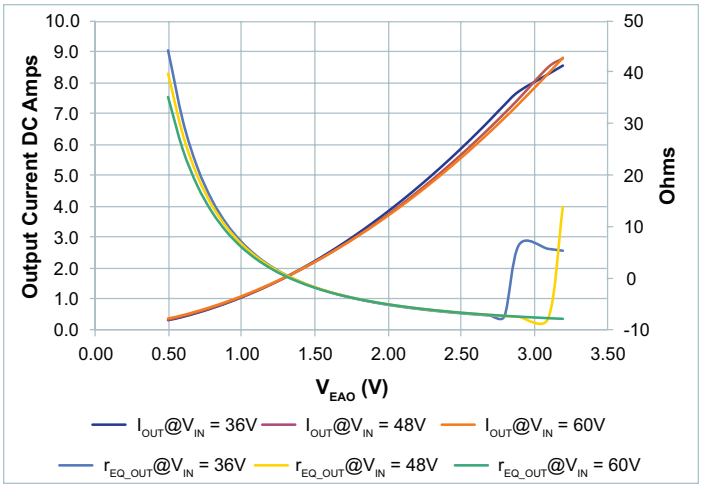


Figure 74 — *r_{EQ_OUT} vs. output current vs. V_{EAO}, V_{OUT} = 12V; 36 – 60V_{IN}*

PI3740-00 Modulator Gain / Output Resistance T_{PCB} = 25°C (Cont.)

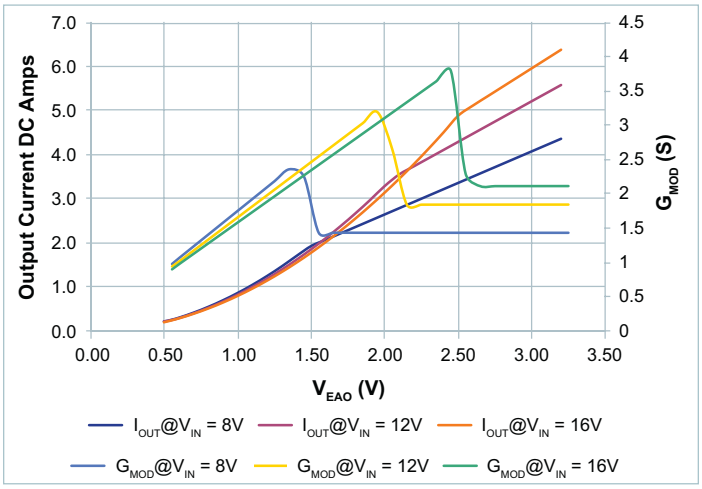


Figure 75 — *G_{MOD} vs output current vs. V_{EAO}, V_{OUT} = 18V 8 – 16V_{IN}*

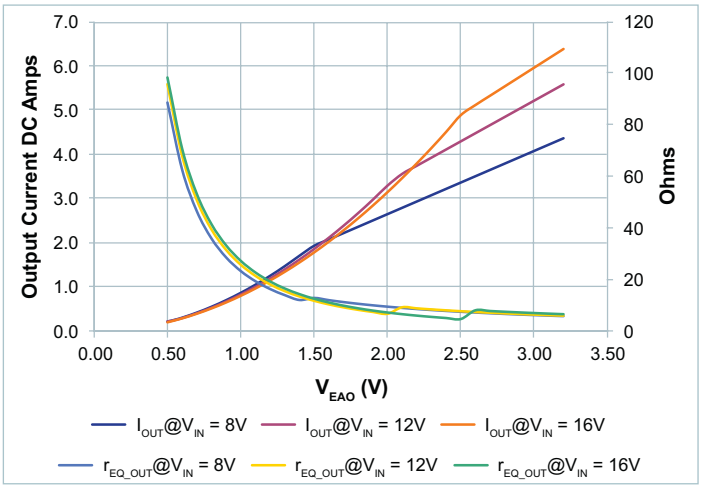


Figure 78 — *r_{EQ_OUT} vs. output current vs. V_{EAO}, V_{OUT} = 18V; 8 – 16V_{IN}*

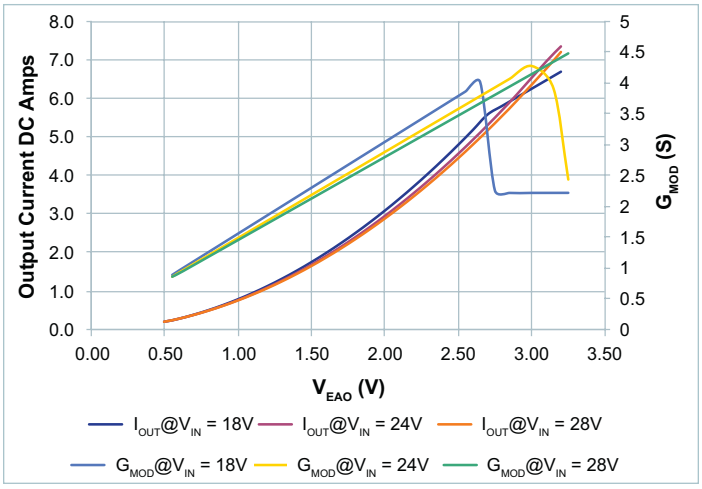


Figure 76 — *G_{MOD} vs output current vs. V_{EAO}, V_{OUT} = 18V; 18 – 28V_{IN}*

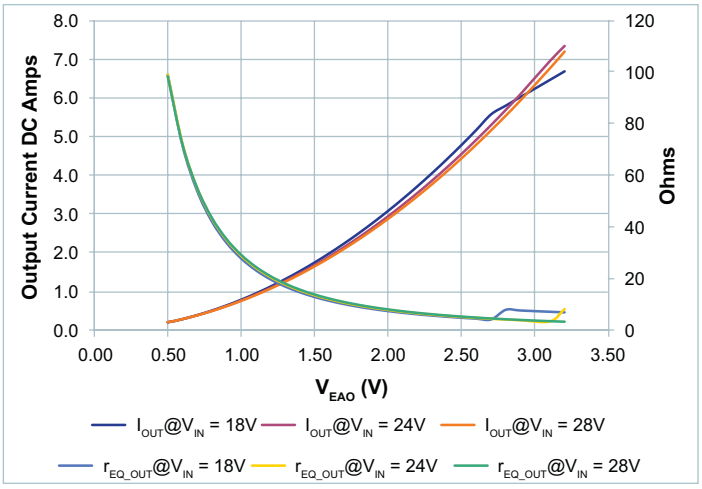


Figure 79 — *r_{EQ_OUT} vs. output current vs. V_{EAO}, V_{OUT} = 18V; 18 – 28V_{IN}*

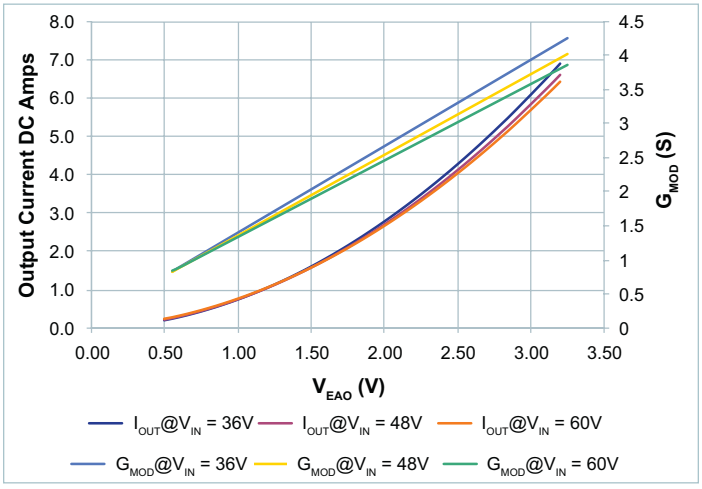


Figure 77 — *G_{MOD} vs output current vs. V_{EAO}, V_{OUT} = 18V; 36 – 60V_{IN}*

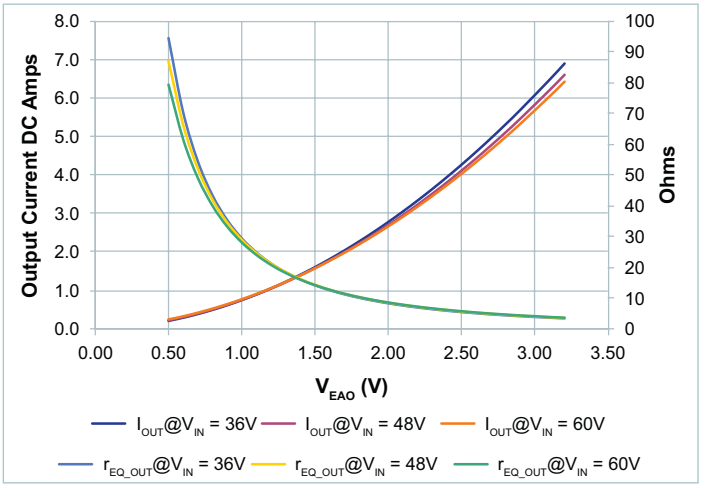


Figure 80 — *r_{EQ_OUT} vs. output current vs.V_{EAO}, V_{OUT} = 18V; 36 – 60V_{IN}*

PI3740-00 Modulator Gain / Output Resistance T_{PCB} = 25°C (Cont.)

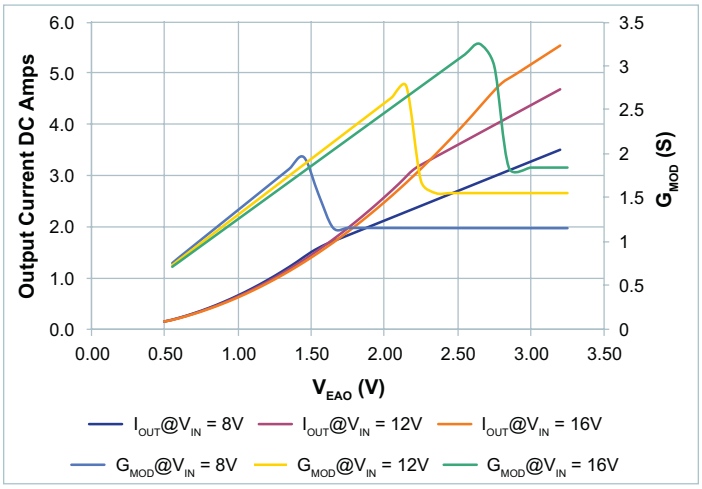


Figure 81 — *G_{MOD} vs output current vs. V_{EAO}, V_{OUT} = 24V; 8 – 16V_{IN}*

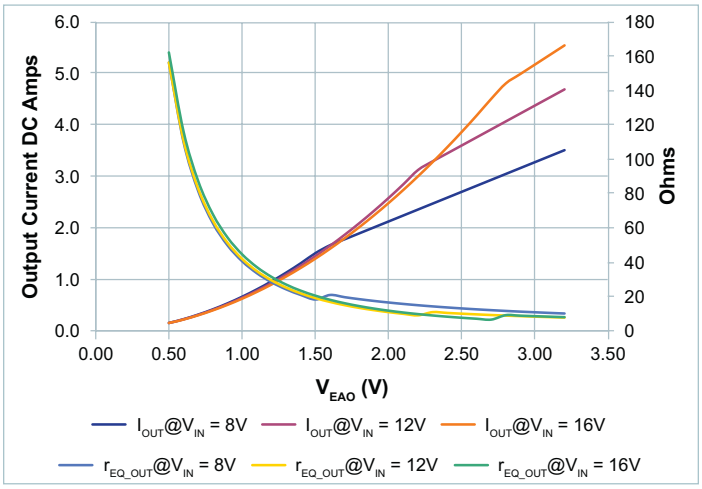


Figure 84 — *r_{EQ_OUT} vs. output current vs. V_{EAO}, V_{OUT} = 24V; 8 – 16V_{IN}*

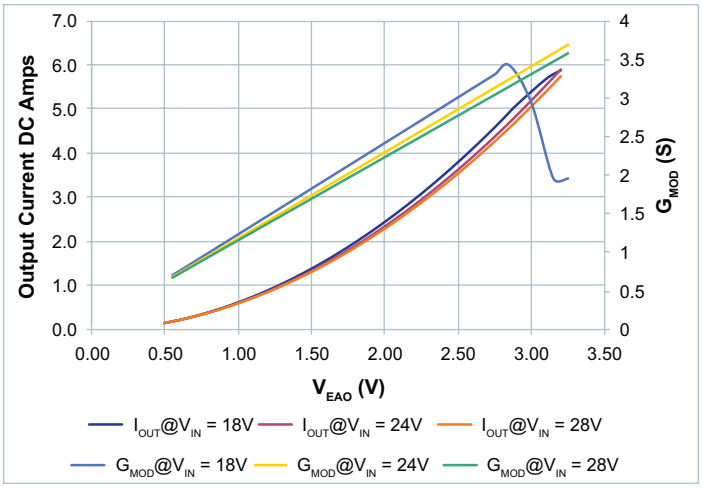


Figure 82 — *G_{MOD} vs output current vs. V_{EAO}, V_{OUT} = 24V; 18 – 28V_{IN}*

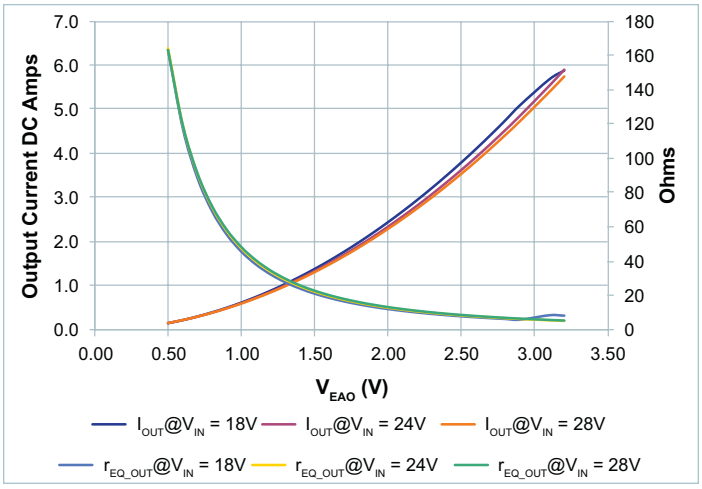


Figure 85 — *r_{EQ_OUT} vs. output current vs. V_{EAO}, V_{OUT} = 24V; 18 – 28V_{IN}*

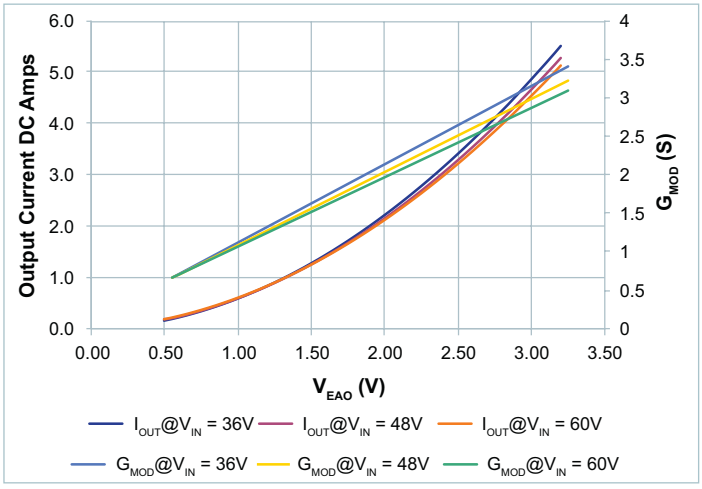


Figure 83 — *G_{MOD} vs output current vs. V_{EAO}, V_{OUT} = 24V; 36 – 60V_{IN}*

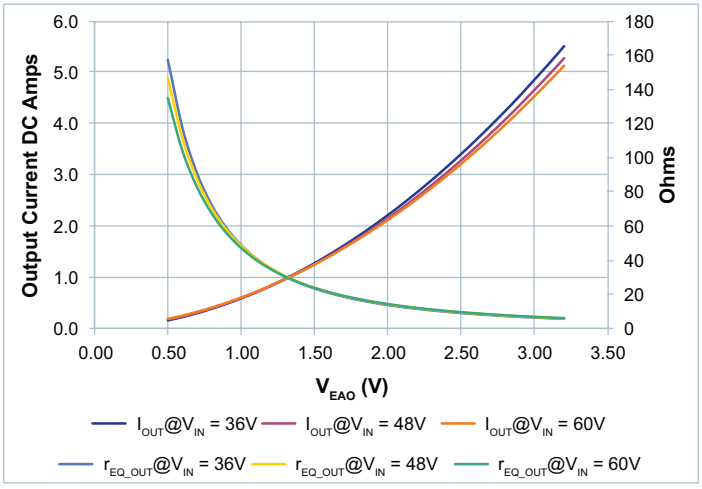


Figure 86 — *r_{EQ_OUT} vs. output current vs. V_{EAO}, V_{OUT} = 24V; 36 – 60V_{IN}*

PI3740-00 Modulator Gain / Output Resistance T_{PCB} = 25°C (Cont.)

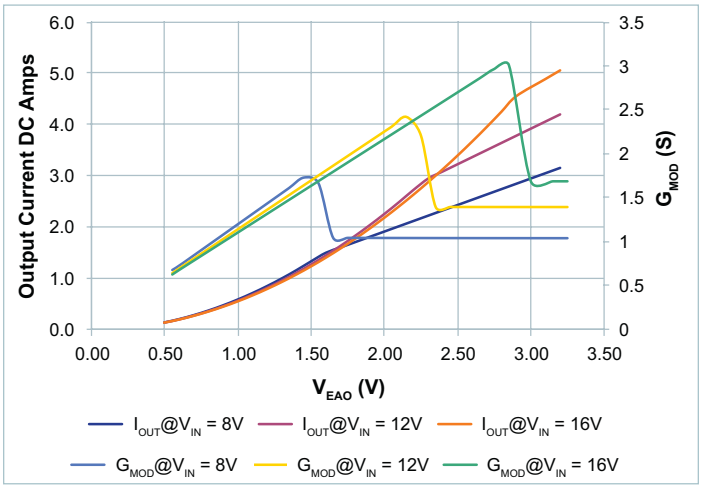


Figure 87 — *G_{MOD} vs output current vs. V_{EAO}, V_{OUT} = 28V; 8 – 16V_{IN}*

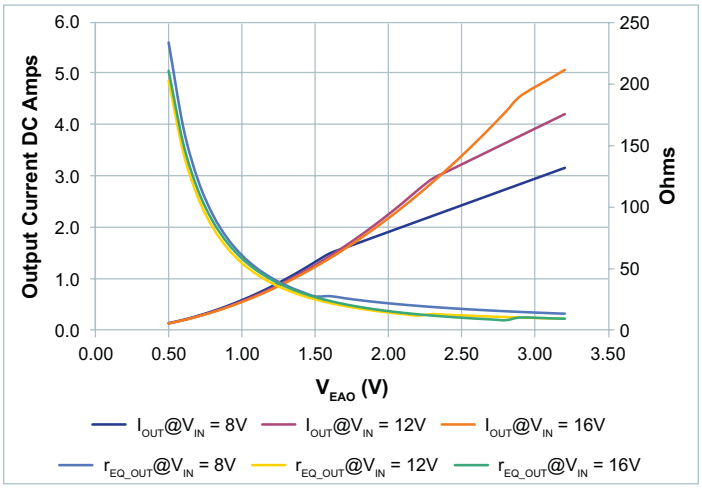


Figure 90 — *r_{EQ_OUT} vs. output current vs. V_{EAO}, V_{OUT} = 28V; 8 – 16V_{IN}*

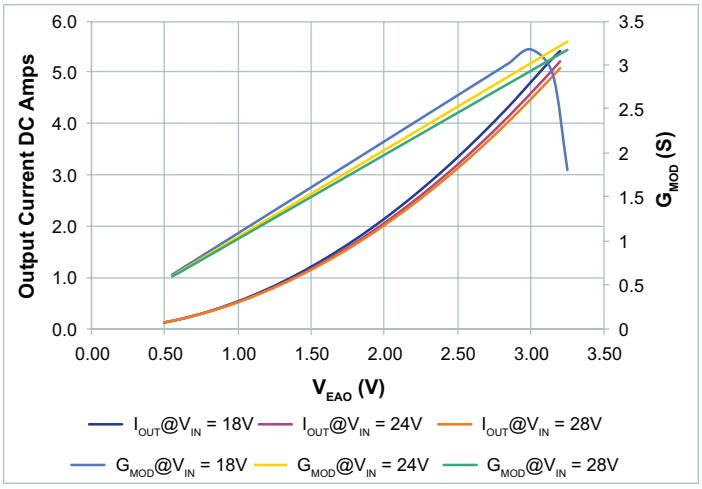


Figure 88 — *G_{MOD} vs output current vs. V_{EAO}, V_{OUT} = 28V; 18 – 28V_{IN}*

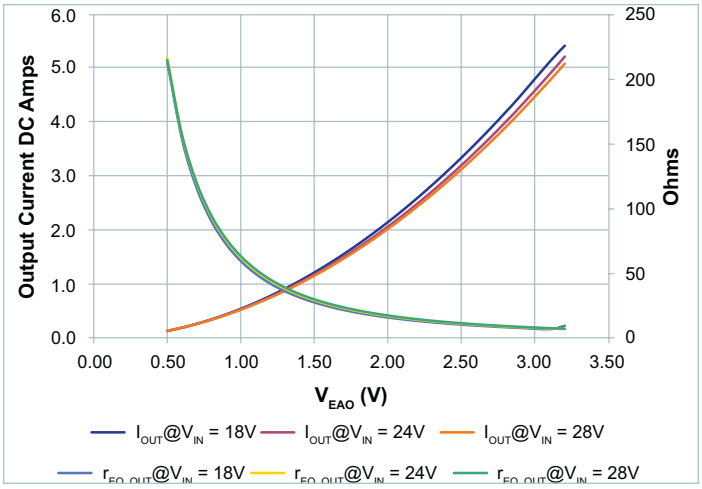


Figure 91 — *r_{EQ_OUT} vs. output current vs. V_{EAO}, V_{OUT} = 28V; 18 – 28V_{IN}*

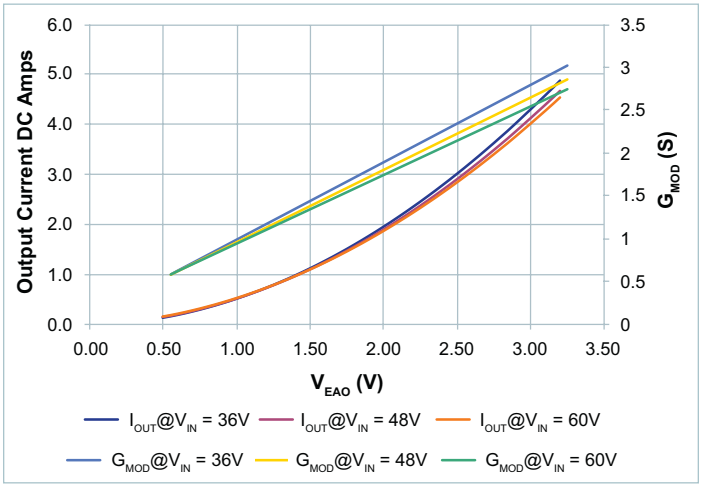


Figure 89 — *G_{MOD} vs output current vs. V_{EAO}, V_{OUT} = 28V; 36 – 60V_{IN}*

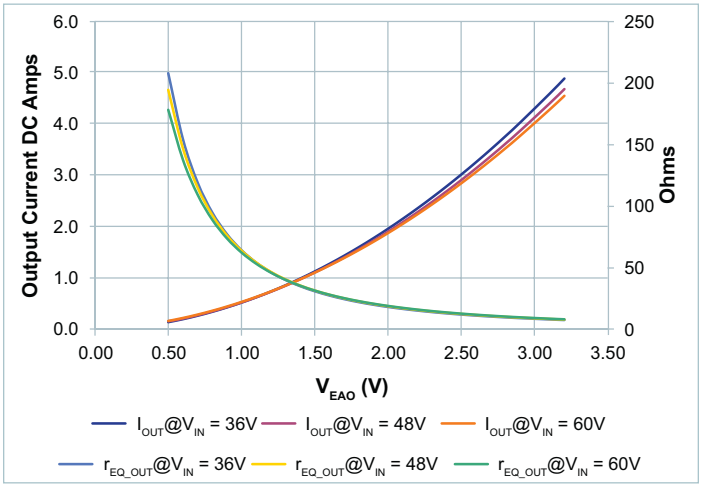


Figure 92 — *r_{EQ_OUT} vs. output current vs. V_{EAO}, V_{OUT} = 28V; 36 – 60V_{IN}*

PI3740-00 Modulator Gain / Output Resistance T_{PCB} = 25°C (Cont.)

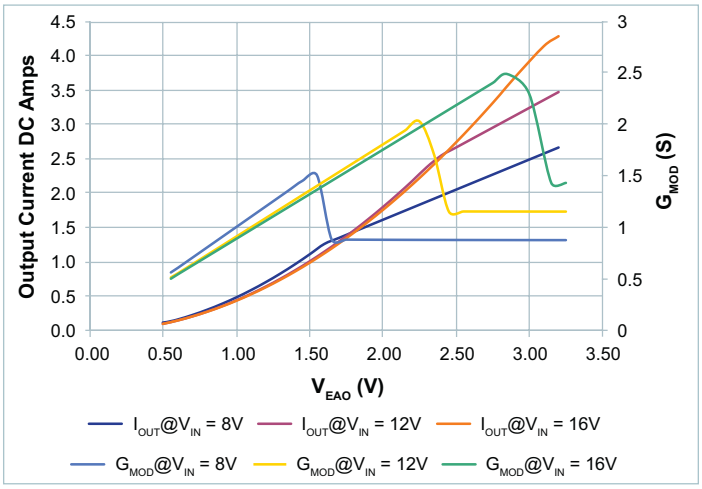


Figure 93 — *G_{MOD} vs output current vs. V_{EAO}, V_{OUT} = 36V; 8 – 16V_{IN}*

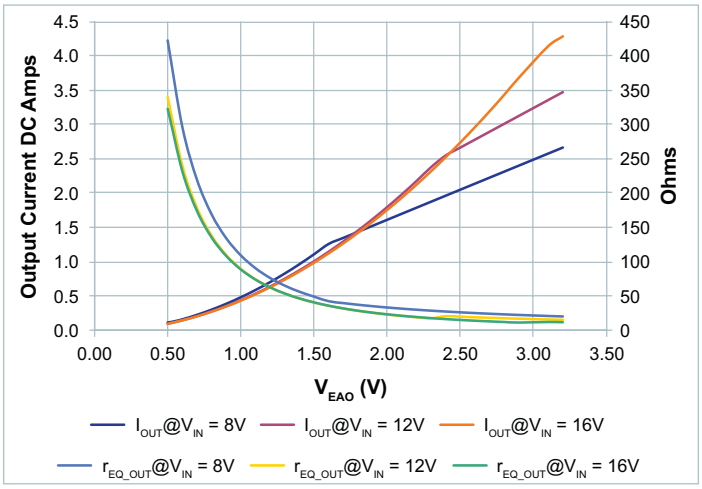


Figure 96 — *r_{EQ_OUT} vs. output current vs. V_{EAO}, V_{OUT} = 36V; 8 – 16V_{IN}*

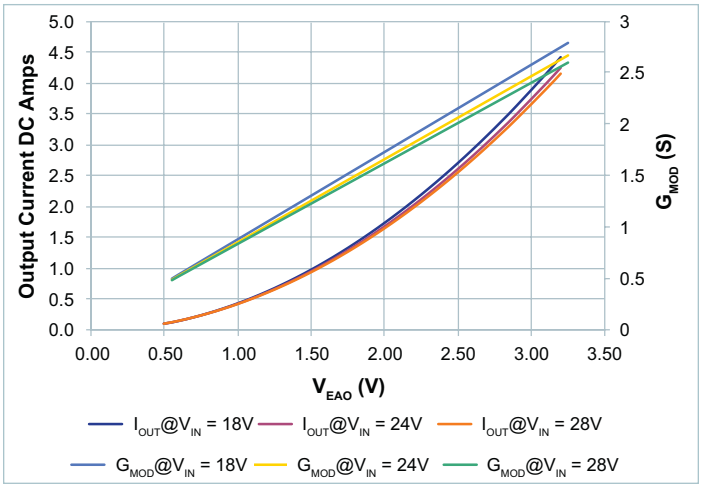


Figure 94 — *G_{MOD} vs output current vs. V_{EAO}, V_{OUT} = 36V; 18 – 28V_{IN}*

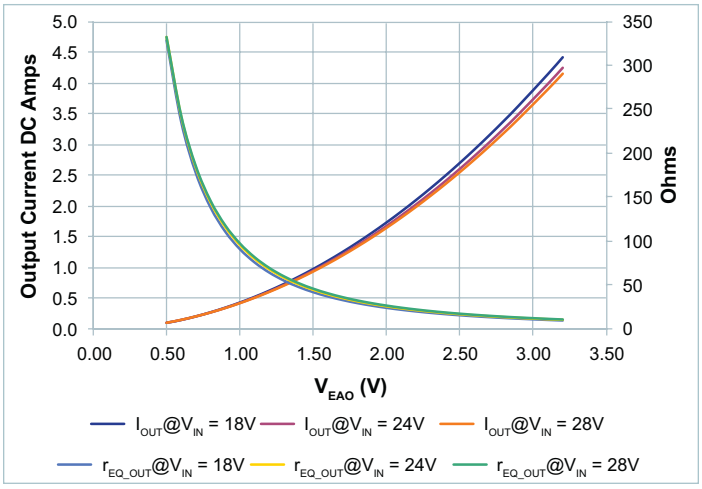


Figure 97 — *r_{EQ_OUT} vs. output current vs. V_{EAO}, V_{OUT} = 36V; 18 – 28V_{IN}*

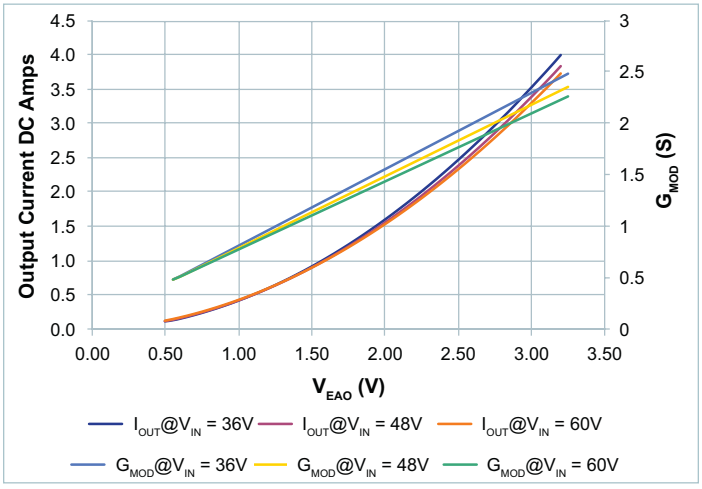


Figure 95 — *G_{MOD} vs output current vs. V_{EAO}, V_{OUT} = 36V; 36 – 60V_{IN}*

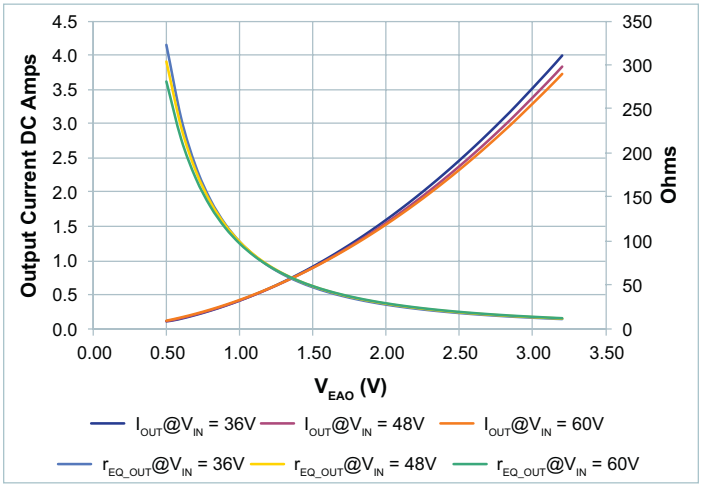


Figure 98 — *r_{EQ_OUT} vs. output current vs. V_{EAO}, V_{OUT} = 36V; 36 – 60V_{IN}*

PI3740-00 Modulator Gain / Output Resistance T_{PCB} = 25°C (Cont.)

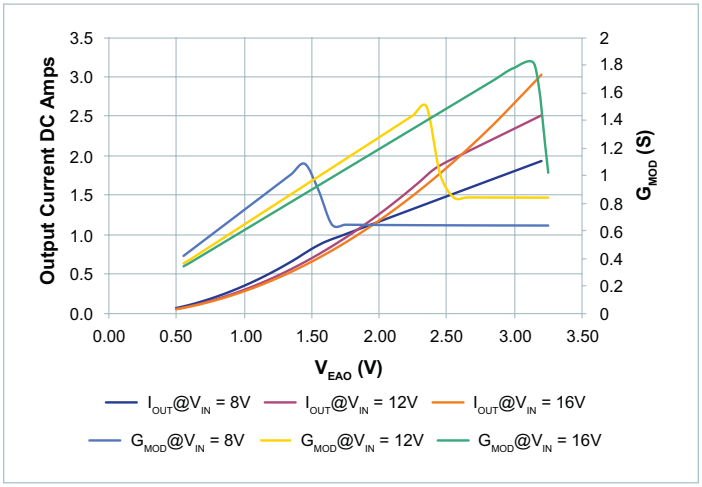


Figure 99 — *G_{MOD} vs output current vs. V_{EAO}, V_{OUT} = 50V; 8 – 16V_{IN}*

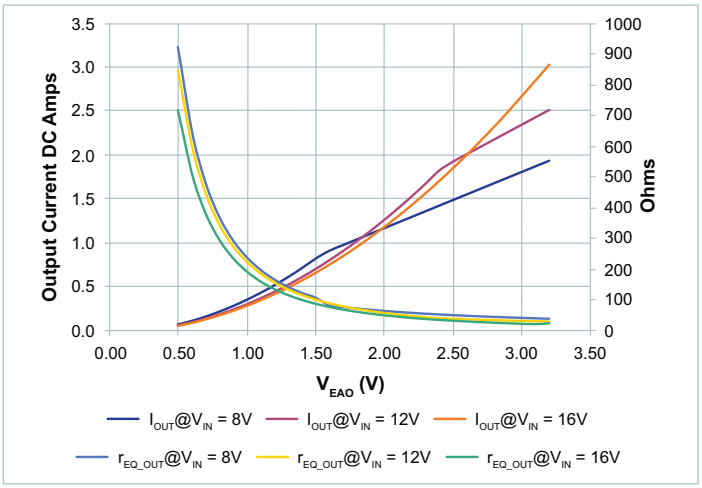


Figure 102 — *r_{EQ_OUT} vs. output current vs. V_{EAO}, V_{OUT} = 50V; 8 – 16V_{IN}*

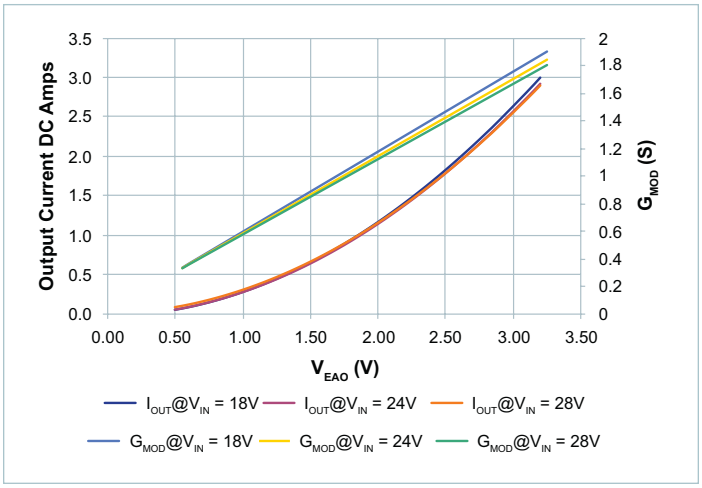


Figure 100 — *G_{MOD} vs output current vs. V_{EAO}, V_{OUT} = 50V; 18 – 28V_{IN}*

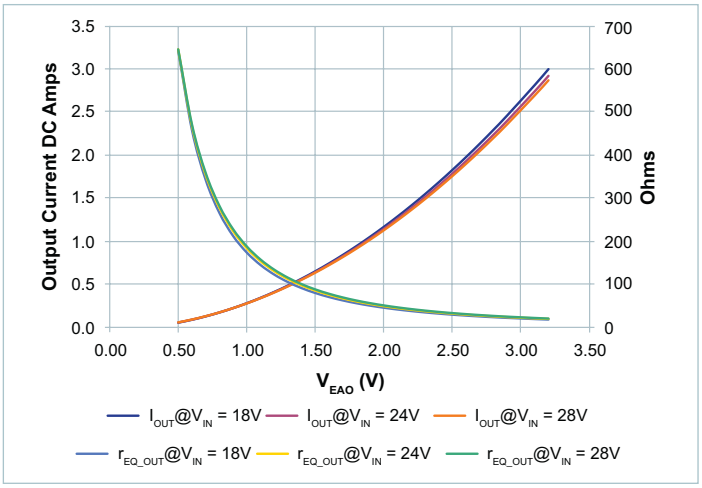


Figure 103 — *r_{EQ_OUT} vs. output current vs. V_{EAO}, V_{OUT} = 50V; 18 – 28V_{IN}*

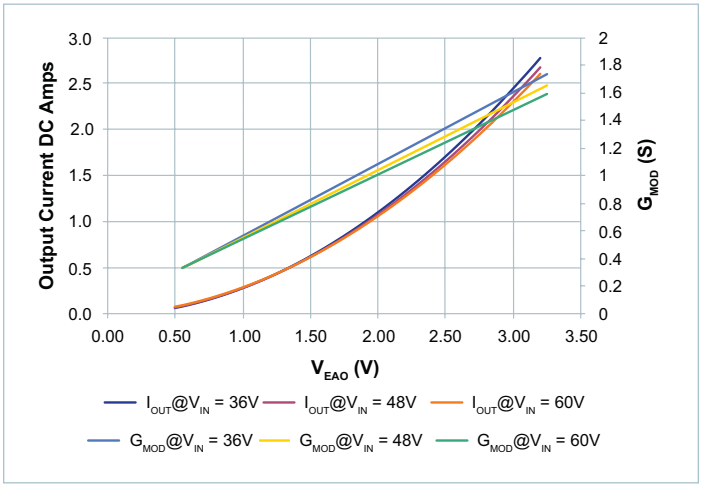


Figure 101 — *G_{MOD} vs output current vs. V_{EAO}, V_{OUT} = 50V; 36 – 60V_{IN}*

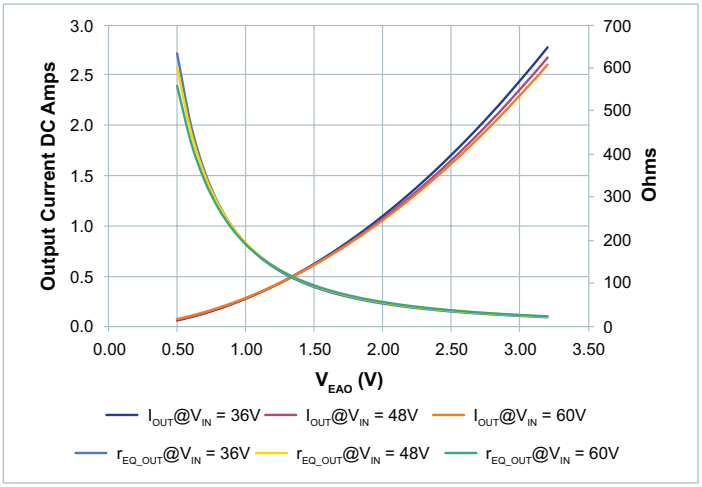


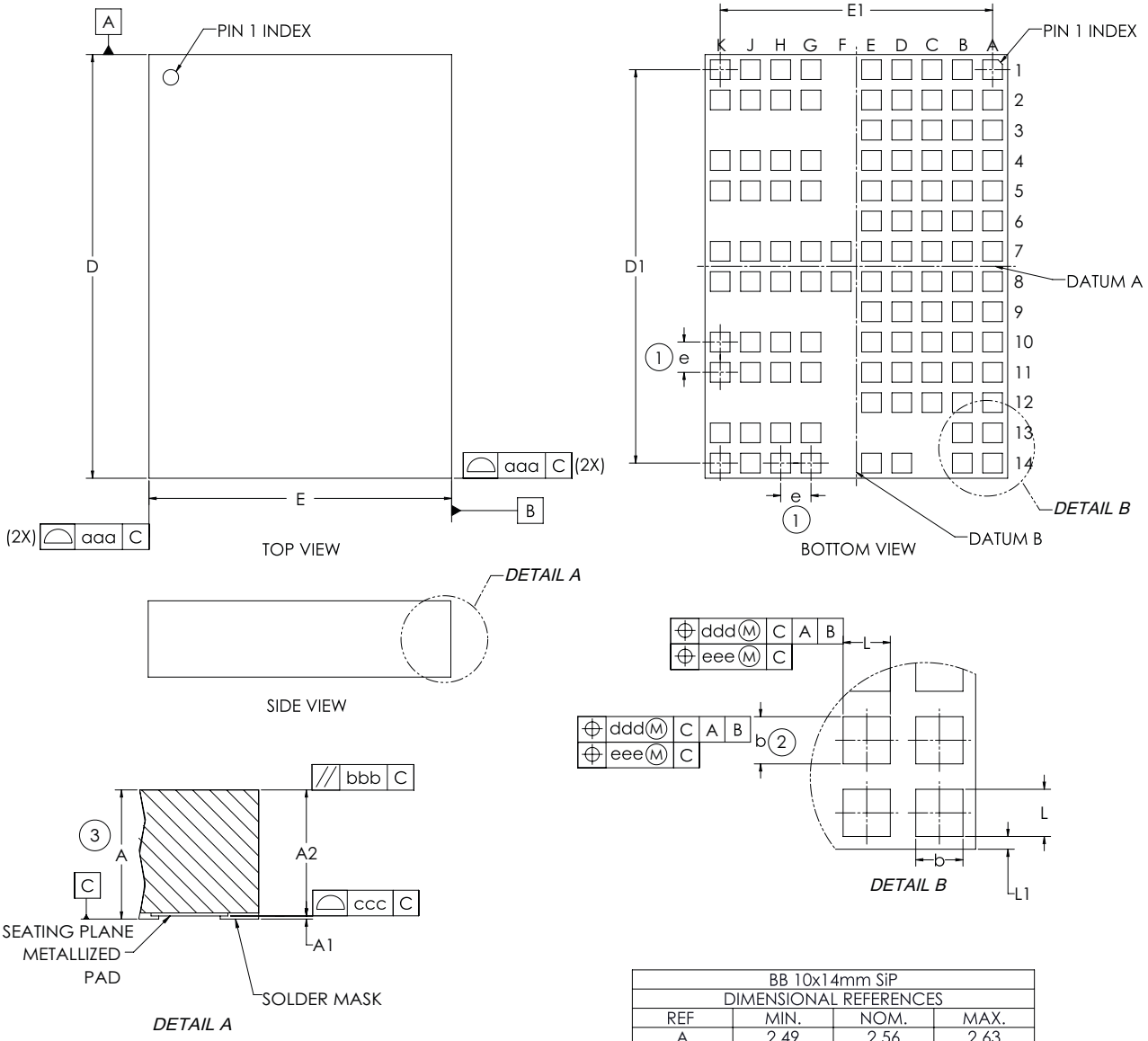
Figure 104 — *r_{EQ_OUT} vs. output current vs. V_{EAO}, V_{OUT} = 50V; 36 – 60V_{IN}*

System Design Considerations

Inductive Loads: As with all power electronic applications, consideration must be given to driving inductive loads that may be exposed to a fault in the system which could result in consequences beyond the scope of the power supply primary protection mechanisms. An inductive load could be a filter, fan motor or even excessively long cables. Consider an instantaneous short circuit through an un-damped inductance that occurs when the output capacitors are already at an initial condition of fully charged. The only thing that limits the current is the inductance of the short circuit and any series resistance. Even if the power supply is off at the time of the short circuit, the current could ramp up in the external inductor and store considerable energy. The release of this energy will result in considerable ringing, with the possibility of ringing nodes connected to the output voltage below ground. The system designer should plan for this by considering the use of other external circuit protection such as load switches, fuses, and transient voltage protectors. The inductive filters should be critically damped to avoid excessive ringing or damaging voltages. Adding a high current Schottky diode from the output voltage to PGND close to the PI3740-00 is recommended for these applications.

Low Voltage Operation: There is no isolation from an SELV (Safety-Extra-Low-Voltage) power system. Powering low voltage loads from input voltages as high as 60V may require additional consideration to protect low voltage circuits from excessive voltage in the event of a short circuit from input to output. A fast TVS (transient voltage suppressor) gating an external load switch is an example of such protection.

LGA Package Drawings

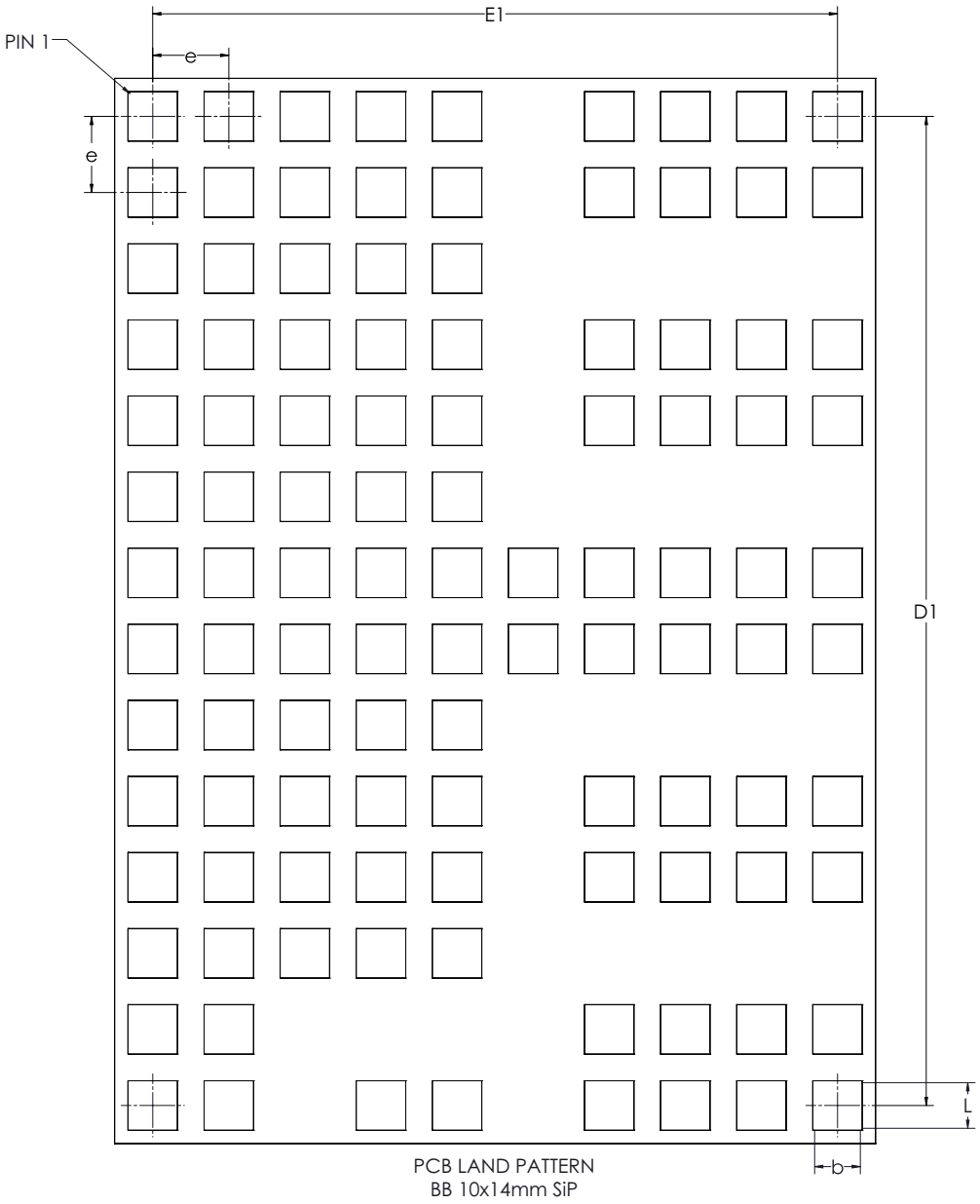


BB 10x14mm SiP DIMENSIONAL REFERENCES	
REF.	TOLERANCE OF FORM AND POSITION
aaa	0.10
bbb	0.10
ccc	0.08
ddd	0.10
eee	0.08

BB 10x14mm SiP DIMENSIONAL REFERENCES			
REF	MIN.	NOM.	MAX.
A	2.49	2.56	2.63
A1	--	--	0.04
A2	--	--	2.59
b	0.50	0.55	0.60
L	0.50	0.55	0.60
D		14.00 BSC	
E		10.00 BSC	
D1		13.00 BSC	
E1		9.00 BSC	
e		1.00 BSC	
L1	.175	0.225	.275

NOTES:
1. 'e' REPRESENTS THE BASIC TERMINAL PITCH. SPECIFIES THE GEOMETRIC POSITION OF THE TERMINAL AXIS.
2. DIMENSION 'b' APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.00mm AND 0.25mm FROM TERMINAL TIP.
3. DIMENSION 'A' INCLUDES PACKAGE WARPAGE.
4. EXPOSED METALLIZED PADS ARE CU PADS WITH SURFACE FINISH PROTECTION.
5. ALL DIMENSIONS ARE IN MM UNLESS OTHERWISE SPECIFIED.
6. RoHS COMPLIANT PER CST-0001LATEST REVISION.

LGA Receiving PCB Pattern Design Recommendations



PCB LAND PATTERN
BB 10x14mm SiP

DIMENSIONAL REFERENCES			
REF.	MIN.	NOM.	MAX.
b	0.50	0.55	0.60
D1	13.00 BSC		
E1	9.00 BSC		
e	1.00 BSC		
L	0.50	0.55	0.60

Recommended receiving footprint for PI3740-00 10 x 14mm package. All pads should have a final copper size of 0.55 x 0.55mm, whether they are solder-mask defined or copper defined, on a 1 x 1mm grid. All stencil openings are 0.45mm when using either a 5 or 6mil stencil.

Revision History

Revision	Date	Description	Page Number(s)
1.0	02/10/17	Initial Release	n/a
1.1	02/27/17	Current Sense Amplifier clarifications	8
1.2	03/10/17	Miscellaneous typo corrections	7
1.3	03/31/17	Correct LGH pin name Include additional PCB Pattern information	5 46
1.4	04/27/17	Correct Absolute Min rating for V_{IN}	3
1.5	06/05/17	Update IMON Output voltage specification	8
1.6	06/16/17	Add Maximum C_{OUT} Capability at Startup section Correct Percentage of SiP Loss to Total Loss 50V_{OUT} figure Parallel Operation update	26 32 34
1.7	08/12/17	Update diagrams to show signal ground	1, 20, 35 – 37
1.8	08/24/17	Updated thermal impedance tables and thermal design inductor	28 – 30
1.9	06/15/18	Updated LGA package drawings Added BGA package information	46, 47 48, 49
2.0	10/12/18	Updated UVLO threshold rising min, OVLO hysteresis, overvoltage threshold, current sense amplifier IMON output at no load and transconductance error amplifier reference min/max	7, 8, 9
2.1	11/05/18	Updated V_{IN} OVLO threshold rising max spec	7
2.2	11/19/18	Updated V_{OUT} overvoltage threshold min spec	7
2.3	02/04/20	Added extended-temperature and lead solder ball options	1, 3, 6 – 10
2.4	05/15/20	Updated to add recommended Pulse Electronics inductor	22
2.5	08/12/20	Updated terminology	22
2.6	02/22/21	Updated to include PI3040-00-LGMZ part number	1, 3, 6, 7, 8, 9, 10
2.7	05/06/21	Removed BGA package option	1, 2, 3, 6, 7– 10
2.8	10/04/21	Revised inductor pairing information	22
2.9	03/11/24	Corrected note/page references	7, 8, 9, 10

Please note: Pages added in Rev 1.6 and 1.9; pages removed in Rev 2.7.

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