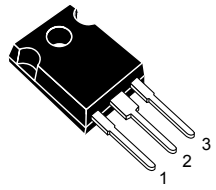
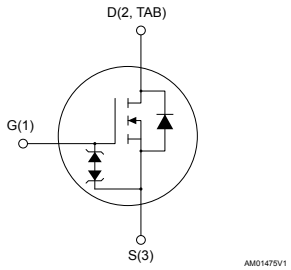
# N-channel 1700 V, 2.3 Ω typ., 5 A, MDmesh™ K5 Power MOSFET in a TO-247 package




TO-247




## Features

| Order code | $V_{DS}$ | $R_{DS(on)}$ max. | $I_D$ | $P_{TOT}$ |
|---|---|---|---|---|
| STW12N170K5 | 1700 V | 2.9 Ω | 5 A | 250 W |

- Industry's lowest $R_{DS(on)}$ x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

## Applications

- Switching applications

## Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

| Product status link |
|---|
| STW12N170K5 |

| Product summary | |
|---|---|
| **Order code** | STW12N170K5 |
| **Marking** | 12N170K5 |
| **Package** | TO-247 |
| **Packing** | Tube |

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{GS}$ | Gate-source voltage | ±30 | V |
| $I_D$ | Drain current at $T_C$ = 25 °C | 5 | A |
| | Drain current at $T_C$ = 100 °C | 3 | A |
| $I_{DM}$(1) | Drain current (pulsed) | 10 | A |
| $P_{TOT}$ | Total power dissipation at $T_C$ = 25 °C | 250 | W |
| dv/dt(2) | Peak diode recovery voltage slope | 4.5 | V/ns |
| dv/dt(3) | MOSFET dv/dt ruggedness | 50 | V/ns |
| $T_J$ | Operating junction temperature range | -55 to 150 | °C |
| $T_{stg}$ | Storage temperature range | | |

1. *Pulse width limited by safe operating area*
2. *$I_{SD}$ ≤ 5 A, di/dt ≤ 100 A/µs, $V_{DS(peak)}$ ≤ $V_{(BR)DSS}$*
3. *$V_{DS}$ ≤ 1360 V*

**Table 2. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thj\text{-}case}$ | Thermal resistance junction-case | 0.5 | °C/W |
| $R_{thj\text{-}amb}$ | Thermal resistance junction-amb | 50 | °C/W |

**Table 3. Avalanche characteristics**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $I_{AR}$(1) | Maximum current during repetitive or single pulse avalanche | 1.7 | A |
| $E_{AS}$(2) | Single pulse avalanche energy | 1000 | mJ |

1. *Pulse width limited by $T_{Jmax}$*
2. *Starting $T_J$ = 25 °C, $I_D$ = $I_{AR}$, $V_{DD}$ = 50 V*

# 2 Electrical characteristics

($T_{CASE}$ = 25 °C unless otherwise specified)

**Table 4. Static**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS}$ = 0 V, $I_D$ = 1 mA | 1700 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current | $V_{GS}$ = 0 V, $V_{DS}$ = 1700 V | | | 1 | µA |
| | | $V_{GS}$ = 0 V, $V_{DS}$ = 1700 V, $T_C$ = 125 °C(1) | | | 50 | µA |
| $I_{GSS}$ | Gate body leakage current | $V_{DS}$ = 0, $V_{GS}$ = ± 20 V | | | ±10 | µA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 100 µA | 3 | 4 | 5 | V |
| $R_{DS(on)}$ | Static drain-source on- resistance | $V_{GS}$ = 10 V, $I_D$ = 2.5 A | | 2.3 | 2.9 | Ω |

1. *Defined by design, not subject to production test.*

**Table 5. Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input capacitance | $V_{GS}$ = 0 V, $V_{DS}$ = 100 V, f = 1 MHz | - | 1380 | - | pF |
| $C_{oss}$ | Output capacitance | | - | 73 | - | pF |
| $C_{rss}$ | Reverse transfer capacitance | | - | 2.7 | - | pF |
| $C_{o(tr)}$(1) | Time-related equivalent capacitance | $V_{DS}$ = 0 V to 1360 V, $V_{GS}$ = 0 V | - | 65 | - | pF |
| $C_{o(er)}$(2) | Energy-related equivalent capacitance | | - | 26 | - | pF |
| $R_G$ | Intrinsic gate resistance | f = 1 MHz, $I_D$ = 0 A | - | 3.8 | - | Ω |
| $Q_g$ | Total gate charge | $V_{DD}$ = 1360 V, $I_D$ = 5 A | - | 37 | - | nC |
| $Q_{gs}$ | Gate-source charge | $V_{GS}$ = 0 to 10 V | - | 10 | - | nC |
| $Q_{gd}$ | Gate-drain charge | (see Figure 15. Test circuit for gate charge behavior) | - | 19 | - | nC |

1. *This parameter is defined as a constant equivalent capacitance giving the same charging time as $C_{OSS}$ when $V_{DS}$ increases from 0 to 80% $V_{DSS}$.*
2. *This parameter is defined as a constant equivalent capacitance giving the same stored energy as $C_{OSS}$ when $V_{DS}$ increases from 0 to 80% $V_{DSS}$.*

**Table 6. Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}$ = 850 V, $I_D$ = 2.5 A, $R_G$ = 4.7 Ω, $V_{GS}$ = 10 V (see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform) | - | 22 | - | ns |
| $t_r$ | Rise time | | - | 7 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | 74 | - | ns |
| $t_f$ | Fall time | | - | 51 | - | ns |

**Table 7. Source drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain current | | - | | 5 | A |
| $I_{SDM}$ | Source-drain current (pulsed) | | - | | 10 | A |
| $V_{SD}$(1) | Forward on voltage | $I_{SD}$ = 5 A, $V_{GS}$ = 0 V | - | | 1.5 | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 5 A, $V_{DD}$ = 60 V, di/dt = 100 A/µs (see Figure 16. Test circuit for inductive load switching and diode recovery times) | - | 350 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 3.91 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 22.3 | | A |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 5 A,$V_{DD}$ = 60 V, di/dt = 100 A/µs, $T_J$ = 150 °C (see Figure 16. Test circuit for inductive load switching and diode recovery times) | - | 481 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 5.07 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 21.0 | | A |

1. *Pulsed: pulse duration = 300µs, duty cycle 1.5%*

**Table 8. Gate-source Zener diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)GSO}$ | Gate-source breakdown voltage | $I_{GS}$ = ±1 mA, $I_D$ = 0 A | 30 | - | | V |

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

## 2.1 Electrical characteristics (curves)

**Figure 1. Safe operating area**

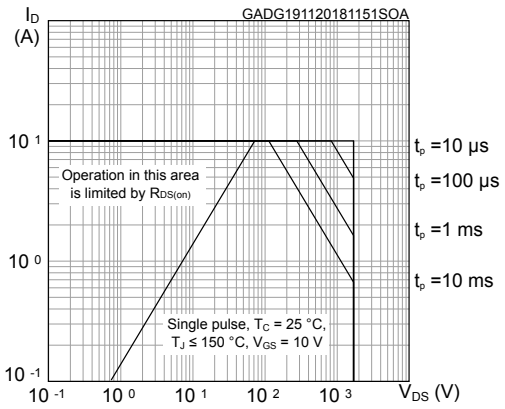



**Figure 2. Thermal impedance**

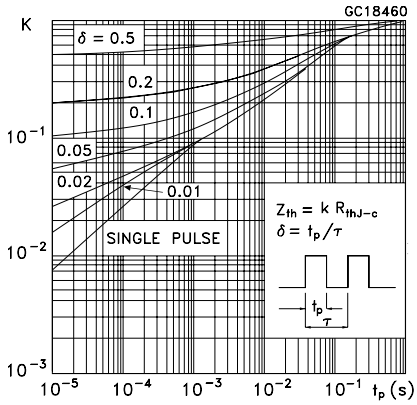



**Figure 3. Output characteristics**

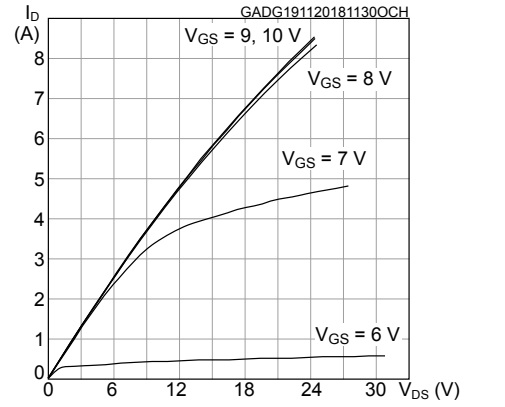



**Figure 4. Transfer characteristics**

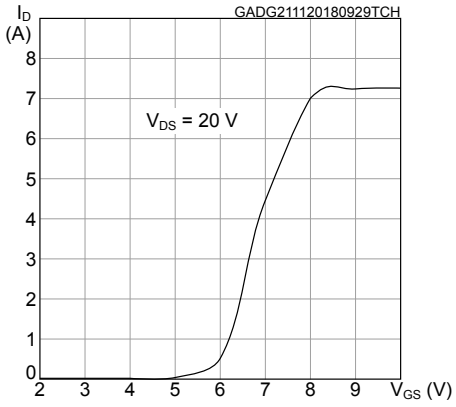



**Figure 5. Gate charge vs gate-source voltage**

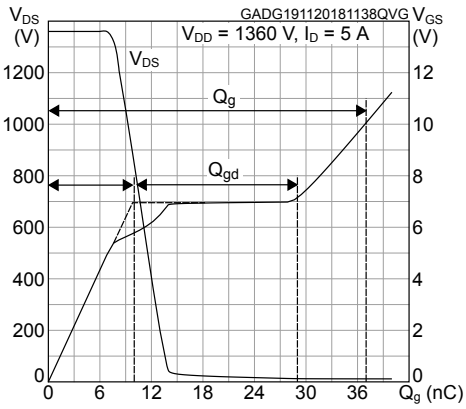



**Figure 6. Static drain-source on-resistance**

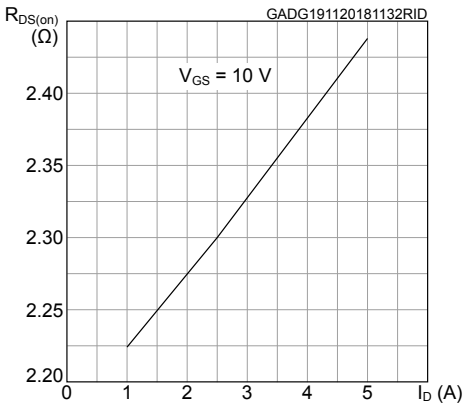


**Figure 7. Normalized gate threshold voltage vs temperature**

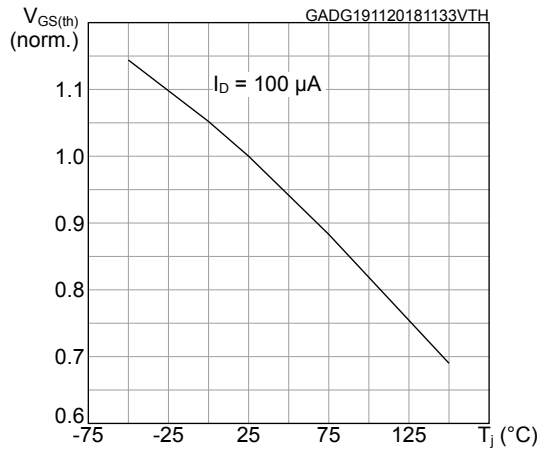



**Figure 8. Normalized on-resistance vs temperature**

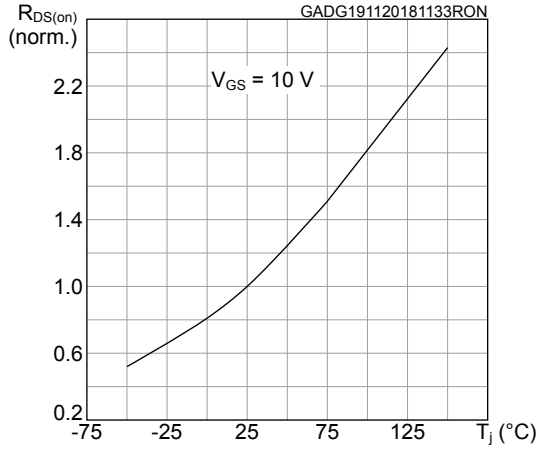



**Figure 9. Normalized $V_{(BR)DSS}$ vs temperature**

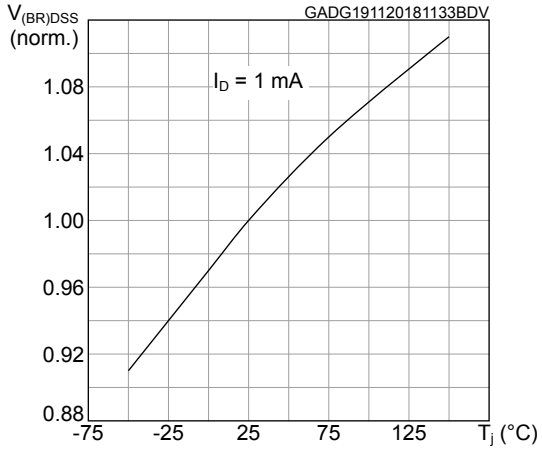



**Figure 10. Source-drain diode forward characteristics**

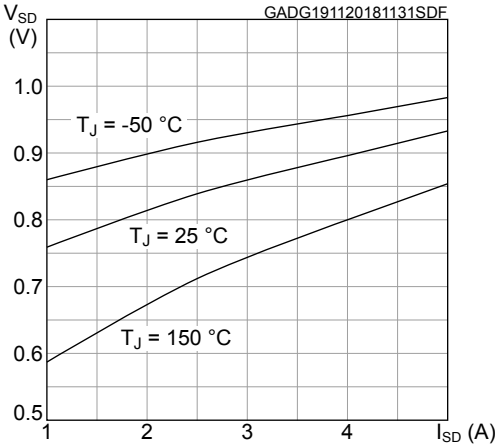



**Figure 11. Capacitance variations**

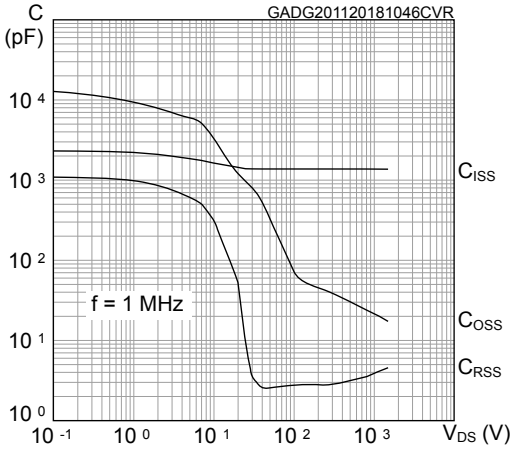



**Figure 12. Maximum avalanche energy vs $T_J$**

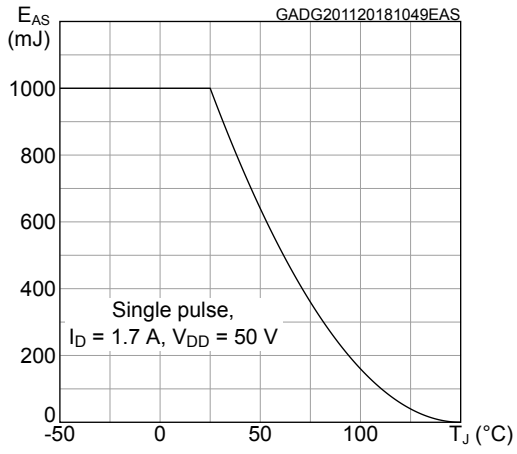
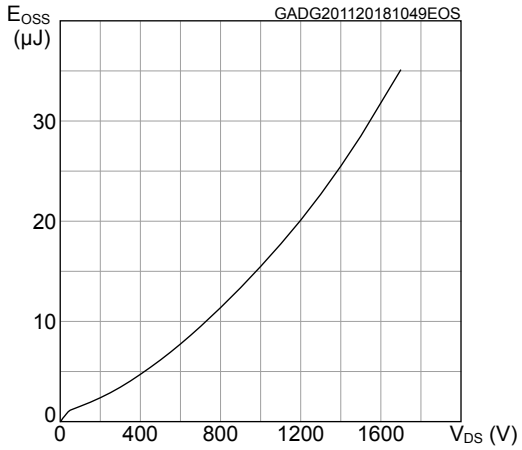


Figure 13. **Output capacitance stored energy**



# 3 Test circuits

**Figure 14. Test circuit for resistive load switching times**

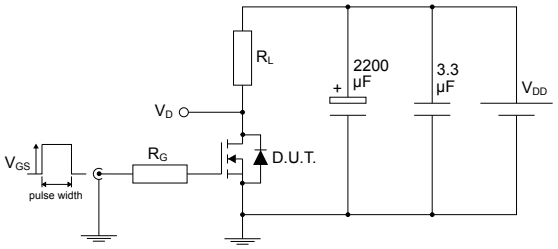



**Figure 15. Test circuit for gate charge behavior**

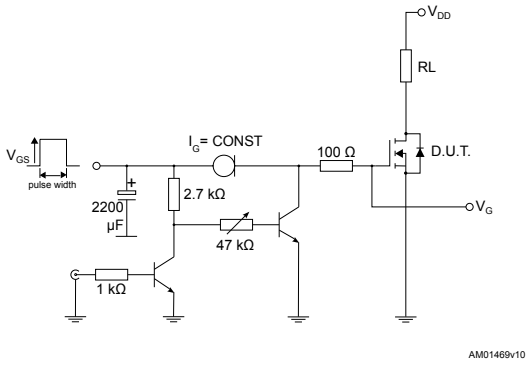



**Figure 16. Test circuit for inductive load switching and diode recovery times**

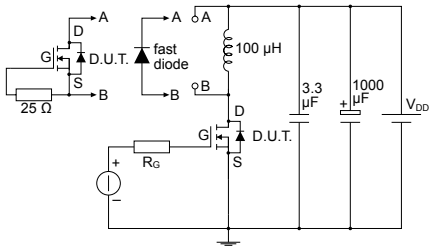



**Figure 17. Unclamped inductive load test circuit**

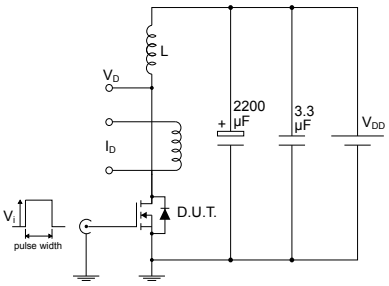



**Figure 18. Unclamped inductive waveform**

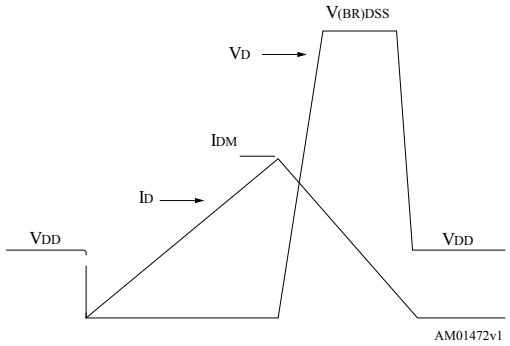
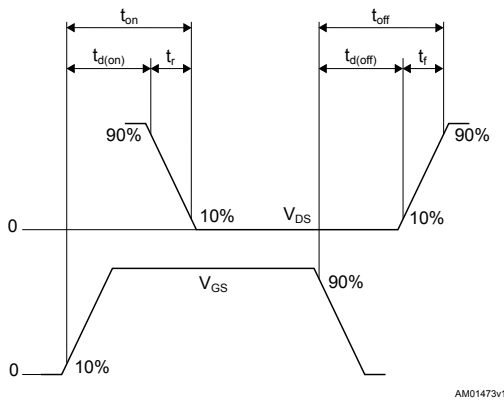



**Figure 19. Switching time waveform**

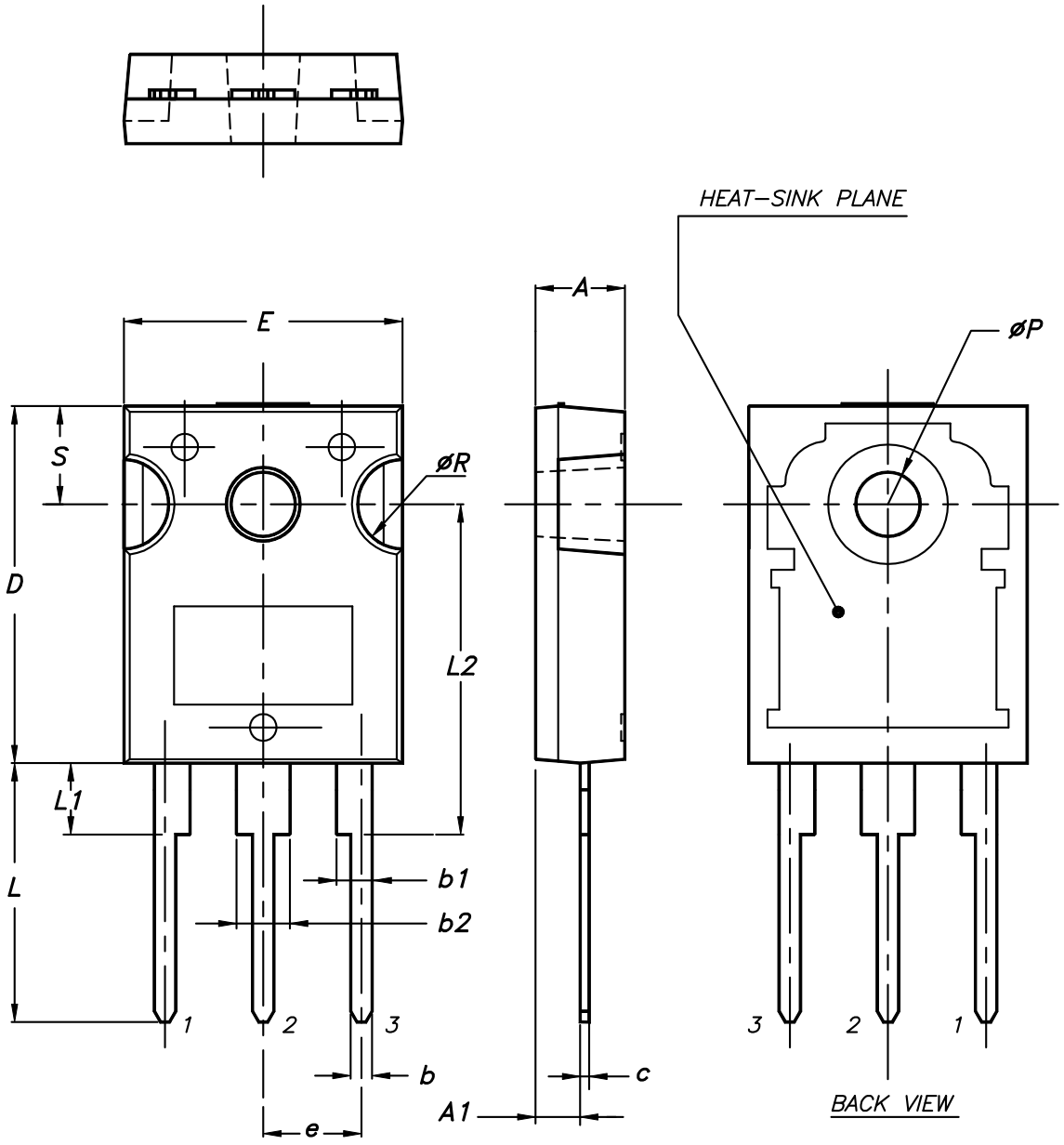


# 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

## 4.1 TO-247 package information

Figure 20. **TO-247 package outline**




0075325_9

Table 9. **TO-247 package mechanical data**

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 4.85 | | 5.15 |
| A1 | 2.20 | | 2.60 |
| b | 1.0 | | 1.40 |
| b1 | 2.0 | | 2.40 |
| b2 | 3.0 | | 3.40 |
| c | 0.40 | | 0.80 |
| D | 19.85 | | 20.15 |
| E | 15.45 | | 15.75 |
| e | 5.30 | 5.45 | 5.60 |
| L | 14.20 | | 14.80 |
| L1 | 3.70 | | 4.30 |
| L2 | | 18.50 | |
| ØP | 3.55 | | 3.65 |
| ØR | 4.50 | | 5.50 |
| S | 5.30 | 5.50 | 5.70 |

## Revision history

Table 10. **Document revision history**

| Date | Version | Changes |
|---|---|---|
| 20-Nov-2018 | 1 | First release. |

# Contents

# Mouser Electronics

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