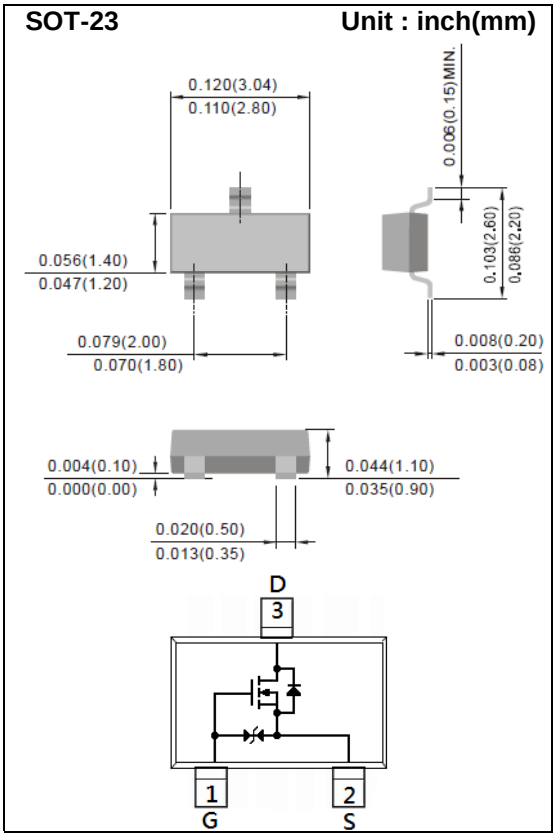
PJA138K-AU

50V N-Channel Enhancement Mode MOSFET – ESD Protected

Voltage	50 V	Current	500mA



Features

- RDS(ON) , V_{GS}@10V, I_D@500mA<1.6Ω
- RDS(ON) , V_{GS}@4.5V, I_D@200mA<2.5Ω
- RDS(ON) , V_{GS}@2.5V, I_D@100mA<4.5Ω
- Advanced Trench Process Technology.
- Specially Designed for Battery Operated Systems, Solid-State Relays Drivers: Relay, Displays, Memories, etc.
- AEC-Q101 qualified.
- ESD Protected 2KV HBM
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case: SOT-23 Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.0003 ounces, 0.0084 grams

Maximum Ratings and Thermal Characteristics (T_A=25°C unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V_{DS}	50	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current		I_D	500	mA
Pulsed Drain Current		I_{DM}	1200	mA
Power Dissipation	T_A=25°C	P_D	500	mW
	Derate above 25°C		4	mW/°C
Operating Junction and Storage Temperature Range		T_J,T_{STG}	-55~150	°C
Typical Thermal Resistance - Junction to Ambient (Note 3)		$R_{\theta JA}$	250	°C/W

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Electrical Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=250uA	50	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250uA	0.8	1.0	1.5	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=500mA	-	0.96	1.6	Ω
		V_{GS}=4.5V,I_D=200mA	-	1.25	2.5	
		V_{GS}=2.5V,I_D=100mA	-	2.73	4.5	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=50V,V_{GS}=0V	-	0.01	1	uA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	±3.0	±10	
Dynamic (Note 4)						
Total Gate Charge	Q_g	V_{DS}=25V, I_D=250mA, V_{GS}=4.5V (Note 1,2)	-	0.63	1	nC
Gate-Source Charge	Q_{gs}		-	0.2	-	
Gate-Drain Charge	Q_{gd}		-	0.23	-	
Input Capacitance	Ciss	V_{DS}=25V, V_{GS}=0V, f=1.0MHZ	-	25	50	pF
Output Capacitance	Coss		-	9.5	20	
Reverse Transfer Capacitance	Crss		-	2.1	5	
Turn-On Delay Time	$td_{(on)}$	V_{DD}=25V, I_D=500mA, V_{GS}=10V, R_G=6Ω (Note 1,2)	-	2.2	5	ns
Turn-On Rise Time	tr		-	19.2	38	
Turn-Off Delay Time	$td_{(off)}$		-	6.2	12	
Turn-Off Fall Time	tf		-	23	50	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I_S	---	-	-	500	mA
Diode Forward Voltage	V_{SD}	I_S=500mA, V_{GS}=0V	-	0.86	1.5	V

NOTES :

1. Pulse width≤300us, Duty cycle≤2%
2. Essentially independent of operating temperature typical characteristics.
3. $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. mounted on a 1 inch square pad of copper
4. Guaranteed by design, not subject to production testing.

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TYPICAL CHARACTERISTIC CURVES

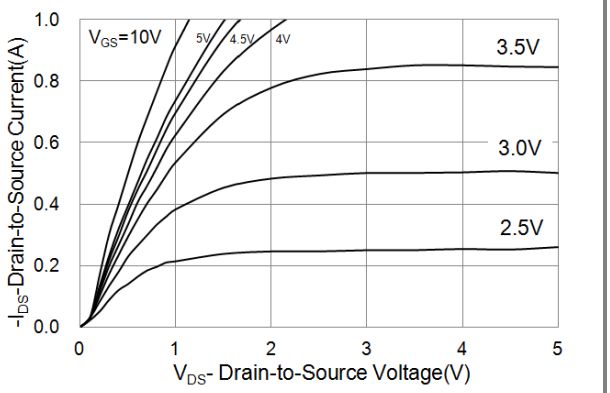

Fig.1 On-Region Characteristics

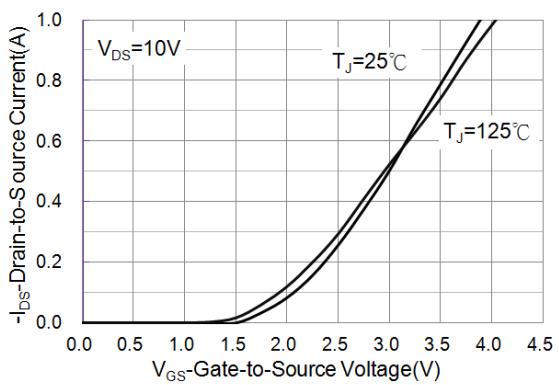

Fig.2 Transfer Characteristics

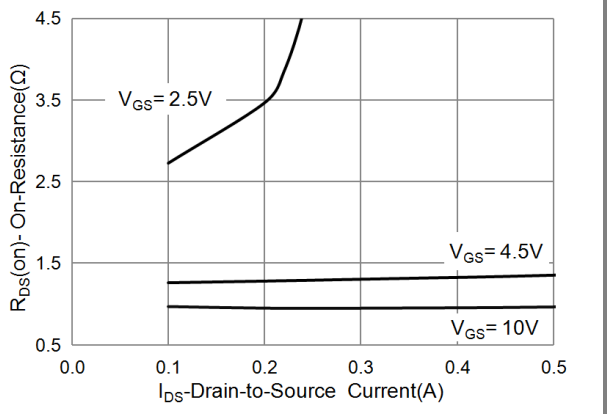

Fig.3 On-Resistance vs. Drain Current

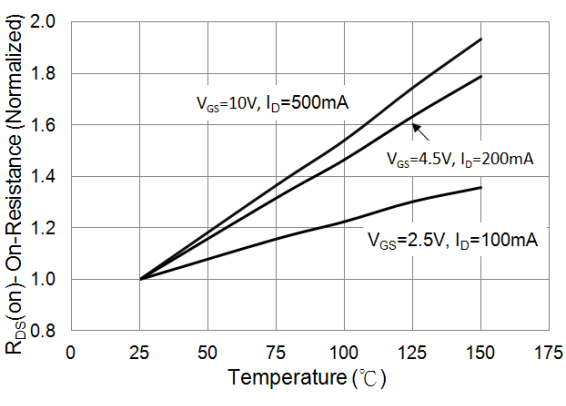

Fig.4 On-Resistance vs. Junction temperature

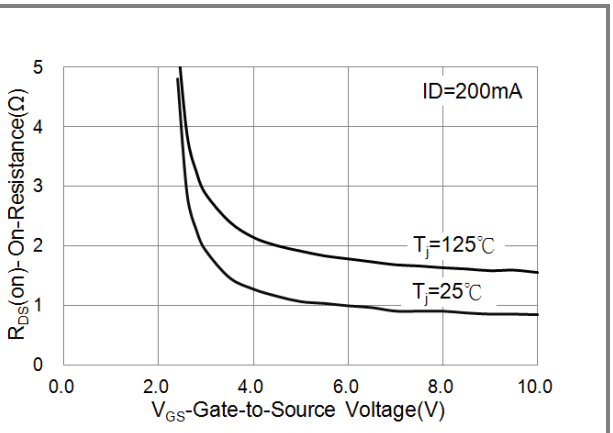

Fig.5 On-Resistance Variation with VGS.

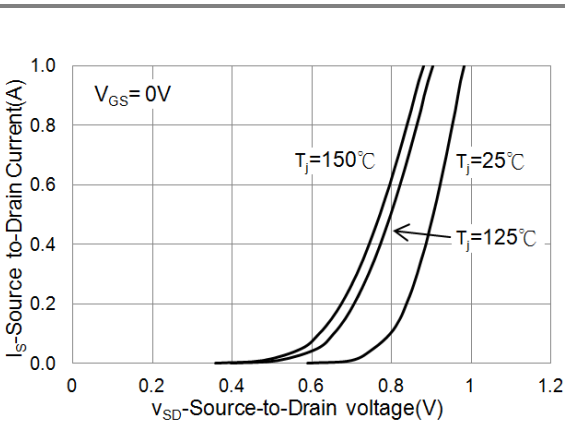

Fig.6 Body Dlode CharacterIsIcs

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TYPICAL CHARACTERISTIC CURVES

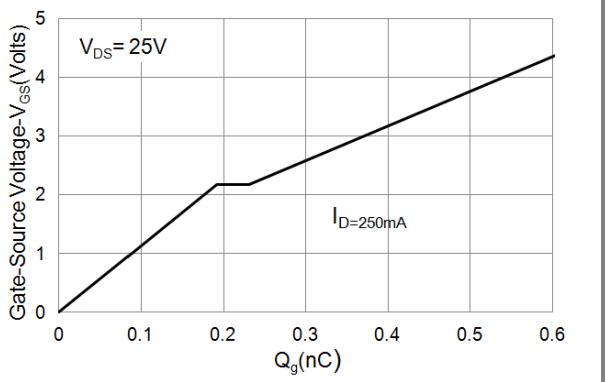

Fig.7 Gate-Charge Characteristics

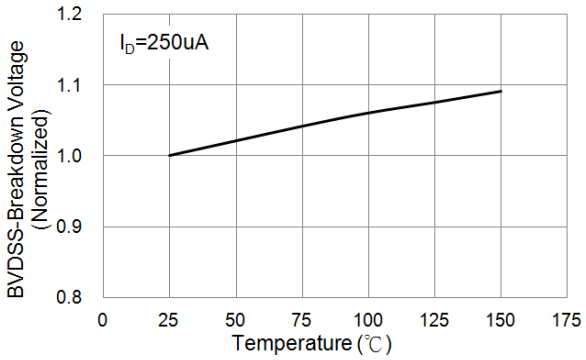

Fig.8 Breakdown Voltage Variation vs. Temperature

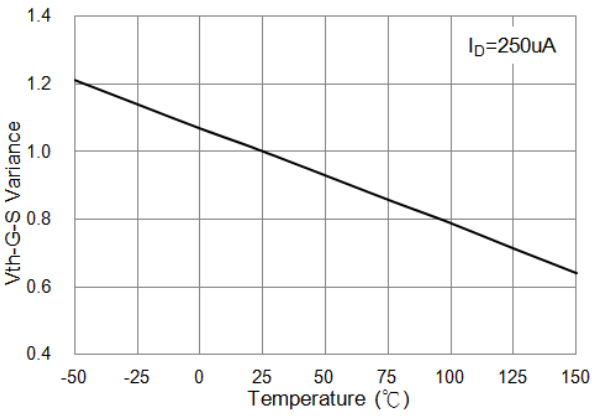

Fig.9 Threshold Voltage Variation with Temperature.

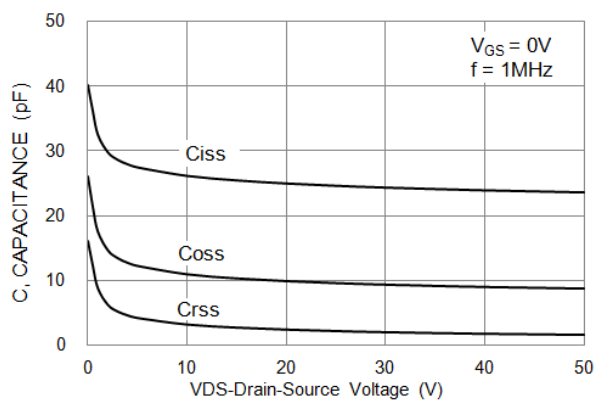

Fig.10 Capacitance vs. Drain-Source Voltage.

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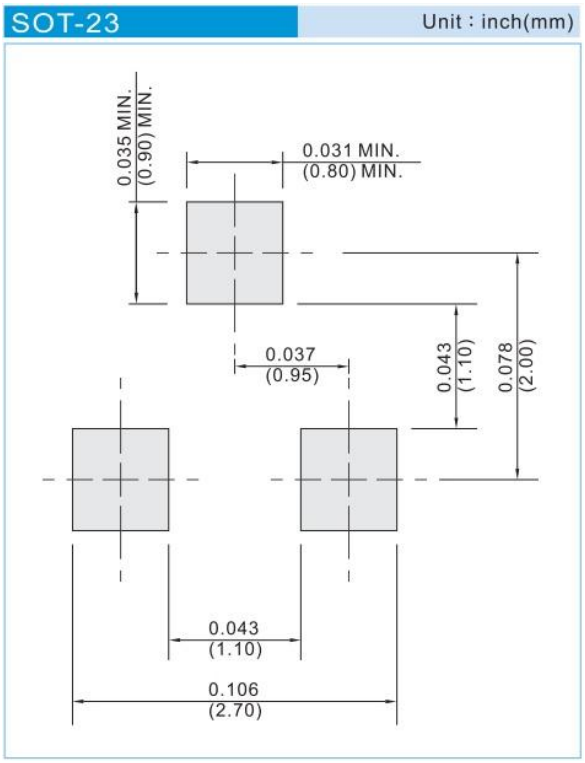
PART NO PACKING CODE VERSION

Part No Packing Code	Package Type	Packing Type	Marking	Version
PJA138K-AU_R1_000A1	SOT-23	3K pcs / 7” reel	8K3	Halogen free

MOUNTING PAD LAYOUT



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