

# DATA SHEET

**74LVC139**

Dual 2-to-4 line  
decoder/demultiplexer

Product specification  
Supersedes data of 2003 May 19

2004 Mar 15

## Dual 2-to-4 line decoder/demultiplexer

## 74LVC139

## FEATURES

- Wide supply voltage range from 1.2 V to 3.6 V
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Demultiplexing capability
- Two independent 2-to-4 decoders
- Multifunction capability
- Active LOW mutually exclusive outputs
- Output drive capability 50  $\Omega$  transmission lines at 125 °C
- In accordance with JEDEC standard no. 8-1A
- ESD protection:  
HBM EIA/JESD22-A114-A exceeds 2000 V  
MM EIA/JESD22-A115-A exceeds 200 V.

## DESCRIPTION

The 74LVC139 is a high-performance, low-voltage and low-power Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74LVC139 is a dual 2-to-4 line decoder/demultiplexer. This device has two independent decoders, each accepting two binary weighted inputs ( $nA0$  and  $nA1$ ) and providing four mutually exclusive active LOW outputs ( $n\bar{Y}0$  to  $n\bar{Y}3$ ). Each decoder has an active LOW input ( $n\bar{E}$ ).

When  $n\bar{E}$  is HIGH, every output is forced HIGH. The enable input can be used as the data input for a 1-to-4 demultiplexer application.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25$  °C;  $t_r = t_f \leq 2.5$  ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	propagation delay $nA$ to $n\bar{Y}n$ $n\bar{E}$ to $n\bar{Y}n$	$C_L = 50$ pF; $V_{CC} = 3.3$ V	2.9 2.7	ns ns
$C_I$	input capacitance		5.0	pF
$C_{PD}$	power dissipation capacitance per multiplexer	$V_{CC} = 3.3$ V; notes 1 and 2	17	pF

## Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  
 $f_o$  = output frequency in MHz;  
 $C_L$  = output load capacitance in pF;  
 $V_{CC}$  = supply voltage in Volts;  
 $N$  = total load switching outputs;  
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.
2. The condition is  $V_I = GND$  to  $V_{CC}$ .

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## FUNCTION TABLE

See note 1

INPUT			OUTPUT			
$n\bar{E}$	nA0	nA1	$n\bar{Y}0$	$n\bar{Y}1$	$n\bar{Y}2$	$n\bar{Y}3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

## Note

1. H = HIGH voltage level;  
L = LOW voltage level;  
X = don't care.

## ORDERING INFORMATION

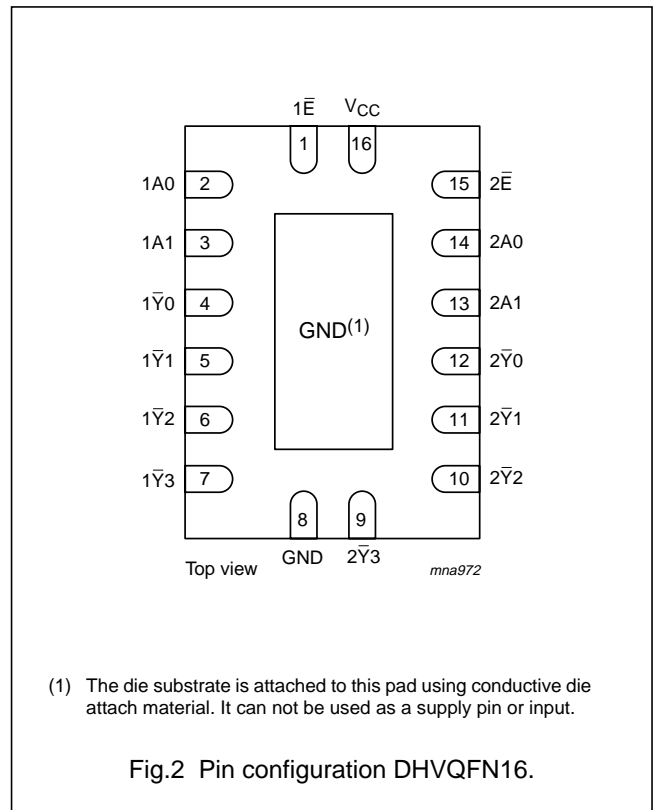
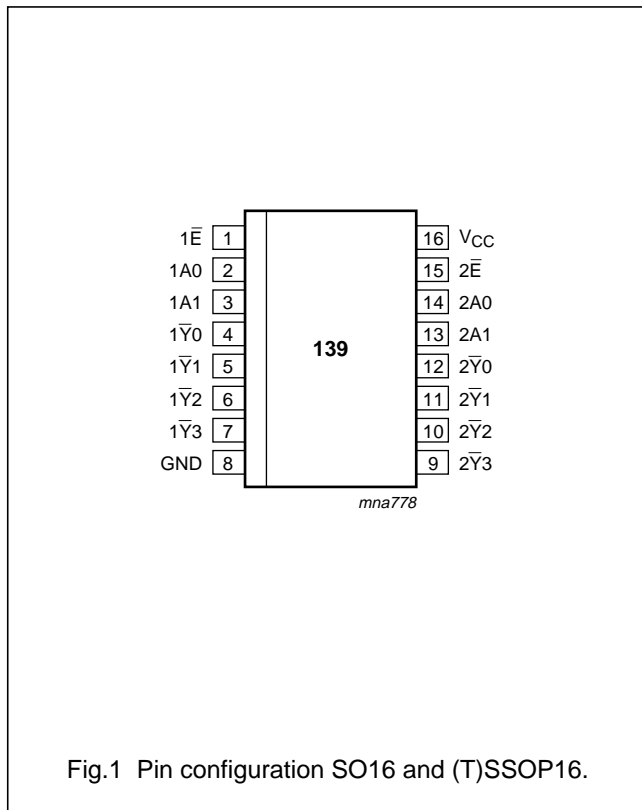
TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74LVC139D	-40 °C to +125 °C	16	SO16	plastic	SOT109-1
74LVC139DB	-40 °C to +125 °C	16	SSOP16	plastic	SOT338-1
74LVC139PW	-40 °C to +125 °C	16	TSSOP16	plastic	SOT403-1
74LVC139BQ	-40 °C to +125 °C	16	DHVQFN16	plastic	SOT763-1

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PINNING

PIN	SYMBOL	DESCRIPTION
1	$1\bar{E}$	enable input (active LOW)
2	1A0	address input
3	1A1	address input
4	$1\bar{Y}0$	output (active LOW)
5	$1\bar{Y}1$	output (active LOW)
6	$1\bar{Y}2$	output (active LOW)
7	$1\bar{Y}3$	output (active LOW)
8	GND	ground (0 V)
9	$2\bar{Y}3$	output (active LOW)
10	$2\bar{Y}2$	output (active LOW)
11	$2\bar{Y}1$	output (active LOW)
12	$2\bar{Y}0$	output (active LOW)
13	2A1	address input
14	2A0	address input
15	$2\bar{E}$	enable input (active LOW)
16	V <sub>CC</sub>	positive supply voltage



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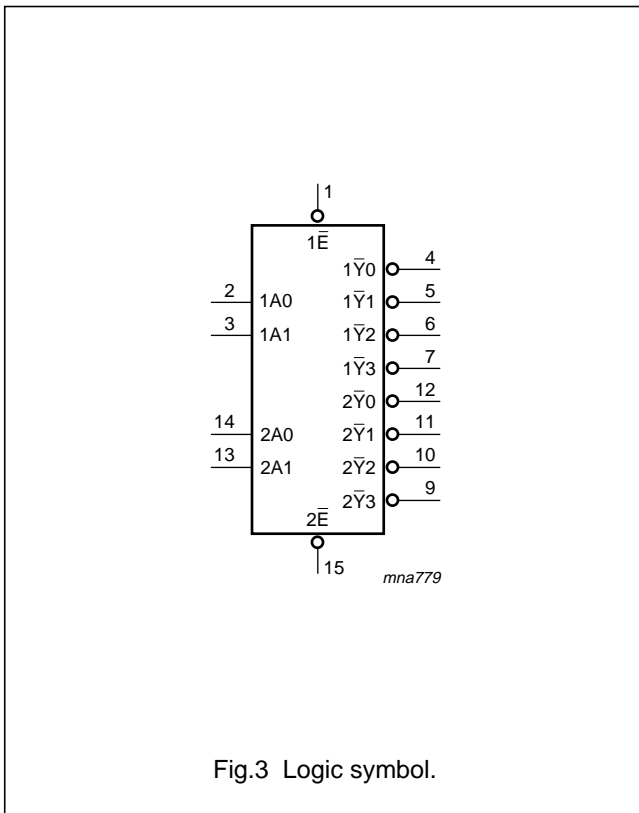


Fig.3 Logic symbol.

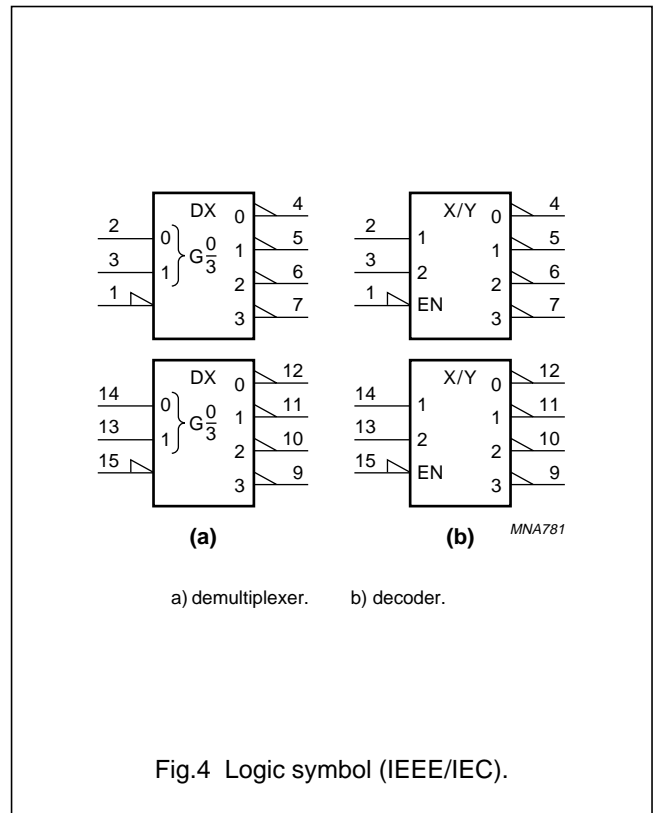


Fig.4 Logic symbol (IEEE/IEC).

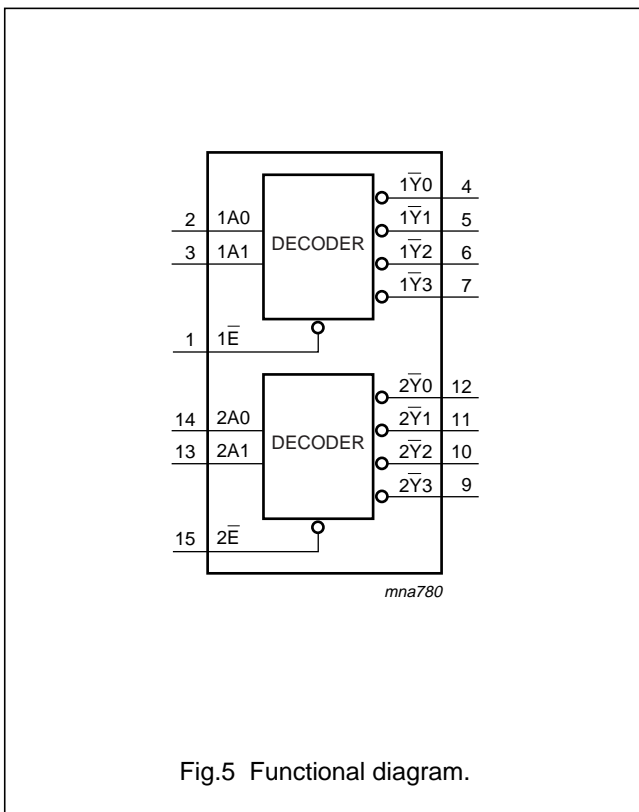


Fig.5 Functional diagram.

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## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CC</sub>	supply voltage	for maximum speed performance	2.7	3.6	V
		for low-voltage applications	1.2	3.6	V
V <sub>I</sub>	input voltage		0	5.5	V
V <sub>O</sub>	output voltage		0	V <sub>CC</sub>	V
T <sub>amb</sub>	operating ambient temperature	in free air	-40	+125	°C
t <sub>r</sub> , t <sub>f</sub>	input rise and fall times	V <sub>CC</sub> = 1.2 V to 2.7 V	0	20	ns/V
		V <sub>CC</sub> = 2.7 V to 3.6 V	0	10	ns/V

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CC</sub>	supply voltage		-0.5	+6.5	V
I <sub>IK</sub>	input diode current	V <sub>I</sub> < 0	-	-50	mA
V <sub>I</sub>	input voltage	note 1	-0.5	+6.5	V
I <sub>OK</sub>	output diode current	V <sub>O</sub> > V <sub>CC</sub> or V <sub>O</sub> < 0 V	-	±50	mA
V <sub>O</sub>	output voltage	note 1	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>O</sub>	output source or sink current	V <sub>O</sub> = 0 V to V <sub>CC</sub>	-	±50	mA
I <sub>CC</sub> , I <sub>GND</sub>	V <sub>CC</sub> or GND current		-	±100	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	power dissipation	T <sub>amb</sub> = -40 °C to +125 °C; note 2	-	500	mW

## Notes

- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- For SO16 packages: above 70 °C derate linearly with 8 mW/K.  
For SSOP16 and TSSOP16 packages: above 60 °C derate linearly with 5.5 mW/K.  
For DHVQFN16 packages: above 60 °C derate linearly with 4.5 mW/K.

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**DC CHARACTERISTICS**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. <sup>(1)</sup>	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 °C to +85 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		1.2	V <sub>CC</sub>	–	–	V
			2.7 to 3.6	2.0	–	–	V
V <sub>IL</sub>	LOW-level input voltage		1.2	–	–	GND	V
			2.7 to 3.6	–	–	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -100 µA	2.7 to 3.6	V <sub>CC</sub> - 0.2	–	–	V
		I <sub>O</sub> = -12 mA	2.7	V <sub>CC</sub> - 0.5	–	–	V
		I <sub>O</sub> = -18 mA	3.0	V <sub>CC</sub> - 0.6	–	–	V
		I <sub>O</sub> = -24 mA	3.0	V <sub>CC</sub> - 0.8	–	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 100 µA	2.7 to 3.6	–	–	0.2	V
		I <sub>O</sub> = 12 mA	2.7	–	–	0.4	V
		I <sub>O</sub> = 24 mA	3.0	–	–	0.55	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND	3.6	–	±0.1	±5	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	3.6	–	0.1	10	µA
ΔI <sub>CC</sub>	additional quiescent supply current per input pin	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A	2.7 to 3.6	–	5	500	µA

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SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. <sup>(1)</sup>	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 °C to +125 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		1.2	V <sub>CC</sub>	–	–	V
			2.7 to 3.6	2.0	–	–	V
V <sub>IL</sub>	LOW-level input voltage		1.2	–	–	GND	V
			2.7 to 3.6	–	–	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -100 μA	2.7 to 3.6	V <sub>CC</sub> - 0.3	–	–	V
		I <sub>O</sub> = -12 mA	2.7	V <sub>CC</sub> - 0.65	–	–	V
		I <sub>O</sub> = -18 mA	3.0	V <sub>CC</sub> - 0.75	–	–	V
		I <sub>O</sub> = -24 mA	3.0	V <sub>CC</sub> - 1	–	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 100 μA	2.7 to 3.6	–	–	0.3	V
		I <sub>O</sub> = 12 mA	2.7	–	–	0.6	V
		I <sub>O</sub> = 24 mA	3.0	–	–	0.8	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND	3.6	–	–	±20	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	3.6	–	–	40	μA
ΔI <sub>CC</sub>	additional quiescent supply current per input pin	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A	2.7 to 3.6	–	–	5000	μA

**Note**

1. Typical values are measured at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.



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**AC CHARACTERISTICS**GND = 0 V;  $t_r = t_f \leq 2.5$  ns;  $C_L = 50$  pF;  $R_L = 500$   $\Omega$ .

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 °C to +85 °C; note 1</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay nAn to $\bar{Y}_n$	see Figs 6 and 8	1.2	–	14	–	ns
			2.7	1.0	3.5	6.3	ns
			3.0 to 3.6	1.0	2.9 <sup>(2)</sup>	5.3	ns
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay n $\bar{E}$ to $\bar{Y}_n$	see Figs 7 and 8	1.2	–	14	–	ns
			2.7	1.0	3.1	5.4	ns
			3.0 to 3.6	1.0	2.7 <sup>(2)</sup>	5.0	ns
t <sub>sk(0)</sub>	skew	note 3	3.0 to 3.6	–	–	1.0	ns
<b>T<sub>amb</sub> = -40 °C to +125 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay nAn to $\bar{Y}_n$	see Figs 6 and 8	1.2	–	–	–	ns
			2.7	1.0	–	8.0	ns
			3.0 to 3.6	1.0	–	7.0	ns
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay n $\bar{E}$ to $\bar{Y}_n$	see Figs 7 and 8	1.2	–	–	–	ns
			2.7	1.0	–	7.0	ns
			3.0 to 3.6	1.0	–	6.5	ns
t <sub>sk(0)</sub>	skew	note 3	3.0 to 3.6	–	–	1.5	ns

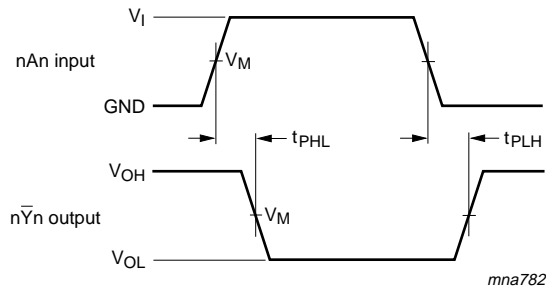
**Notes**

1. All typical values are measured at T<sub>amb</sub> = 25 °C.
2. This typical value is measured at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

Dual 2-to-4 line decoder/demultiplexer

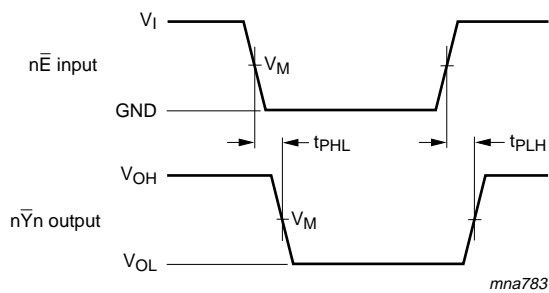
74LVC139

AC WAVEFORMS



$V_M = 1.5\text{ V}$  at  $V_{CC} \geq 2.7\text{ V}$ .  
 $V_M = 0.5 \times V_{CC}$  at  $V_{CC} < 2.7\text{ V}$ .  
 $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.s

Fig.6 Input (nAn) to output (nYn) propagation delays.

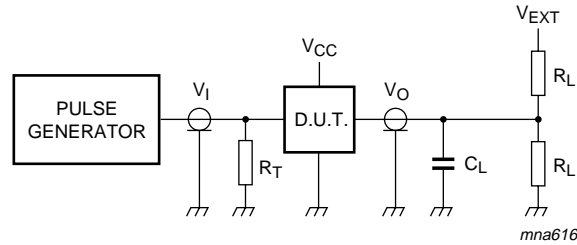


$V_M = 1.5\text{ V}$  at  $V_{CC} \geq 2.7\text{ V}$ .  
 $V_M = 0.5 \times V_{CC}$  at  $V_{CC} < 2.7\text{ V}$ .  
 $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.

Fig.7 Enable input (nE) to output (nYn) propagation delays.

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V <sub>CC</sub>	V <sub>I</sub>	C <sub>L</sub>	R <sub>L</sub>	V <sub>EXT</sub>		
				t <sub>PLH</sub> /t <sub>PHL</sub>	t <sub>PZH</sub> /t <sub>PHZ</sub>	t <sub>PZL</sub> /t <sub>PLZ</sub>
1.2 V	V <sub>CC</sub>	50 pF	500 Ω <sup>(1)</sup>	open	GND	2 × V <sub>CC</sub>
2.7 V	2.7 V	50 pF	500 Ω	open	GND	2 × V <sub>CC</sub>
3.0 V to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	2 × V <sub>CC</sub>

**Note**

1. The circuit performs better when R<sub>L</sub> = 1000 Ω.

Definitions for test circuit:

R<sub>L</sub> = Load resistor.

C<sub>L</sub> = Load capacitance including jig and probe capacitance.

R<sub>T</sub> = Termination resistance should be equal to the output impedance Z<sub>o</sub> of the pulse generator.

Fig.8 Load circuitry for switching times.

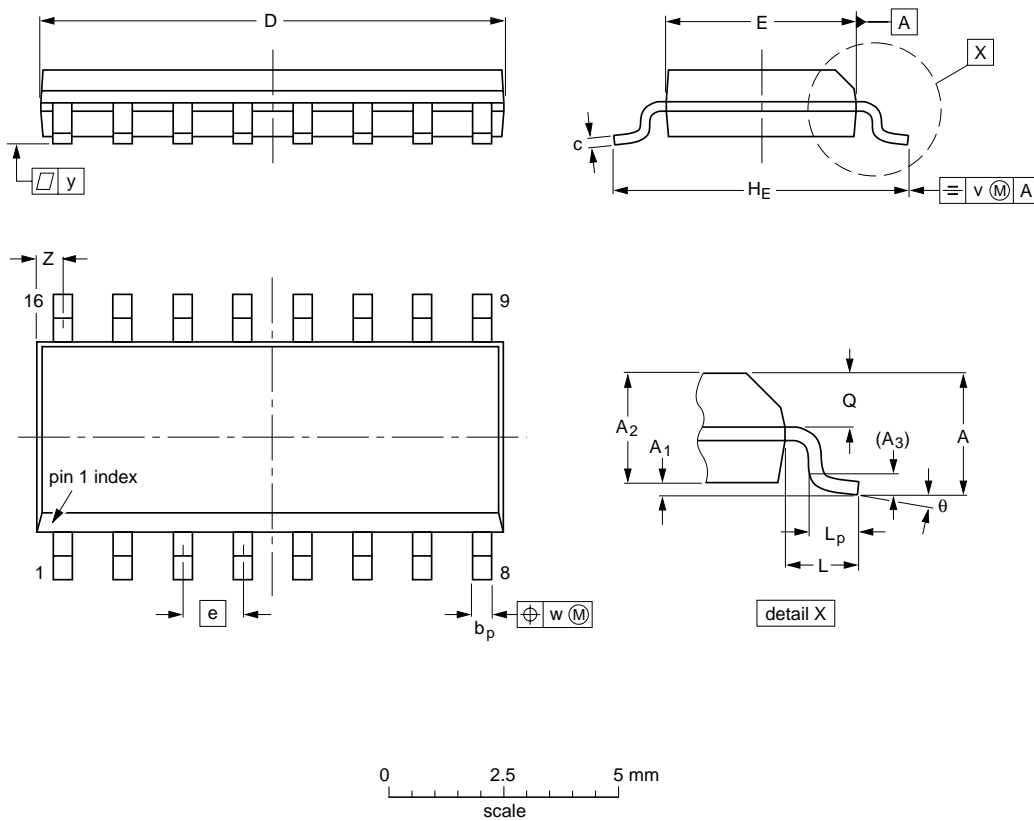
Dual 2-to-4 line decoder/demultiplexer

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PACKAGE OUTLINES

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

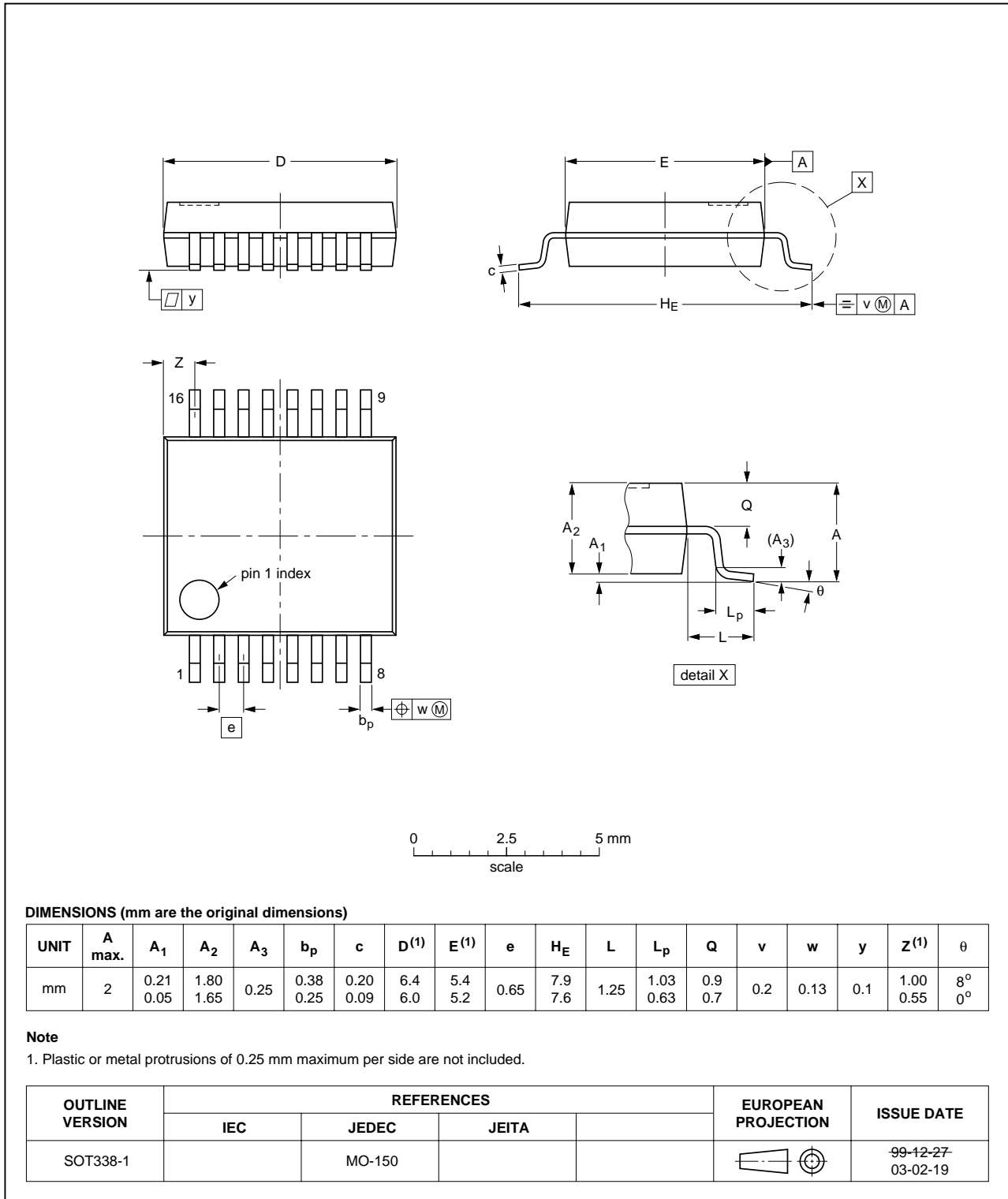
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT109-1	076E07	MS-012			99-12-27 03-02-19

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SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

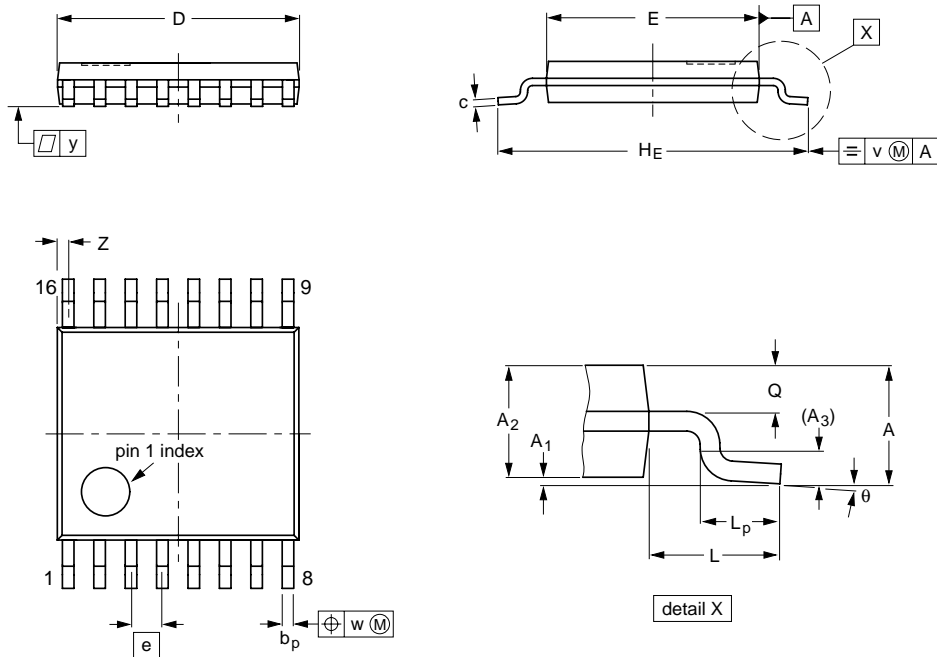


Dual 2-to-4 line decoder/demultiplexer

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TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

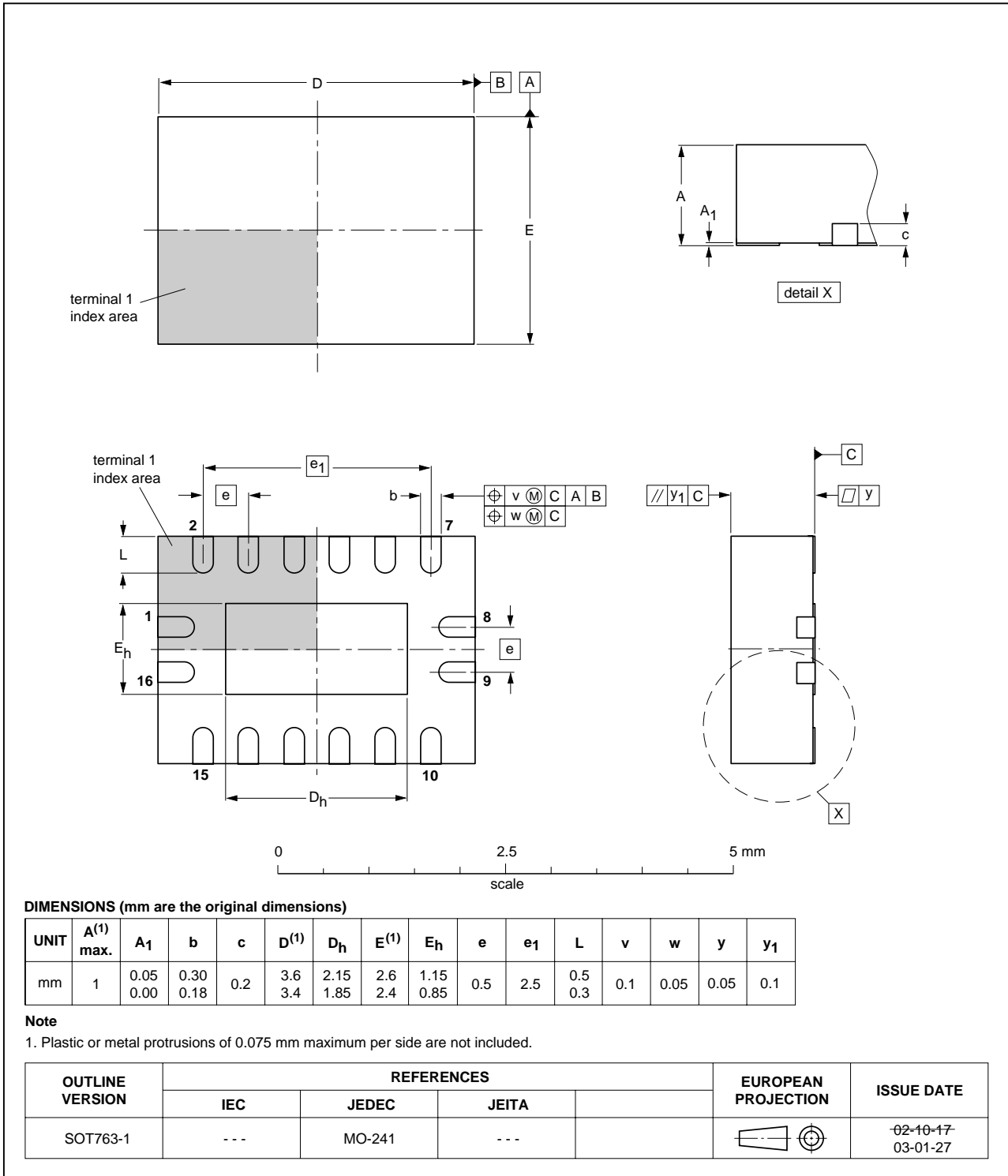
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT403-1		MO-153			99-12-27 03-02-18

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DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1



## Dual 2-to-4 line decoder/demultiplexer

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## DATA SHEET STATUS

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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