

Quad 2-input multiplexer; 3-state

74LVC257

FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- In accordance with JEDEC standard no. 8-1A.
- Inputs accept voltages upto 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Output drive capability 50 Ω transmission lines @ 85 °C
- Non-inverting data path

DESCRIPTION

The 74LVC257 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74LVC257 is a quad 2-input multiplexer with 3-state outputs, which select 4 bits of data from two sources under the control of a common data select input (S). The data inputs from source 0 ($1I_0$ to $4I_0$) are selected when input S is LOW and the data inputs from source 1 ($1I_1$ to $4I_1$) are selected when S is HIGH. Data appears at the outputs (1Y to 4Y) in true (non-inverting) form from the selected inputs. The "257" is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S. The outputs are forced to a high impedance OFF-state when \overline{OE} is HIGH.

The logic equations for the outputs are:

$$1Y = \overline{OE} \cdot (1I_1 \cdot S + 1I_0 \cdot \overline{S})$$

$$2Y = \overline{OE} \cdot (2I_1 \cdot S + 2I_0 \cdot \overline{S})$$

$$3Y = \overline{OE} \cdot (3I_1 \cdot S + 3I_0 \cdot \overline{S})$$

$$4Y = \overline{OE} \cdot (4I_1 \cdot S + 4I_0 \cdot \overline{S})$$

The "257" is identical to the "258" but has non-inverting (true) outputs.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25^\circ\text{C}$; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nI_0, nI_1 to nY S to nY	$C_L = 50$ pF $V_{CC} = 3.3$ V	4.0 4.5	ns
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	30	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; C_L = output load capacity in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is $V_i = \text{GND to } V_{CC}$

ORDERING AND PACKAGE INFORMATION

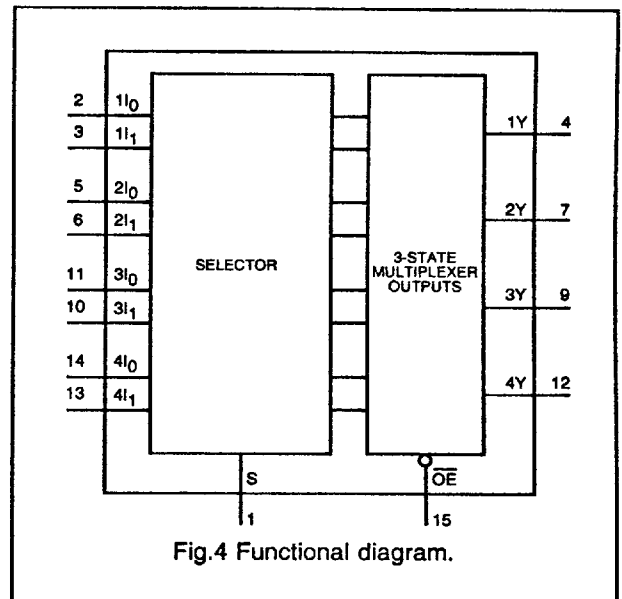
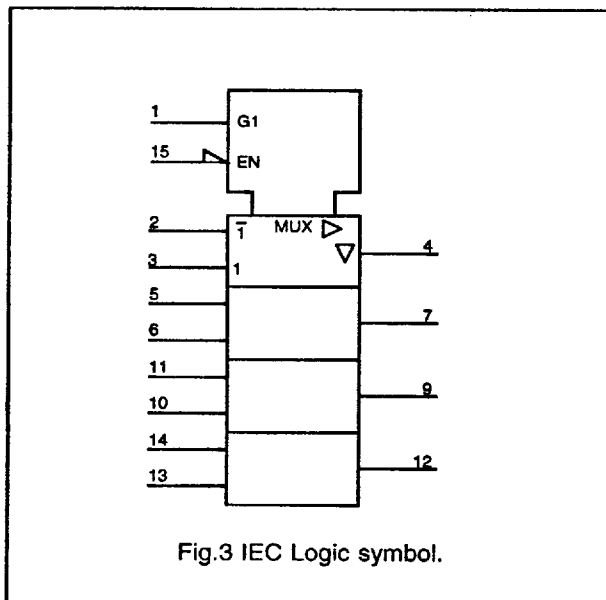
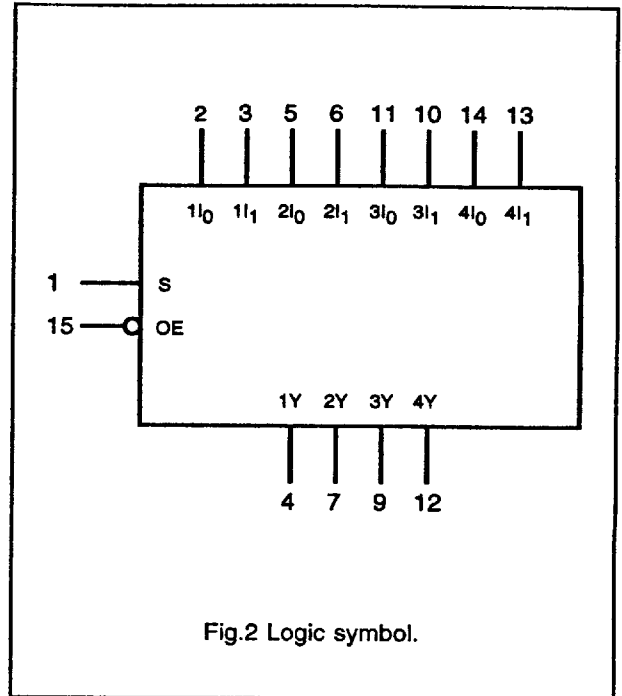
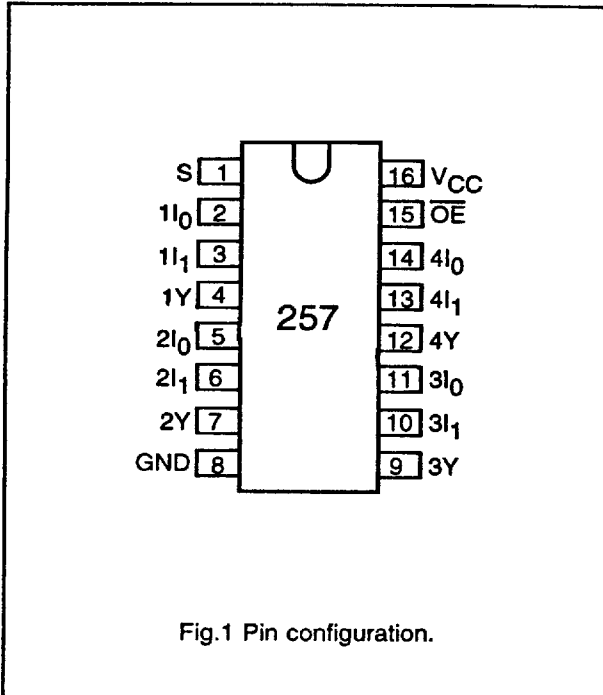
TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC257D	16	SO	plastic	SO16/SOT109A
74LVC257DB	16	SSOP	plastic	SSOP16/SOT338M
74LVC257PW	16	TSSOP	plastic	TSSOP16/SOT403

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	S	common data select input
2, 5, 11, 14	$1I_0$ to $4I_0$	data inputs from source 0
3, 6, 10, 13	$1I_1$ to $4I_1$	data inputs from source 1
4, 7, 9, 12	1Y to 4Y	3-state multiplexer outputs
8	GND	ground (0 V)
15	\overline{OE}	3-state output enable input (active LOW)
16	V_{CC}	positive supply voltage

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FUNCTION TABLE

INPUTS				OUTPUT
\overline{OE}	S	ni_0	ni_1	nY
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 Z = high impedance OFF-state

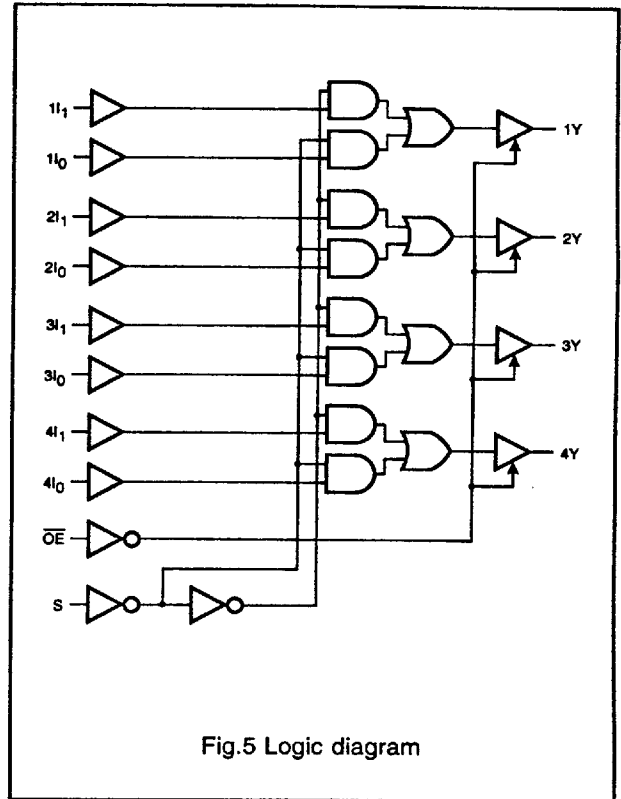


Fig.5 Logic diagram

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DC CHARACTERISTICS FOR 74LVC257

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".

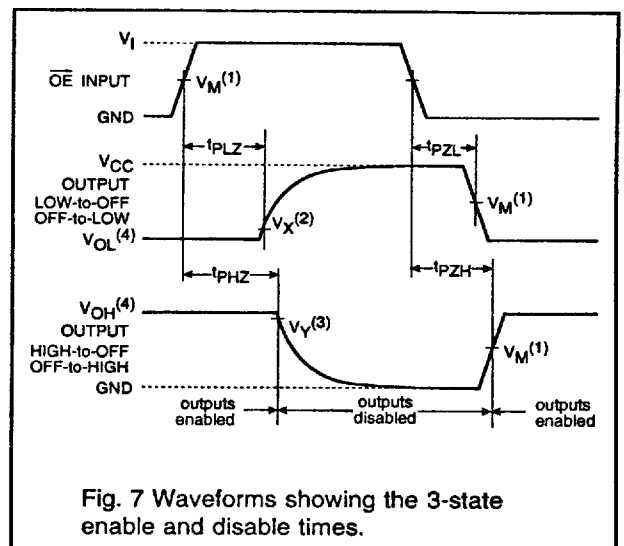
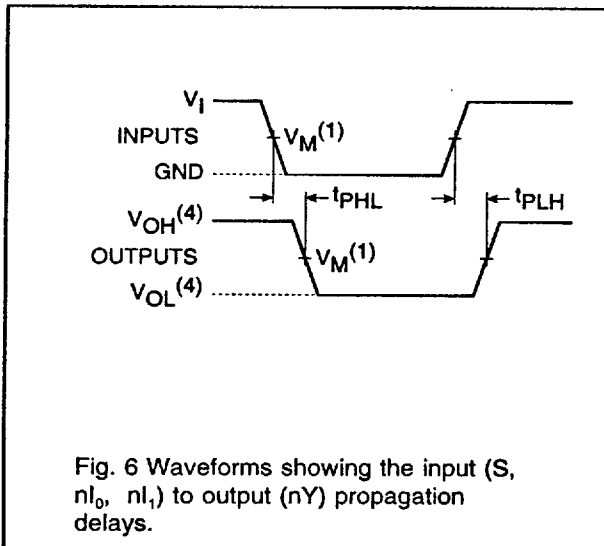
AC CHARACTERISTICS FOR 74LVC257

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		MIN.	TYP.	MAX.		V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay nI_0 to nY ; nI_1 to nY	-	-	-	ns	1.2	Fig.6
		-	4.8	8.0		2.7	
		-	4.0*	7.0		3.0 to 3.6	
t_{PHL}/t_{PLH}	propagation delay S to nY	-	-	-	ns	1.2	Fig.6
		-	5.2	10.5		2.7	
		-	4.5*	9.5		3.0 to 3.6	
t_{PHZ}/t_{PZL}	3-state output enable time \overline{OE} to nY	-	-	-	ns	1.2	Fig.7
		-	5.2	9.0		2.7	
		-	4.5*	8.0		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time \overline{OE} to nY	-	-	-	ns	1.2	Fig.7
		-	4.0	7.0		2.7	
		-	3.8*	6.0		3.0 to 3.6	

Notes: All typical values are measured at $T_{amb} = 25$ °C.
* Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS



- Notes:
- (1) $V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
 $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
 - (2) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
 $V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
 - (3) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
 $V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
 - (4) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

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