

1:3 LVPECL CLOCK BUFFER WITH PROGRAMMABLE DIVIDER

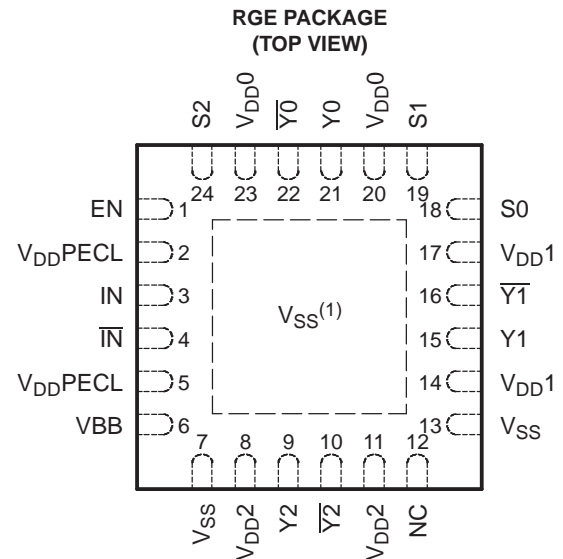
FEATURES

- Distributes One Differential Clock Input to Three LVPECL Differential Clock Outputs
- Programmable Output Divider for Two LVPECL Outputs
- Low-Output Skew 15 ps (Typical)
- V_{CC} Range 3 V–3.6 V
- Signaling Rate Up to 800-MHz LVPECL
- Differential Input Stage for Wide Common-Mode Range
- Provides VBB Bias Voltage Output for Single-Ended Input Signals
- Receiver Input Threshold ± 75 mV
- 24-Terminal QFN Package (4 mm \times 4 mm)
- Accepts Any Differential Signaling: LVDS, HSTL, CML, VML, SSTL-2, and Single-Ended: LVTTTL/LVCMOS

DESCRIPTION

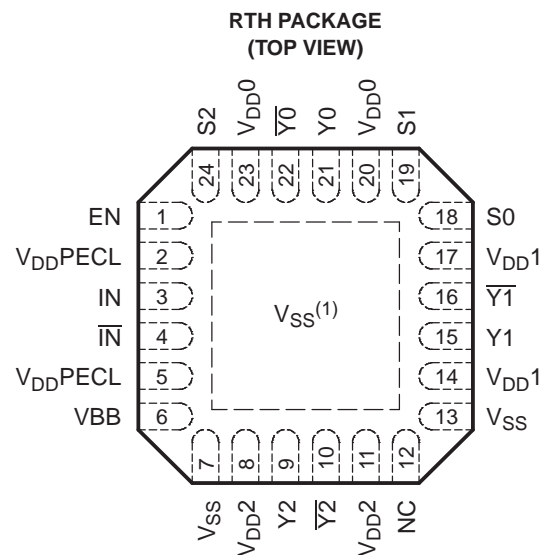
The CDCP1803 clock driver distributes one pair of differential clock inputs to three pairs of LVPECL differential clock outputs $Y[2:0]$ and $\overline{Y[2:0]}$ with minimum skew for clock distribution. The CDCP1803 is specifically designed for driving 50- Ω transmission lines.

The CDCP1803 has three control terminals, S0, S1, and S2, to select different output mode settings; see Table 1 for details. The CDCP1803 is characterized for operation from -40°C to 85°C . For use in single-ended driver applications, the CDCP1803 also provides a VBB output terminal that can be directly connected to the unused input as a common-mode voltage reference.



(1) Thermal pad must be connected to V_{SS} .

P0024-02



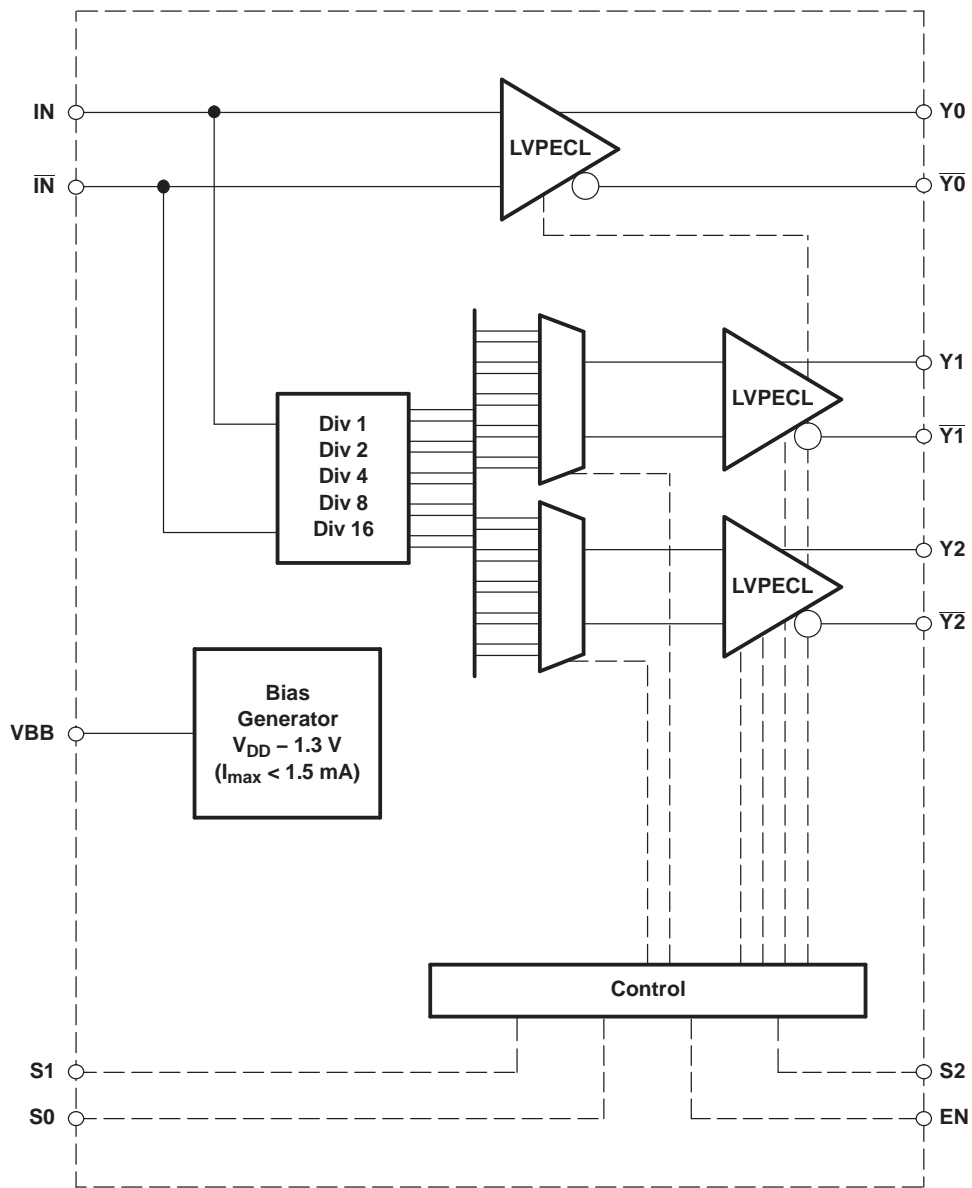
(1) Thermal pad must be connected to V_{SS} .

P0025-02



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

FUNCTIONAL BLOCK DIAGRAM



B0059-02

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
EN	1	I (with 60-k Ω pullup)	<p>ENABLE: Enables or disables all outputs simultaneously.</p> <p>EN = 1: outputs on according to S[2:0] settings EN = 0: outputs Y[2:0] off (high impedance) See Table 1 for details.</p>
IN, $\overline{\text{IN}}$	3, 4	I (differential)	<p>Differential input clock. Input stage is sensitive and has a wide common-mode range. Therefore, almost any type of differential signal can drive this input (LVPECL, LVDS, CML, HSTL). Because the input is high-impedance, it is recommended to terminate the PCB transmission line before the input (e.g., with 100 Ω across input). Input can also be driven by a single-ended signal if the complementary input is tied to VBB. A more-advanced scheme for single-ended signals is given in the <i>Application Information</i> section near the end of this document.</p> <p>The inputs employ an ESD structure protecting the inputs in case of an input voltage exceeding the rails by more than ~ 0.7 V. Reverse biasing of the IC through these inputs is possible and must be prevented by limiting the input voltage $< V_{\text{DD}}$.</p>
NC	12		No connect. Leave this terminal open or tie to ground.
S[2:0]	24, 19, 18	I (with 60-k Ω pullup)	Select mode of operation. Defines the output configuration of Y[2:0], see Table 1 for configuration.
VBB	6	O	<p>Bias voltage output can be used to bias unused complementary input $\overline{\text{IN}}$ for single-ended input signals.</p> <p>The output voltage of VBB is $V_{\text{DD}} - 1.3$ V. When driving a load, the output current drive is limited to about 1.5 mA.</p>
V_{DDPECL}	2, 5	Supply	Supply voltage PECL input + internal logic
$V_{\text{DD}}[2:0]$	8, 11, 14, 17, 20, 23	Supply	<p>PECL output supply voltage for output Y[2:0]. Each output can be disabled by pulling the corresponding V_{DDX} to GND.</p> <p>CAUTION: In this mode, no voltage from outside may be forced, because internal diodes could be forced in forward direction. Thus, it is recommended to disconnect the output if it is not being used.</p>
V_{SS}	7, 13	Supply	Device ground
$\overline{\text{Y}}[2:0]$ Y[2:0]	9, 15, 21 10, 16, 22	O (LVPECL)	LVPECL clock outputs. These outputs provide low-skew copies of IN or down-divided copies of clock IN based on selected mode of operation S[2:0]. If an output is unused, the output can simply be left open to save power and minimize noise impact to the remaining outputs.

CONTROL TERMINAL SETTINGS

The CDCP1803 has three control terminals (S0, S1, and S2) and an enable terminal (EN) to select different output mode settings.

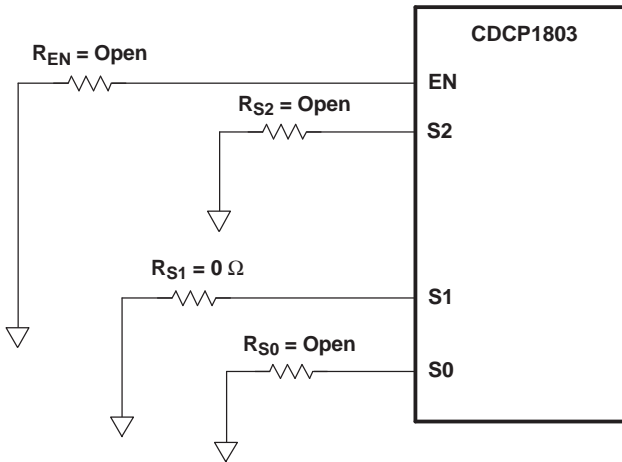
Setting for Mode 20:

EN = 1

S2 = 1

S1 = 0

S0 = 1



S0084-02

Figure 1. Control Terminal Setting for Example

Table 1. Selection Mode Table

MODE	EN	S2	S1	S0	LVPECL ⁽¹⁾		
					Y0	Y1	Y2
0	0	x	x	x	Off (high-z)		
1	1	0	0	0	÷ 1	÷ 1	÷ 1
2	1	0	0	V _{DD} /2	÷ 1	Off (high-z)	Off (high-z)
3	1	0	0	1	÷ 1	÷ 1	Off (high-z)
4	1	0	V _{DD} /2	0	÷ 1	÷ 2	Off (high-z)
5	1	0	V _{DD} /2	V _{DD} /2	÷ 1	÷ 4	Off (high-z)
6	1	0	V _{DD} /2	1	÷ 1	÷ 8	Off (high-z)
7	1	0	1	0	÷ 1	Off (high-z)	÷ 1
8	1	0	1	1	÷ 1	÷ 2	÷ 1
9	1	V _{DD} /2	0	0	÷ 1	÷ 4	÷ 1
10	1	V _{DD} /2	0	V _{DD} /2	÷ 1	÷ 8	÷ 1
11	1	V _{DD} /2	0	1	÷ 1	Off (high-z)	÷ 2
12	1	V _{DD} /2	V _{DD} /2	0	÷ 1	÷ 1	÷ 2
13	1	V _{DD} /2	V _{DD} /2	V _{DD} /2	÷ 1	÷ 2	÷ 2
14	1	V _{DD} /2	V _{DD} /2	1	÷ 1	÷ 4	÷ 2
15	1	V _{DD} /2	1	0	÷ 1	÷ 8	÷ 2
16	1	V _{DD} /2	1	V _{DD} /2	÷ 1	Off (high-z)	÷ 4
17	1	V _{DD} /2	1	1	÷ 1	÷ 1	÷ 4
18	1	1	0	0	÷ 1	÷ 2	÷ 4
19	1	1	0	V _{DD} /2	÷ 1	÷ 4	÷ 4
20	1	1	0	1	÷ 1	÷ 8	÷ 4
21	1	1	V _{DD} /2	0	÷ 1	Off (high-z)	÷ 8
22	1	1	V _{DD} /2	V _{DD} /2	÷ 1	÷ 1	÷ 8
23	1	1	V _{DD} /2	1	÷ 1	÷ 2	÷ 8
24	1	1	1	0	÷ 1	÷ 4	÷ 8
25	1	1	1	V _{DD} /2	÷ 1	÷ 8	÷ 8
26	1	1	1	1	÷ 1	Off (high-z)	÷ 16
27	V _{DD} /2	0	0	0	÷ 1	÷ 1	÷ 16
28	V _{DD} /2	0	0	V _{DD} /2	÷ 1	÷ 2	÷ 16
29	V _{DD} /2	0	0	1	÷ 1	÷ 4	÷ 16
30	V _{DD} /2	0	V _{DD} /2	0	÷ 1	÷ 8	÷ 16
Rsv	V _{DD} /2	1	V _{DD} /2	1	Reserved	Reserved	Reserved
Rsv	V _{DD} /2	1	1	0	N/A	Low	Low

(1) The LVPECL outputs are open-emitter stages. Thus, if the unused LVPECL outputs Y0, Y1, or Y2 are left unconnected, then the current consumption is minimized and noise impact to remaining outputs is neglectable. Also, each output can be individually disabled by connecting the corresponding V_{DD} input to GND.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature (unless otherwise noted)⁽¹⁾

V _{DD}	Supply voltage	–0.3 V to 3.8 V
V _I	Input voltage	–0.2 V to (V _{DD} + 0.2 V)
V _O	Output voltage	–0.2 V to (V _{DD} + 0.2 V)
	Differential short-circuit current, Y _n , \overline{Y}_n , I _{OSD}	Continuous
	Electrostatic discharge (HBM 1.5 kΩ, 100 pF), ESD	>2000 V
	Moisture level 24-terminal QFN package (solder reflow temperature of 235°C) MSL	2
T _{stg}	Storage temperature	–65°C to 150°C
T _J	Maximum junction temperature	125°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
V _{DD}	Supply voltage	3	3.3	3.6	V
T _A	Operating free-air temperature	–40		85	°C

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

LVPECL INPUT IN, \overline{IN}

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{clk}	Input frequency		0		800	MHz
V _{CM}	High-level input common mode		1	V _{DD} – 0.3		V
V _{IN}	Input voltage swing between IN and \overline{IN} ⁽¹⁾		500		1300	mV
	Input voltage swing between IN and \overline{IN} ⁽²⁾		125		1300	
I _{IN}	Input current	V _I = V _{DD} or 0 V			±10	μA
R _{IN}	Input impedance		300			kΩ
C _I	Input capacitance at IN, \overline{IN}			1		pF

(1) Is required to maintain ac specifications

(2) Is required to maintain device functionality

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

LVPECL OUTPUT DRIVER Y[2:0], $\overline{Y[2:0]}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clk}	Output frequency, see Figure 3 .		0		800	MHz
V_{OH}	High-level output voltage	Termination with 50 Ω to $V_{DD} - 2 V$	$V_{DD} - 1.18$		$V_{DD} - 0.81$	V
V_{OL}	Low-level output voltage	Termination with 50 Ω to $V_{DD} - 2 V$	$V_{DD} - 1.98$		$V_{DD} - 1.55$	V
V_O	Output voltage swing between Y and \overline{Y} , see Figure 3 .	Termination with 50 Ω to $V_{DD} - 2 V$	500			mV
I_{OZL}	Output 3-state current	$V_{DD} = 3.6 V, V_O = 0 V$			5	μA
I_{OZH}		$V_{DD} = 3.6 V, V_O = V_{DD} - 0.8 V$			10	
t_r/t_f	Rise and fall times	20% to 80% of V_{OUTPP} , see Figure 7 .	200		350	ps
$t_{skpecl(o)}$	Output skew between any LVPECL output Y[2:0] and $\overline{Y[2:0]}$	See Note A in Figure 6 .		15	30	ps
t_{Duty}	Output duty-cycle distortion ⁽¹⁾	Crossing point-to-crossing point distortion	-50		50	ps
$t_{sk(pp)}$	Part-to-part skew	Any Y, see Note B in Figure 6 .		50		ps
C_O	Output capacitance	$V_O = V_{DD}$ or GND		1		pF
LOAD	Expected output load			50		Ω

(1) For an 800-MHz signal, the 50-ps error would result in a duty cycle distortion of $\pm 4\%$ when driven by an ideal clock input signal.

LVPECL INPUT-TO-LVPECL OUTPUT PARAMETERS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd(lh)}$	Propagation delay, rising edge	VOX to VOX	320		600	ps
$t_{pd(hl)}$	Propagation delay, falling edge	VOX to VOX	320		600	ps
$t_{sk(p)}$	LVPECL pulse skew	VOX to VOX, see Note C in Figure 6 .			100	ps

JITTER CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
JITTER CHARACTERISTICS						
$t_{jitterLVPECL}$	Additive phase jitter from input to LVPECL output Y[2:0], see Figure 2 .	12 kHz to 20 MHz, $f_{out} = 250 MHz$ to 800 MHz, divide-by-1 mode			0.15	ps rms
		50 kHz to 40 MHz, $f_{out} = 250 MHz$ to 800 MHz, divide-by-1 mode			0.25	

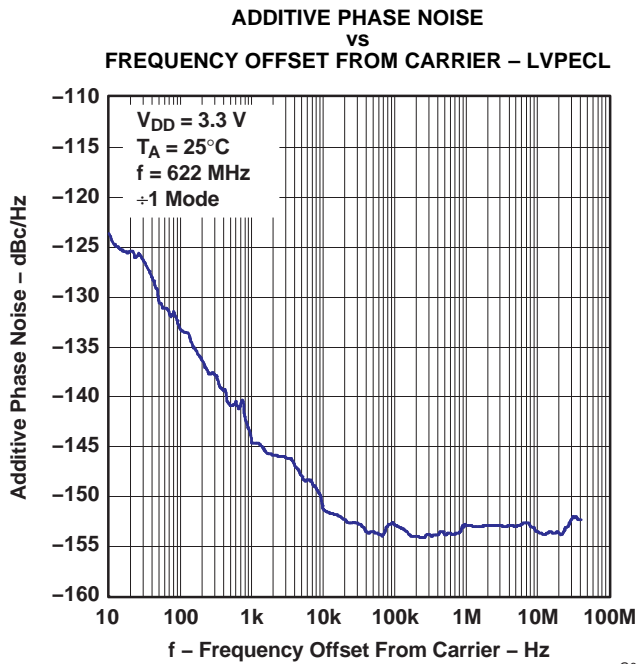


Figure 2.

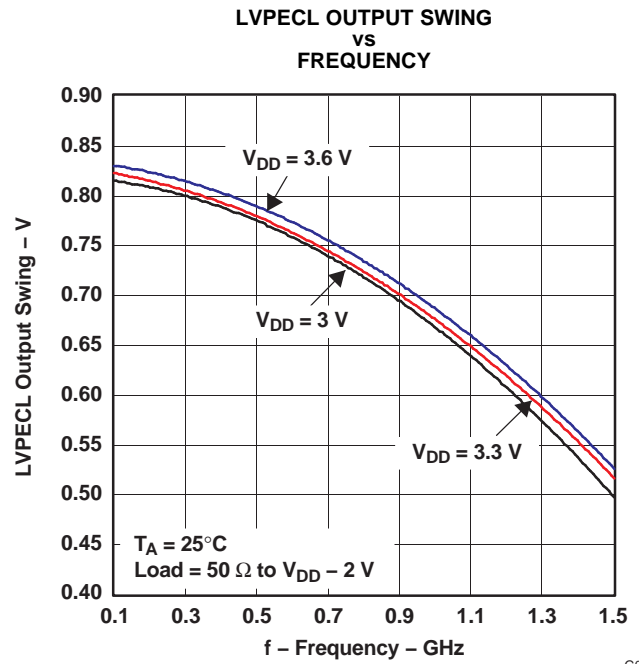
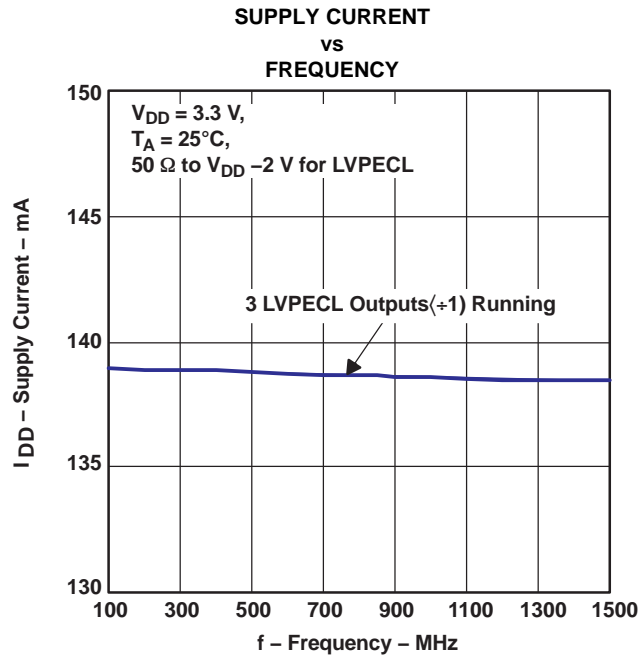


Figure 3.

SUPPLY CURRENT ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{DD}	Supply current	Full load		140		mA
		No load			90	
	Supply current saving per LVPECL output stage disabled, no load	f = 800 MHz for LVPECL output, V _{DD} = 3.3 V		10		
I _{DDZ}	Supply current, 3-state	All outputs in high-impedance state by control logic, f = 0 Hz, V _{DD} = 3.6 V			0.5	mA



PACKAGE THERMAL RESISTANCE

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA-1}$ QFN-24 package thermal resistance ⁽¹⁾	4-layer JEDEC test board (JESD51-7), airflow = 0 ft/min		106.6		°C/W
$R_{\theta JA-2}$ QFN-24 package thermal resistance with thermal vias in PCB ⁽¹⁾	4-layer JEDEC test board (JESD51-7) with four thermal vias of 22-mil diameter each, airflow = 0 ft/min		55.4		°C/W

- (1) It is recommended to provide four thermal vias to connect the thermal pad of the package effectively with the PCB and ensure a good heat sink.

Example:

Calculation of the junction-lead temperature with a 4-layer JEDEC test board using four thermal vias:

$$T_{\text{Chassis}} = 85^{\circ}\text{C} \text{ (temperature of the chassis)}$$

$$P_{\text{effective}} = I_{\text{max}} \times V_{\text{max}} = 90 \text{ mA} \times 3.6 \text{ V} = 324 \text{ mW} \text{ (max power consumption inside the package)}$$

$$\theta T_{\text{Junction}} = \theta_{\text{JA-2}} \times P_{\text{effective}} = 55.45^{\circ}\text{C/W} \times 324 \text{ mW} = 17.97^{\circ}\text{C}$$

$$T_{\text{Junction}} = \theta T_{\text{Junction}} + T_{\text{Chassis}} = 17.97^{\circ}\text{C} + 85^{\circ}\text{C} = 103^{\circ}\text{C} \text{ (the maximum junction temperature of } T_{\text{die-max}} = 125^{\circ}\text{C is not violated)}$$

CONTROL INPUT CHARACTERISTICS

over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{su}	Setup time, S0, S1, S2, and EN terminals before clock IN		25			ns
t_h	Hold time, S0, S1, S2, and EN terminals after clock IN		0			ns
$t_{(disable)}$	Time between latching the EN low transition and when all outputs are disabled (how much time is required until the outputs turn off)			10		ns
$t_{(enable)}$	Time between latching the EN low-to-high transition and when outputs are enabled based on control settings (how much time passes before the outputs carry valid signals)			1		μs
Rpullup	Internal pullup resistor on S[2:0] and EN input		42	60	78	k Ω
$V_{IH(H)}$	Three-level input high, S0, S1, S2, and EN terminals ⁽¹⁾		0.9 V_{DD}			V
$V_{IL(L)}$	Three-level low, S0, S1, S2, and EN terminals				0.1 V_{DD}	V
I_{IH}	Input current, S0, S1, S2, and EN terminals	$V_I = V_{DD}$			-5	μA
I_{IL}		$V_I = GND$	38		85	μA

(1) Leaving this terminal floating automatically pulls the logic level high to V_{DD} through an internal pullup resistor of 60 k Ω .

BIAS VOLTAGE V_{BB}

over operating free-air temperature range

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BB}	Output reference voltage	$V_{DD} - 1.4$		$V_{DD} - 1.2$	V

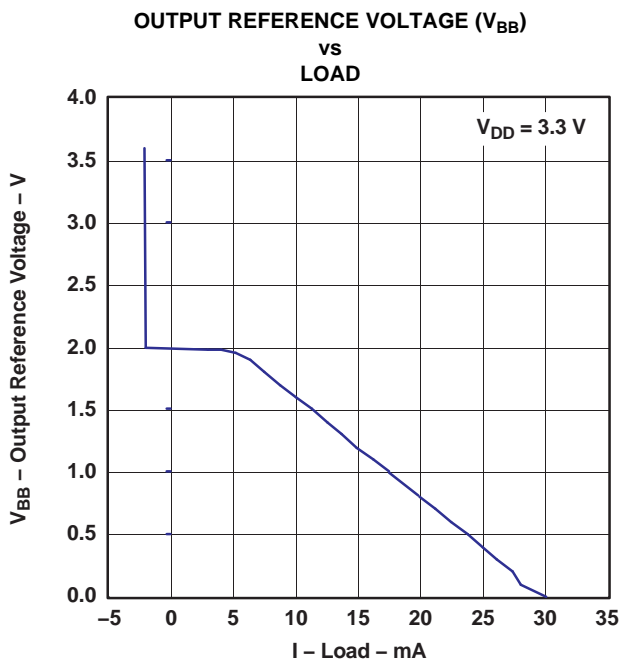
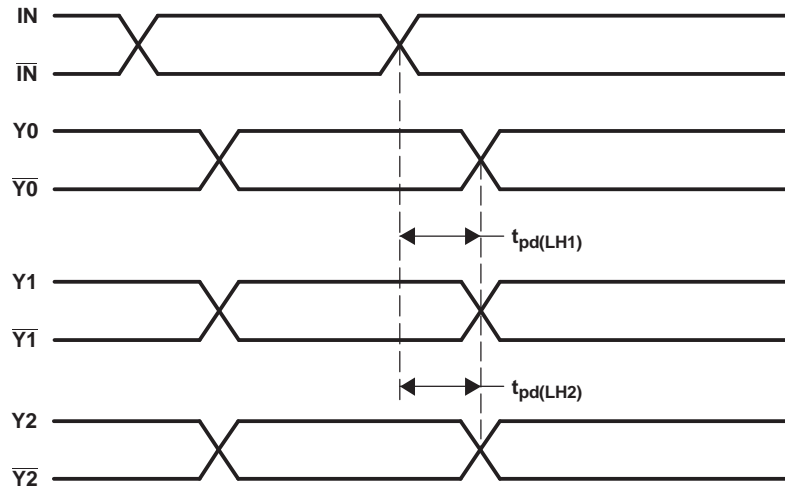


Figure 5.

G004

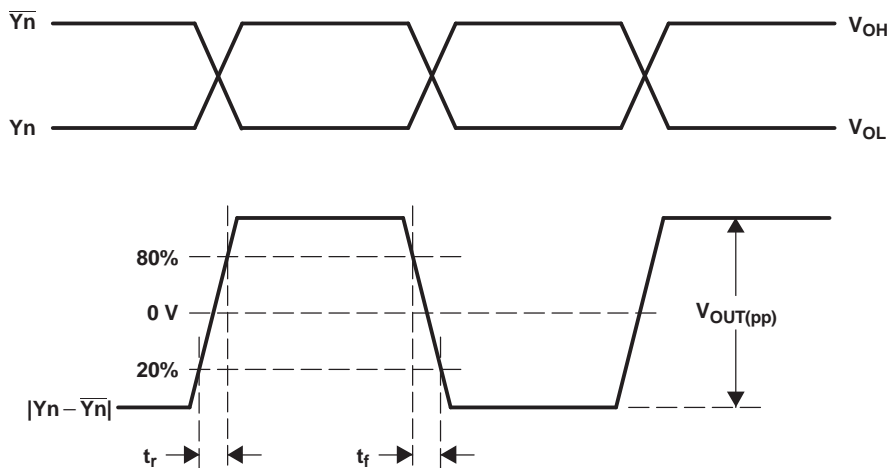
PARAMETER MEASUREMENT INFORMATION



- NOTES: A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and the slowest $t_{pd(LH)n}$ ($n = 0 \dots 2$)
 - The difference between the fastest and the slowest $t_{pd(HL)n}$ ($n = 0 \dots 2$)
- B. Part-to-part skew, $t_{sk(pp)}$, is calculated as the greater of:
- The difference between the fastest and the slowest $t_{pd(LH)n}$ ($n = 0 \dots 2$ for LVPECL, $n = 3$ for LVCMOS) across multiple devices
 - The difference between the fastest and the slowest $t_{pd(HL)n}$ ($n = 0 \dots 2$ for LVPECL, $n = 3$ for LVCMOS) across multiple devices
- C. Pulse skew, $t_{sk(p)}$, is calculated as the magnitude of the absolute time difference between the high-to-low ($t_{pd(HL)}$) and the low-to-high ($t_{pd(LH)}$) propagation delays when a single switching input causes one or more outputs to switch, $t_{sk(p)} = |t_{pd(HL)} - t_{pd(LH)}|$. Pulse skew is sometimes referred to as *pulse width distortion* or *duty cycle skew*.

T0067-02

Figure 6. Waveforms for Calculation of $t_{sk(o)}$ and $t_{sk(pp)}$



T0058-02

Figure 7. LVPECL Differential Output Voltage and Rise/Fall Time

PCB DESIGN FOR THERMAL FUNCTIONALITY

It is recommended to take special care of the PCB design for good thermal flow from the QFN 24-terminal package to the PCB.

Due to the three LVPECL outputs, the current consumption of the CDCP1803 is fixed.

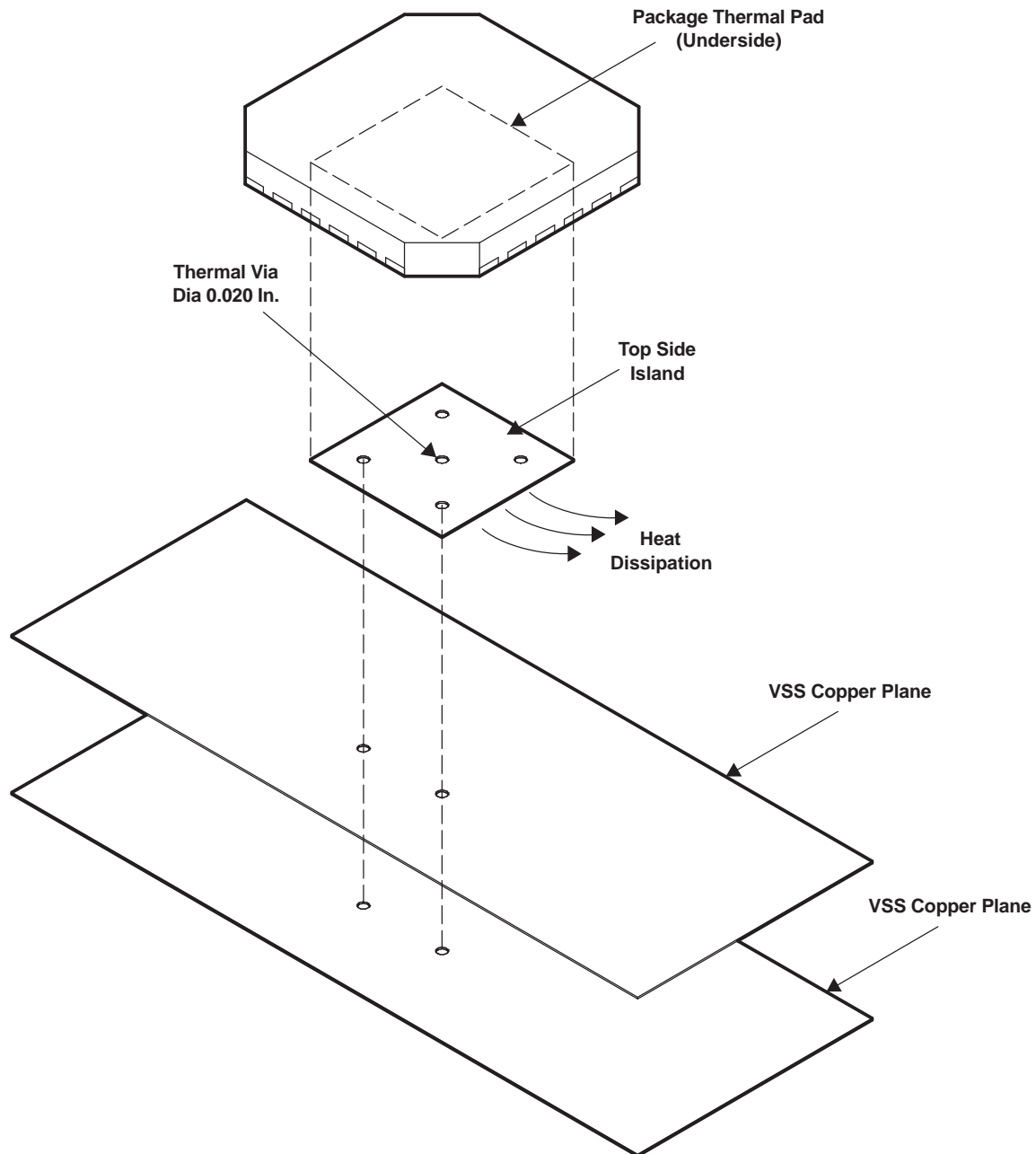
JEDEC JESD51-7 specifies thermal conductivity for standard PCB boards.

PARAMETER MEASUREMENT INFORMATION (continued)

Modeling the CDCP1803 with a standard 4-layer JEDEC board results in a 59.5°C maximum temperature with $R_{\theta JA}$ of 106.62°C/W for 25°C ambient temperature.

When deploying four thermal vias (one per quadrant), the thermal flow improves significantly, yielding 42.9°C maximum temperature with $R_{\theta JA}$ of 55.4°C/W for 25°C ambient temperature.

To ensure sufficient thermal flow, it is recommended to design with four thermal vias in applications enabling all four outputs at once.



M0029-01

Figure 8. Recommended Thermal Via Placement

See the *Quad Flatpack No-Lead Logic Packages (SCBA017)* and *QFN/SON PCB Attachment (SLUA271)* application reports for further package-related information.

APPLICATION INFORMATION

LVPECL RECEIVER INPUT TERMINATION

The input of the CDCP1803 has a high impedance and comes with a large common-mode voltage range.

For optimized noise performance, it is recommended to properly terminate the PCB trace (transmission line). If a differential signal drives the CDCP1803, then a 100- Ω termination resistor is recommended to be placed as close as possible across the input terminals. An even better approach is to install $2 \times 50\text{-}\Omega$ resistors, with the center tap connected to a capacitor (C) to terminate odd-mode noise and make up for transmission line mismatches. The VBB output can also be connected to the center tap to bias the input signal to ($V_{DD} - 1.3\text{ V}$) (see Figure 9).

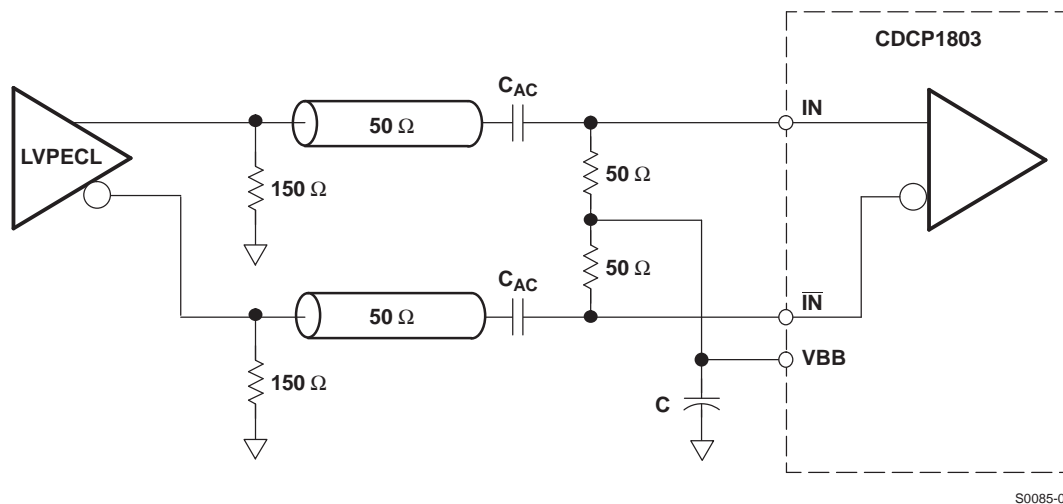


Figure 9. Recommended AC-Coupling LVPECL Receiver Input Termination

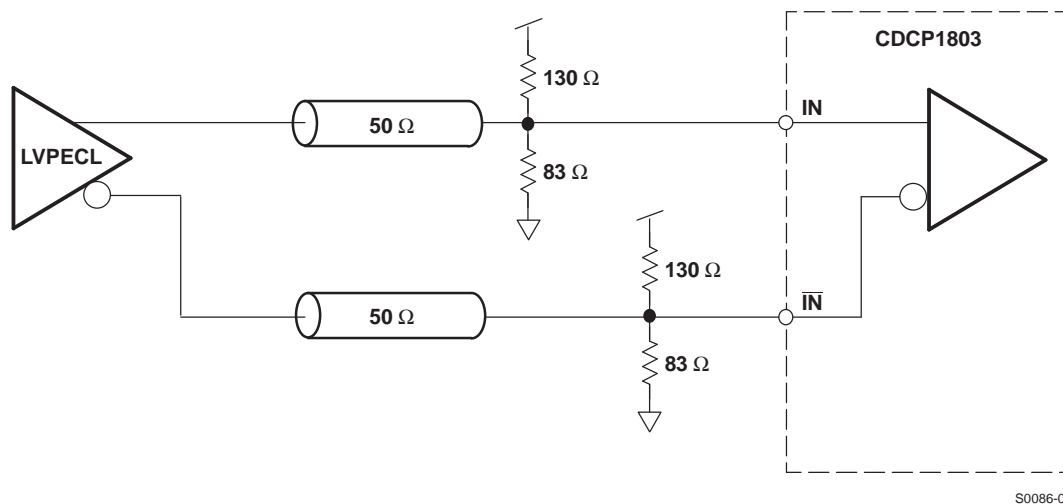
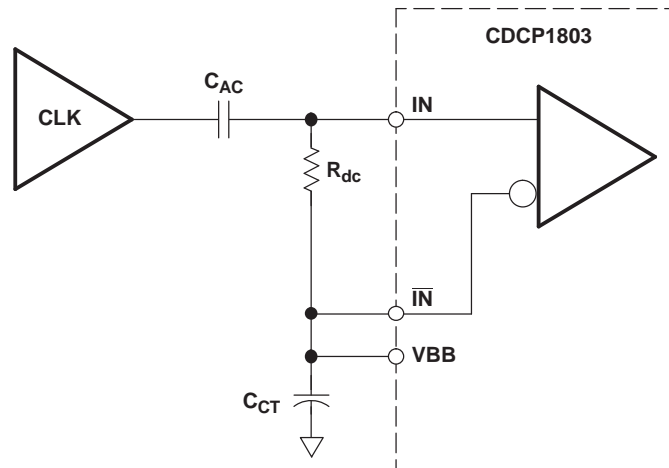


Figure 10. Recommended DC-Coupling LVPECL Receiver Input Termination

The CDCP1803 can also be driven by single-ended signals. Typically, the input signal becomes connected to one input, while the complementary input must be properly biased to the center voltage of the incoming input signal. For LVCMOS signals, this would be $V_{CC}/2$, realized by a simple voltage divider (e.g., two 10-k Ω resistors). The best option (especially if the dc offset of the input signal might vary) is to ac-couple the input signal and then rebias the signal using the VBB reference output. See Figure 11.

APPLICATION INFORMATION (continued)



NOTE: C_{AC} – AC-coupling capacitor (e.g., 10 nF)
 C_{CT} – Capacitor keeps voltage at \overline{IN} constant (e.g., 10 nF)
 R_{dc} – Load and correct duty cycle (e.g., 50 Ω)
VBB – Bias voltage output

S0087-02

Figure 11. Typical Application Setting for Single-Ended Input Signals Driving the CDCP1803

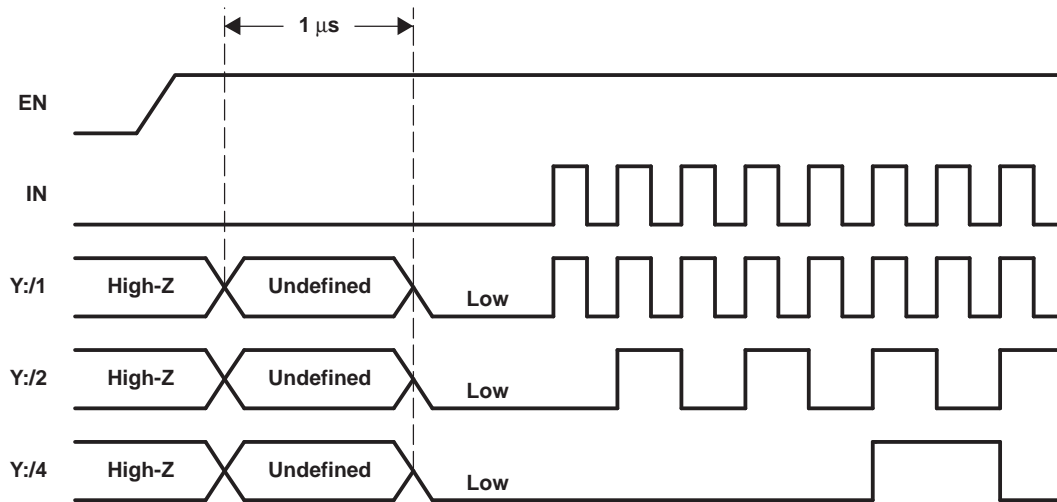
DEVICE BEHAVIOR DURING RESET AND CONTROL-TERMINAL SWITCHING

Output Behavior From Enabling the Device ($EN = 0 \rightarrow 1$)

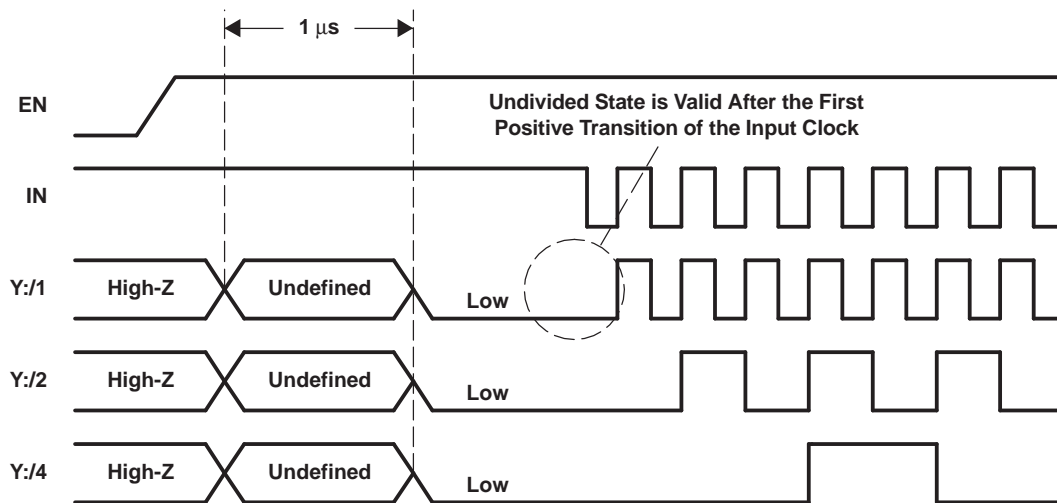
In disable mode ($EN = 0$), all output drivers are switched in high-Z mode. The S[2:0] control inputs are also switched off. In the same mode, all flip-flops are reset. The typical current consumption is below 500 μA .

When the device is enabled again, it takes typically 1 μs for the settling of the reference voltage and currents. During this time, the outputs Y[2:0] and \overline{Y} [2:0] drive a high signal. After the settle time, the outputs go into the low state. Due to the synchronization of each output driver signal with the input clock, the state of the waveforms after enabling the device is as shown in [Figure 12](#). The inverting input and output signal is not included. The Y:/1 waveform is the undivided output driver state.

APPLICATION INFORMATION (continued)



Signal State After the Device is Enabled (IN = Low)



Signal State After the Device is Enabled (IN = High)

T0068-01

Figure 12. Waveforms

APPLICATION INFORMATION (continued)

Enabling a Single Output Stage

If a single output stage becomes enabled:

- Y[2:0] is either low or high (undefined).
- $\overline{Y[2:0]}$ is the inverted signal of Y[2:0].

With the first positive clock transition, the undivided output becomes the input clock state. The divided output states are equal to the actual internal divider. The internal divider is not reset while enabling single output drivers.

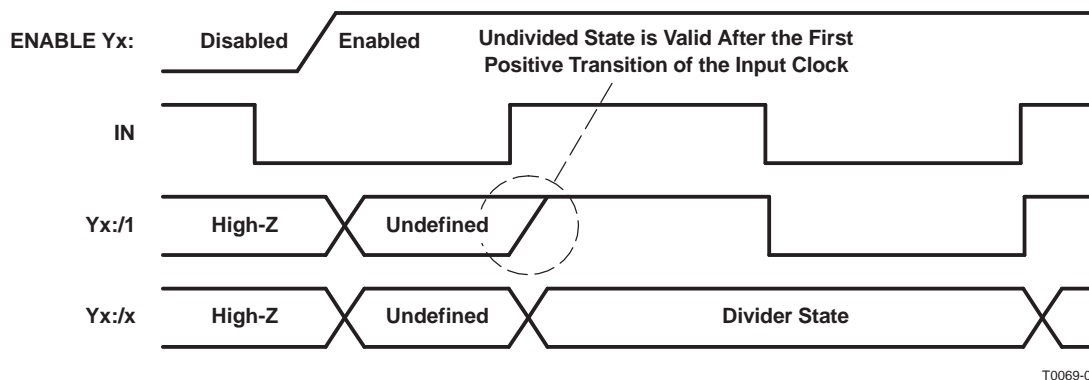


Figure 13. Signal State After an Output Driver Becomes Enabled While IN = 0

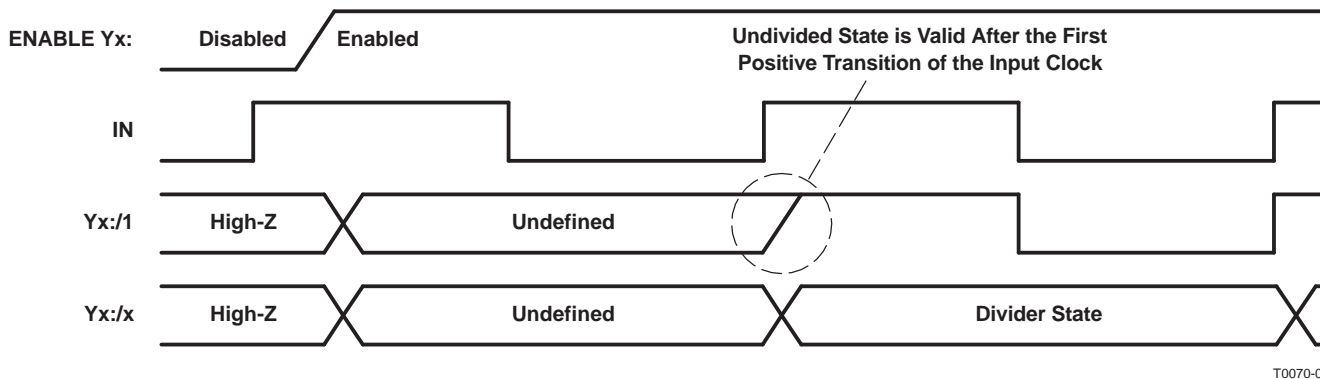


Figure 14. Signal State After an Output Driver Becomes Enabled While IN = 1

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
CDCP1803RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
CDCP1803RGERG4	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
CDCP1803RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	
CDCP1803RGETG4	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	
CDCP1803RTHR	OBSOLETE	VQFN	RTH	24		TBD	Call TI	Call TI	
CDCP1803RTHT	OBSOLETE	VQFN	RTH	24		TBD	Call TI	Call TI	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CDCP1803 :

- Enhanced Product: [CDCP1803-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCP1803RGER	VQFN	RGE	24	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
CDCP1803RGET	VQFN	RGE	24	250	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCP1803RGER	VQFN	RGE	24	3000	340.5	338.1	20.6
CDCP1803RGET	VQFN	RGE	24	250	340.5	338.1	20.6

THERMAL PAD MECHANICAL DATA

RGE (S-PVQFN-N24)

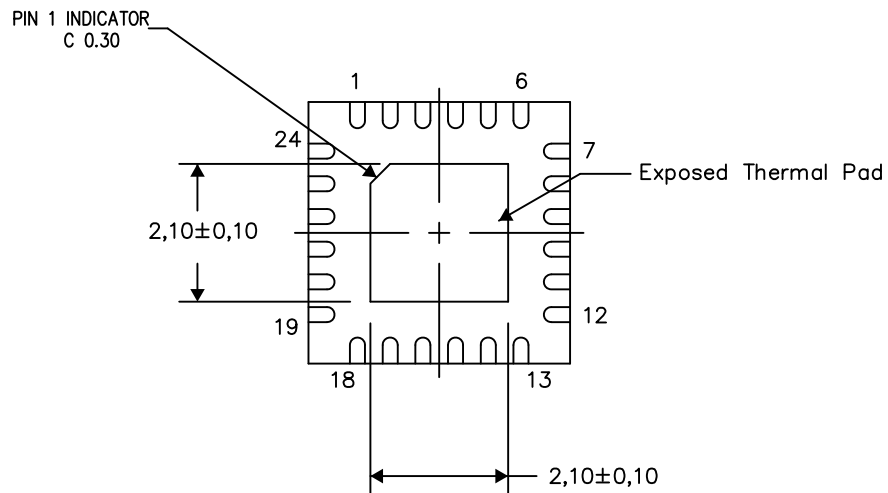
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

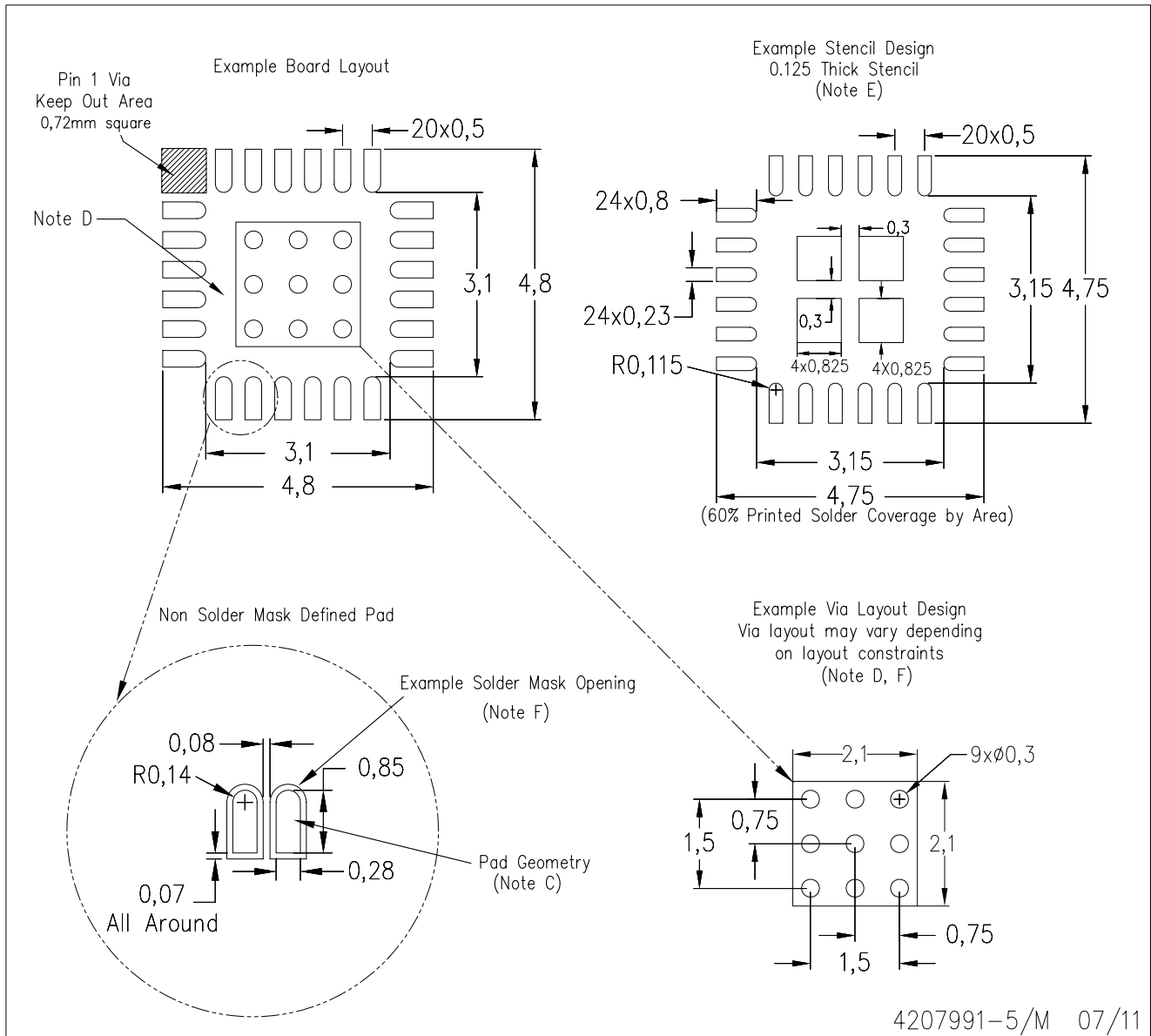
Exposed Thermal Pad Dimensions

4206344-6/AA 04/12

NOTES: A. All linear dimensions are in millimeters

RGE (S-PVQFN-N24)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46C and to discontinue any product or service per JESD48B. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components which meet ISO/TS16949 requirements, mainly for automotive use. Components which have not been so designated are neither designed nor intended for automotive use; and TI will not be responsible for any failure of such components to meet such requirements.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Mobile Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community e2e.ti.com