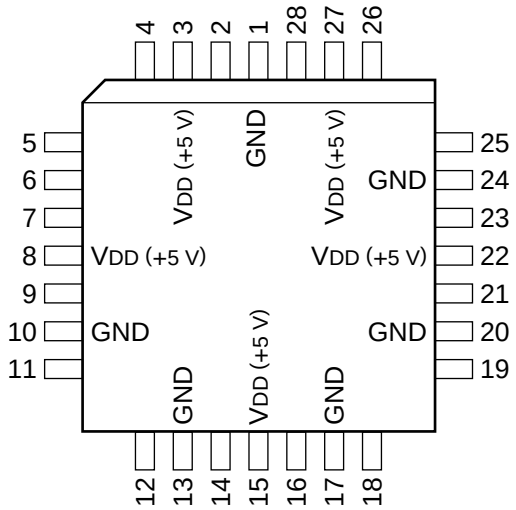
C-MOS CLOCK DRIVER

—TOP VIEW—



(VDD = +5 V)

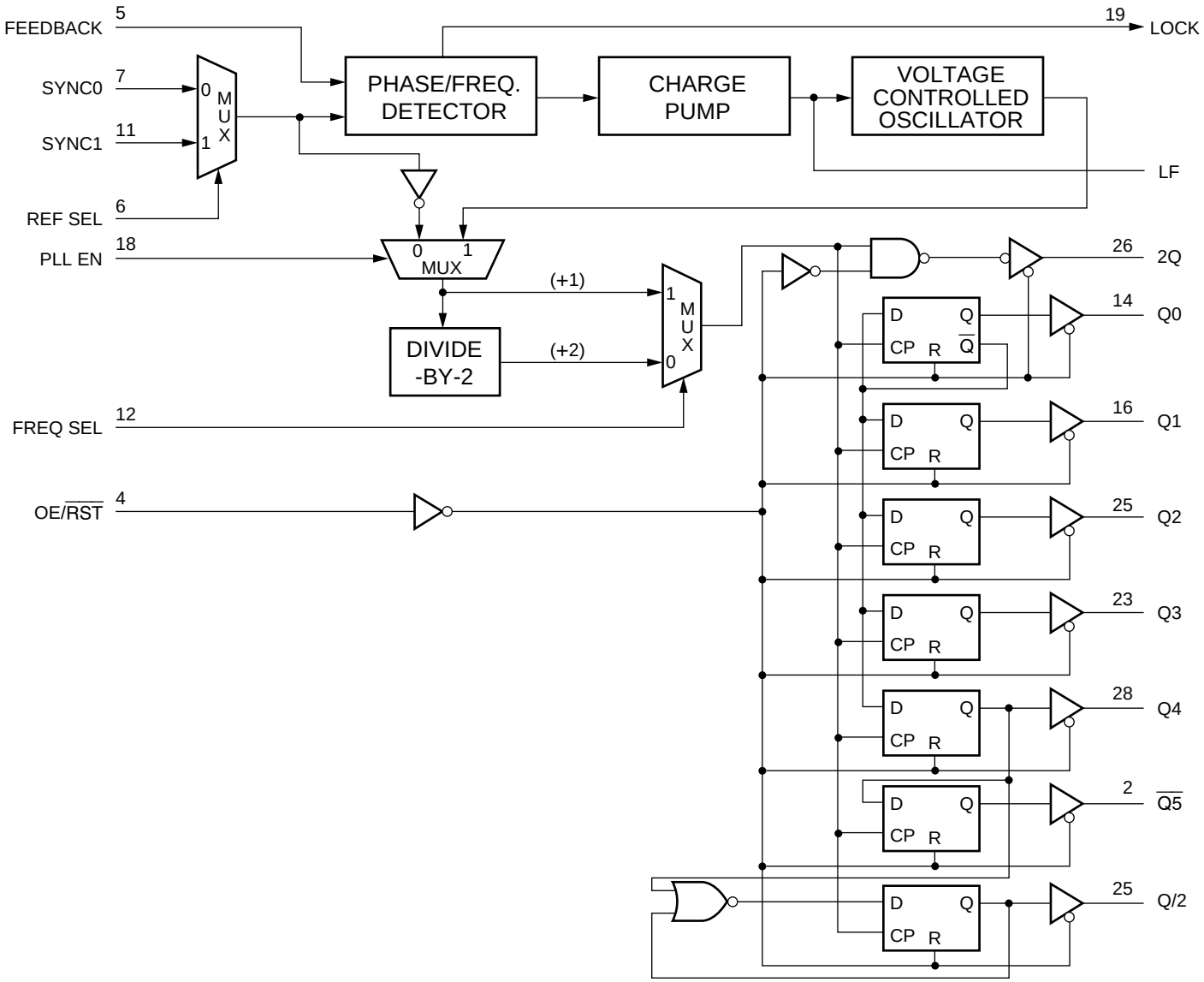
PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	GND	8	—	VDD	15	—	VDD	22	—	VDD
2	O	$\overline{Q5}$	9	I	LF	16	O	Q1	23	O	Q3
3	—	VDD	10	—	GND	17	—	GND	24	—	GND
4	I	OE/$\overline{RST}$	11	I	SYNC1	18	I	PLL EN	25	O	Q/2
5	I	FEEDBK	12	I	FREQ SEL	19	O	LOCK	26	O	2Q
6	I	REF SEL	13	—	GND	20	—	GND	27	—	VDD
7	I	SYNC0	14	O	Q0	21	O	Q2	28	O	Q4

INPUT

FEEDBK : FEEDBACK TO PHASE DETECTOR
FREQ SEL : ×1/×2 FREQUENCY SELECT
LF : EXTERNAL LOOP CAPACITOR
OE/$\overline{RST}$: OUTPUT ENABLE/ASYNCHRONOUS RESET
PLL EN : PHASE LOCKED LOOP ENABLE
REF SEL : SYNC0 OR SYNC1 SELECT
SYNC0, SYNC1 : REFERENCE CLOCK

OUTPUT

2Q : 2×Q CLOCK
LOCK : PHASE LOCK
Q/2 : Q/2 CLOCK
Q0 - Q4 : CLOCK
$\overline{Q5}$: INVERTED CLOCK


FEEDBACK
5
19
LOCK
SYNC0
7
SYNC1
11
0
1
MUX
PHASE/FREQ.
DETECTOR
CHARGE
PUMP
VOLTAGE
CONTROLLED
OSCILLATOR
LF
REF SEL
6
PLL EN
18
0
1
MUX
(+1)
(+2)
DIVIDE
-BY-2
1
0
MUX
FREQ SEL
12
OE/RST
4
D
Q
CP
R
26
2Q
14
Q0
16
Q1
25
Q2
23
Q3
28
Q4
2
Q5
25
Q/2