LM3691 High Accuracy, Miniature 1A, Step-Down DC-DC Converter for Portable Applications

Check for Samples: LM3691

FEATURES

- **V_{OUT} = 0.75V to 3.3V**
- **±1% DC Output Voltage Precision**
- **2.3V ≤ V_{IN} ≤ 5.5V**
- **4 MHz Switching Frequency**
- **64 µA (typ.) Quiescent Current in ECO Mode**
- **1A Maximum Load Capability**
- **Automatic ECO/PWM Mode Switching**
- **Mode Pin to Select ECO/Forced PWM Mode**
- **1 µH Inductor, 4.7 µF Input Capacitor (0603(1608) Case Size) and 4.7 µF Output Capacitor (0603(1608) Case Size)**
- **Current Overload and Thermal Shutdown Protections**
- **Only Three Tiny Surface-Mount External Components Required (Solution Size Less Than 15 mm^2)**

APPLICATIONS

- **Mobile Phones**
- **Hand-Held Radios**
- **MP3 Players**
- **Portable Hard Disk Drives**

DESCRIPTION

The LM3691 step-down DC-DC converter is optimized for powering ultra-low voltage circuits from a single Li-Ion cell or 3 cell NiMH/NiCd batteries. It provides up to 1A load current, over an input voltage range from 2.3V to 5.5V. There are several different fixed voltage output options available.

LM3691 has a mode-control pin that allows the user to select Forced PWM mode or ECO mode that changes modes between gated PWM mode and PWM automatically depending on the load. In ECO, LM3691 offers superior efficiency and very low I_q under light load conditions. ECO mode extends the battery life through reduction of the quiescent current during light load conditions and system standby.

The LM3691 is available in a 6-bump DSBGA package. Only three external surface-mount components, a 1 µH inductor, a 4.7 µF input capacitor and a 4.7 µF output capacitor, are required.

Typical Application Circuit

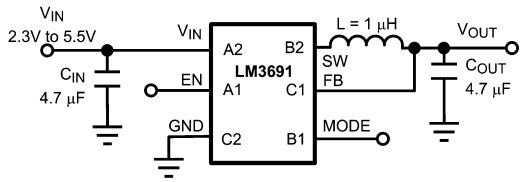

Figure 1. Typical Application Circuit

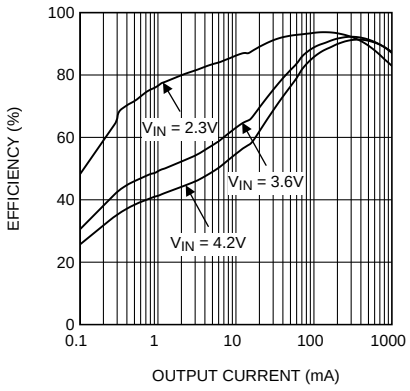

Figure 2. Efficiency vs. Output Current (V_{OUT} = 1.8V, ECO Mode)

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Connection Diagram

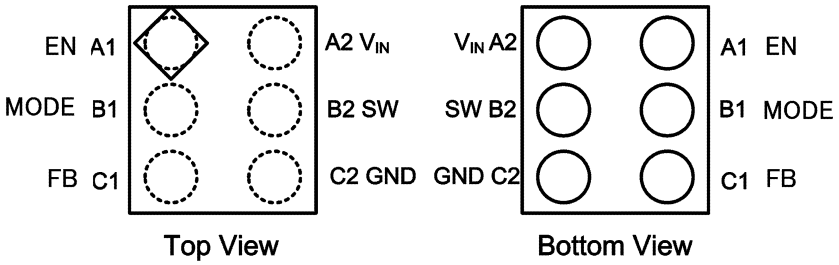

Figure 3. 6-Bump Thin DSBGA Package, Large Bump
See Package Number YZR0006LCA

PIN DESCRIPTIONS

Pin DSBGA	Name	Description
A1	**EN**	**Enable pin. The device is in shutdown mode when voltage to this pin is <0.4V and enabled when >1.2V.** **Do not leave this pin floating.**
B1	MODE	Mode Pin: Mode = 1, Forced PWM Mode = 0, ECO Do not leave this pin floating.
C1	FB	Feedback analog input. Connect directly to the output filter capacitor. (Figure 1)
A2	VIN	Power supply input. Connect to the input filter capacitor. (Figure 1)
B2	SW	Switching node connection to the internal PFET switch and NFET synchronous rectifier.
C2	GND	Ground pin.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)(2)

DSBGA PACKAGE	
ORDERABLE	**VOLTAGE OPTION (V)**
LM3691TL-0.75/NOPB	0.75
LM3691TLX-0.75/NOPB	
LM3691TL-1.0/NOPB	1
LM3691TLX-1.0/NOPB	
LM3691TL-1.2/NOPB	1.2
LM3691TLX-1.2/NOPB	
LM3691TL-1.5/NOPB	1.5
LM3691TLX-1.5/NOPB	
LM3691TL-1.8/NOPB	1.8
LM3691TLX-1.8/NOPB	
LM3691TL-2.5/NOPB	2.5
LM3691TLX-2.5/NOPB	
LM3691TL-3.3/NOPB	3.3
LM3691TLX-3.3/NOPB	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

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Absolute Maximum Ratings (1) (2)

V_{IN} Pin to GND	−0.2V to 6.0V
EN, MODE, FB, SW pins	(GND−0.2V) to V_{IN} + 0.2V
Junction Temperature (T_{J-MAX})	+150°C
Storage Temperature Range	−65°C to +150°C
Continuous Power Dissipation (3)	Internally Limited
Maximum Lead Temperature (Soldering, 10 sec.)	260°C
ESD Rating (4)	
Human Body Model	2 kV
Machine Model	200V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply performance limits. For performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typ.) and disengages at T_J = 130°C (typ.).
(4) The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin. MIL-STD-883 3015.7

Operating Ratings (1) (2)

Input Voltage Range	2.3V to 5.5V
Recommended Load Current	0 mA to 1000 mA
Junction Temperature (T_J) Range	−30°C to +125°C
Ambient Temperature (T_A) Range (3)	−30°C to +85°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply performance limits. For performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) In applications where high power dissipation and/or poor package resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature (T_{J-MAX}), the maximum power dissipation of the device in the application (P_{D-MAX}) and the junction to ambient thermal resistance of the package (θ_{JA}) in the application, as given by the following equation: $T_{A-MAX} = T_{J-MAX} - (\theta_{JA} \times P_{D-MAX})$. Due to the pulsed nature of testing the part, the temp in the Electrical Characteristic table is specified as $T_A = T_J$.

Thermal Properties

Junction-to-Ambient Thermal Resistance (θ_{JA}) (1) (DSBGA)	85°C/W

(1) Junction-to-ambient thermal resistance is highly application and board layout dependent. In applications where high power dissipation exists, special care must be given to thermal dissipation issues in board design.

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Electrical Characteristics (1) (2) (3)

Limits in standard typeface are for T_A = 25°C. Limits in **boldface** type apply over the operating ambient temperature range (−30°C ≤ T_A= T_J ≤ +85°C). Unless otherwise noted, specifications apply to the LM3691 open loop Typical Application Circuit with V_{IN} = EN = 3.6V.

Parameter		Test Conditions	Min	Typ	Max	Units
V_{FB}	Feedback Voltage	PWM Mode. No load V_{OUT} = 1.1V to 3.3V	**-1**		**+1**	%
		PWM Mode. No load V_{OUT} = 0.75V to 1.0V	**-10**		**+10**	mV
I_{SHDN}	Shutdown Supply Current	EN = 0V		0.03	**1**	µA
I_{Q_ECO}	ECO Mode I_q	ECO Mode		64	**80**	µA
I_{Q_PWM}	PWM Mode I_q	PWM Mode		490	**600**	µA
$R_{DSON\ (P)}$	Pin-Pin Resistance for PFET	V_{IN} = V_{GS} = 3.6V, I_O = 200 mA		160	**250**	mΩ
$R_{DSON\ (N)}$	Pin-Pin Resistance for NFET	V_{IN} = V_{GS} = 3.6V, I_O = −200 mA		115	**180**	mΩ
I_{LIM}	Switch Peak Current Limit	Open loop	**1250**	1500	**1700**	mA
V_{IH}	Logic High Input		**1.2**			V
V_{IL}	Logic Low Input				**0.4**	V
$I_{EN,MODE}$	Input Current			0.01	**1**	µA
F_{SW}	Switching Frequency	PWM Mode	**3.6**	4	**4.4**	MHz
V_{ON}	UVLO threshold (4)	V_{IN} rising		2.2	2.29	V
		V_{IN} falling		2.1		V
$T_{STARTUP}$	Start Time (5)		70	145	300	µs

(1) All voltages are with respect to the potential at the GND pin.
(2) Min and Max limits are specified by design, test or statistical analysis. Typical numbers represent the most likely norm.
(3) The parameters in the electrical characteristic table are tested under open loop conditions at V_{IN} = 3.6V unless otherwise specified. For performance over the input voltage range and closed loop condition, refer to the datasheet curves.
(4) The UVLO rising threshold minus the falling threshold is always positive.
(5) Specified by design. Not production tested.

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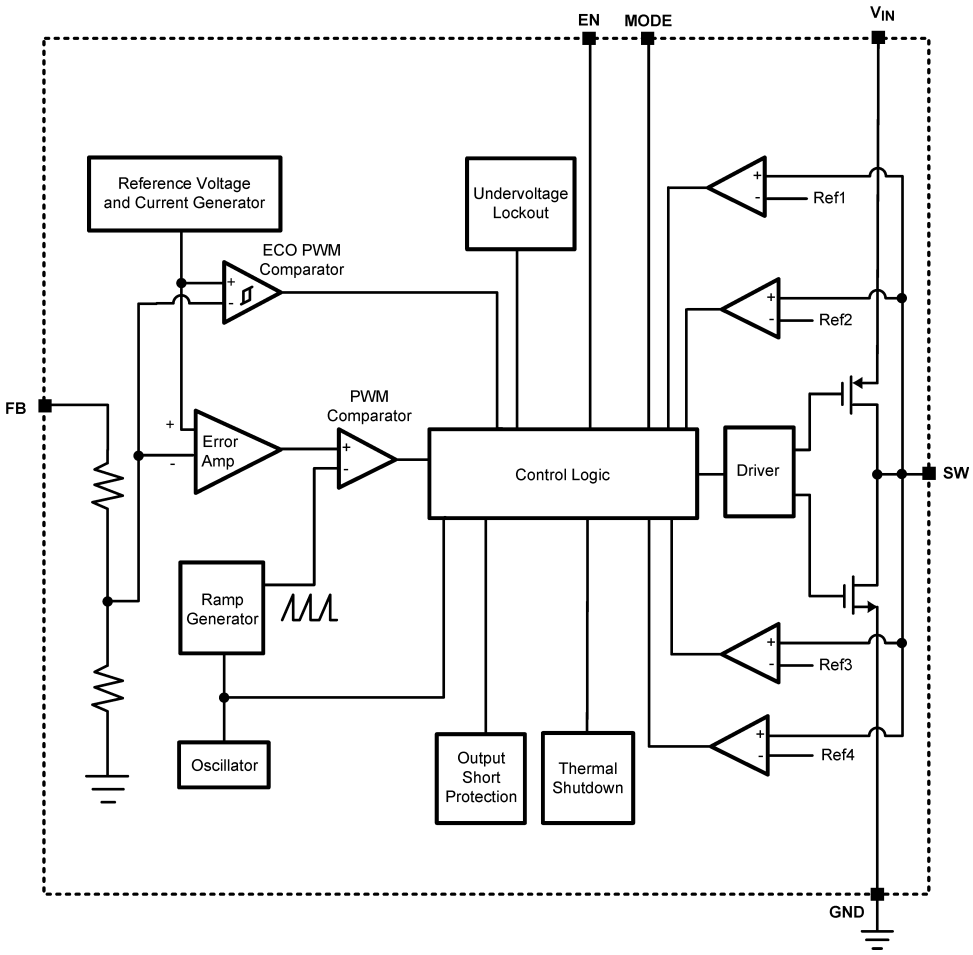
Block Diagram



Typical Performance Characteristics

LM3691TL Typical Application Circuit (page 1), V_{IN} = 3.6V, V_{OUT} = 1.8V, T_A = 25°, L = 1.0 µH, 2520, (LQM2HP1R0), C_{IN} = C_{OUT} = 4.7 µF, 0603(1608), 6.3V, (C1608X5R0J475K) unless otherwise noted.

Quiescent Supply current vs. Supply Voltage No Switching (ECO Mode)

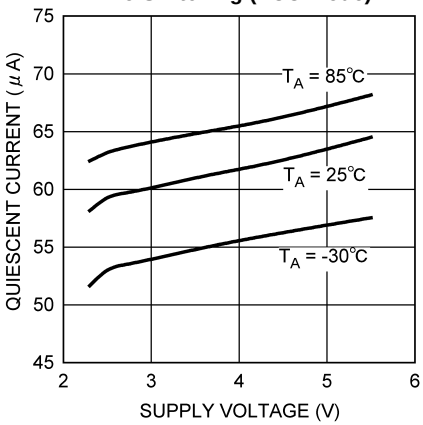


Figure 4.

Quiescent Supply current vs. Supply Voltage No Switching (PWM Mode)

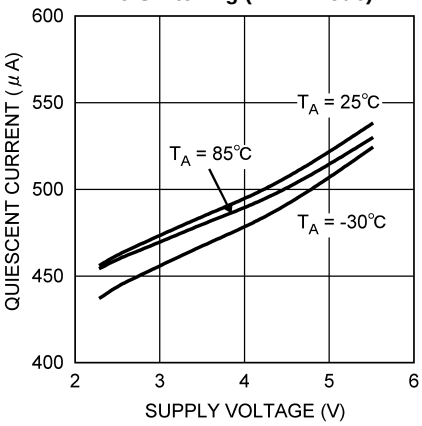


Figure 5.

Shutdown Current vs. Temp (V_{OUT} = 1.8V)

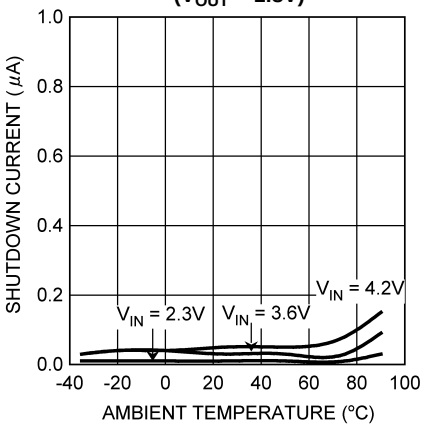


Figure 6.

Switching Frequency vs. Temp (V_{OUT} = 1.8V, PWM Mode)

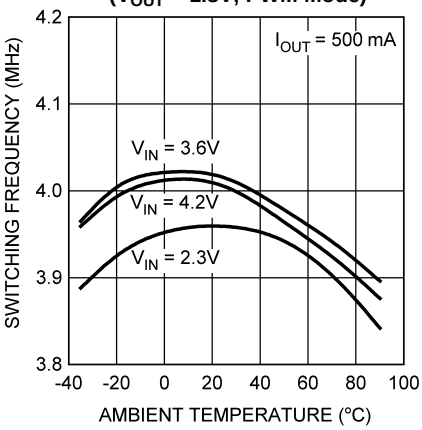


Figure 7.

Output Voltage vs. Supply Voltage (V_{OUT} = 0.75V)

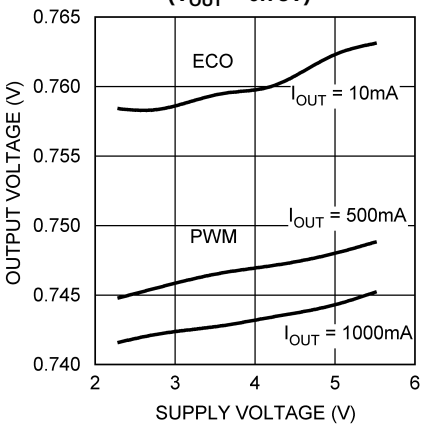


Figure 8.

Output Voltage vs. Supply Voltage (V_{OUT} = 1.8V)

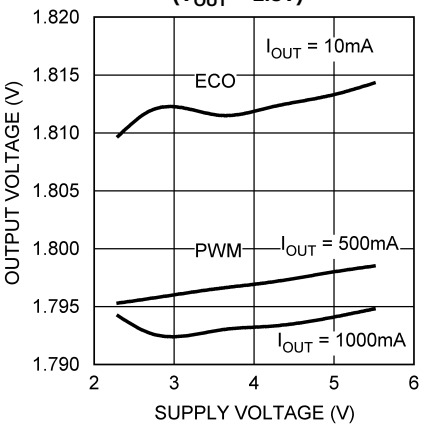


Figure 9.

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Typical Performance Characteristics (continued)

LM3691TL Typical Application Circuit (page 1), V_{IN} = 3.6V, V_{OUT} = 1.8V, T_A = 25°, L = 1.0 µH, 2520, (LQM2HP1R0), C_{IN} = C_{OUT} = 4.7 µF, 0603(1608), 6.3V, (C1608X5R0J475K) unless otherwise noted.

Output Voltage vs. Output Current (V_{OUT} = 0.75V)

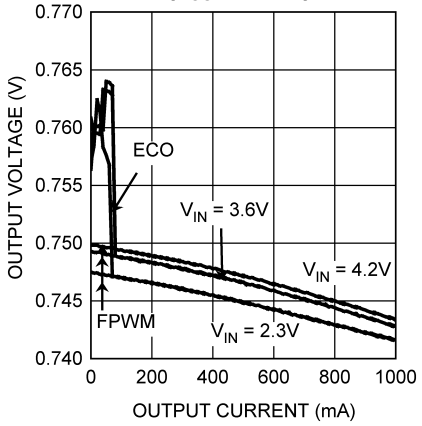

Figure 10.

Output Voltage vs. Output Current (V_{OUT} = 1.8V)

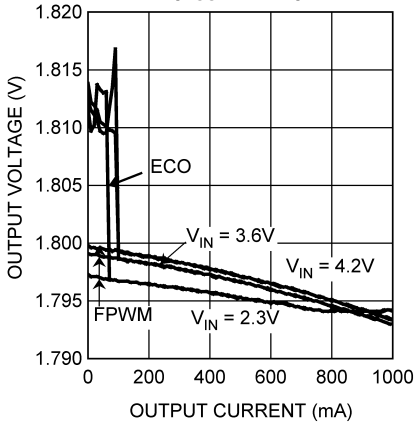

Figure 11.

Input Current vs. Output Current (V_{OUT} = 0.75V)

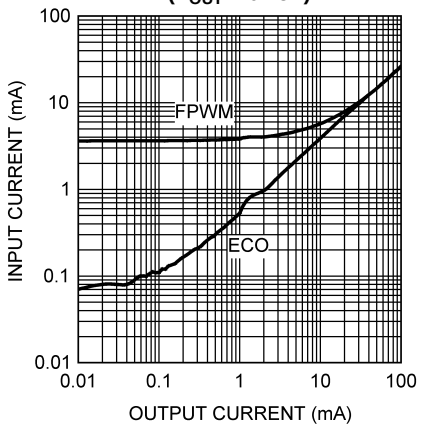

Figure 12.

Input Current vs. Output Current (V_{OUT} = 1.8V)

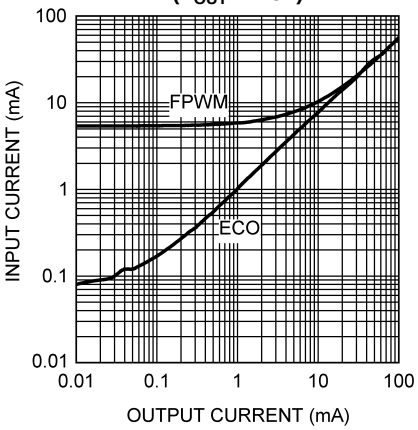

Figure 13.

Efficiency vs. Output Current (V_{OUT} = 0.75V, ECO Mode)

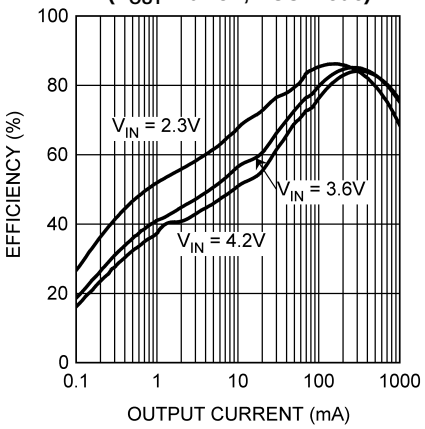

Figure 14.

Efficiency vs. Output Current (V_{OUT} = 1.8V, ECO Mode)

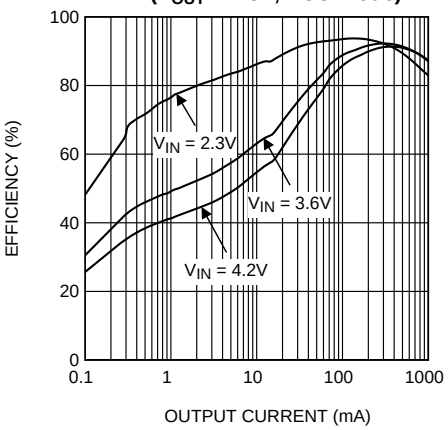

Figure 15.

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Typical Performance Characteristics (continued)

LM3691TL Typical Application Circuit (page 1), V_{IN} = 3.6V, V_{OUT} = 1.8V, T_A = 25°, L = 1.0 µH, 2520, (LQM2HP1R0), C_{IN} = C_{OUT} = 4.7 µF, 0603(1608), 6.3V, (C1608X5R0J475K) unless otherwise noted.

Efficiency vs. Output Current (V_{OUT} = 2.5V, ECO Mode)

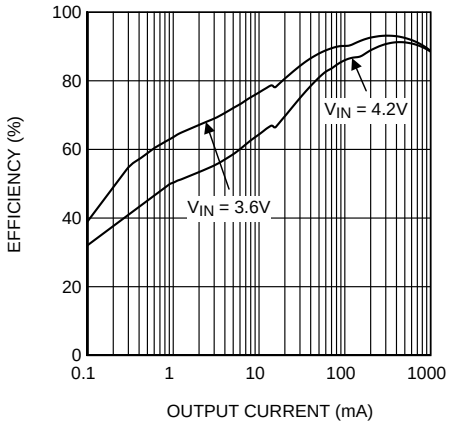

Figure 16.

Efficiency vs. Output Current (V_{OUT} = 0.75V, FPWM Mode)

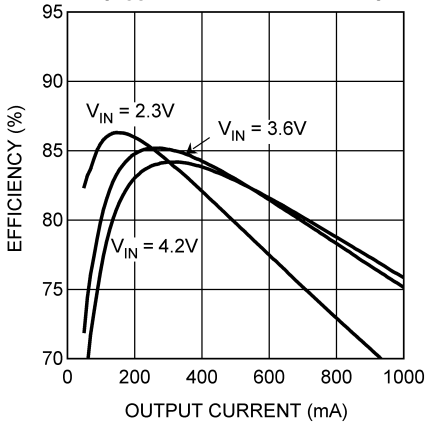

Figure 17.

Efficiency vs. Output Current (V_{OUT} = 1.8V, FPWM Mode)

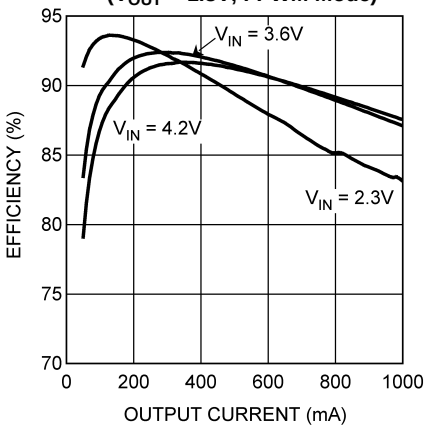

Figure 18.

Efficiency vs. Output Current (V_{OUT} = 2.5V, FPWM Mode)

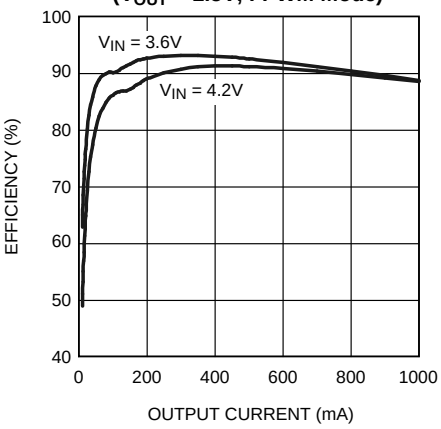

Figure 19.

Load Current Threshold vs. Supply Voltage (V_{OUT} = 0.75V, ECO Mode to PWM Mode)

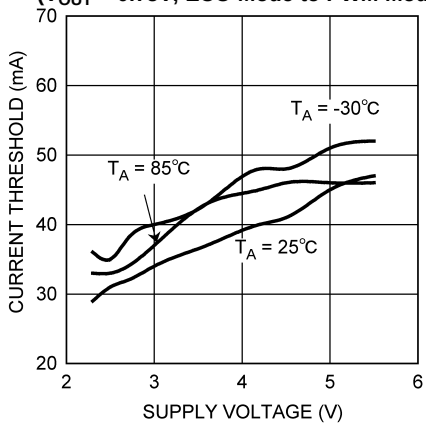

Figure 20.

Load Current Threshold vs. Supply Voltage (V_{OUT} = 1.8V, ECO Mode to PWM Mode)

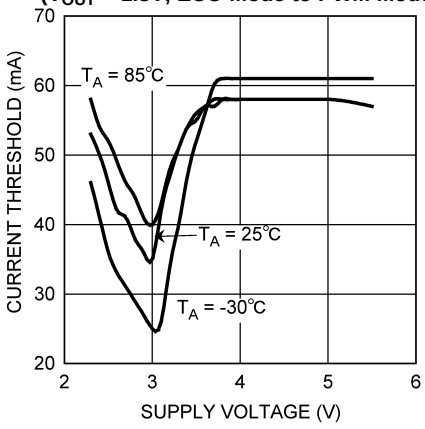

Figure 21.

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Typical Performance Characteristics (continued)

LM3691TL Typical Application Circuit (page 1), V_{IN} = 3.6V, V_{OUT} = 1.8V, T_A = 25°, L = 1.0 µH, 2520, (LQM2HP1R0), C_{IN} = C_{OUT} = 4.7 µF, 0603(1608), 6.3V, (C1608X5R0J475K) unless otherwise noted.

Output Voltage Ripple vs. Supply Voltage (V_{OUT} = 0.75V)

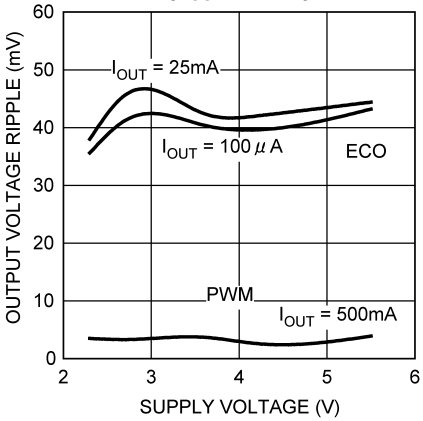

Figure 22.

Output Voltage Ripple vs. Supply Voltage (V_{OUT} = 1.8V)

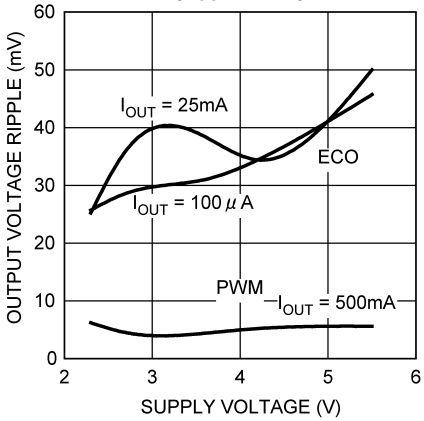

Figure 23.

Closed Loop Current Limit vs. Temperature (V_{OUT} = 0.75V)

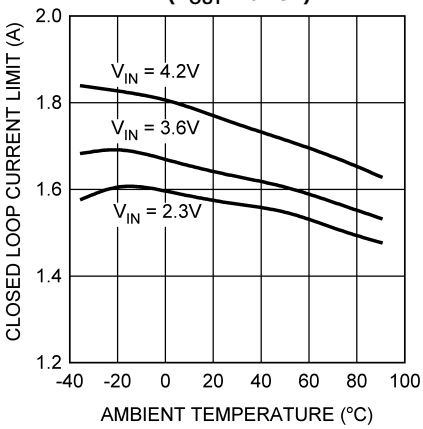

Figure 24.

Closed Loop Current Limit vs. Temperature (V_{OUT} = 1.8V)

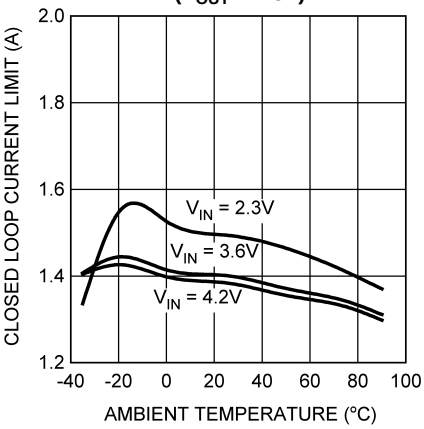

Figure 25.

Line Transient Reponse (V_{OUT} = 0.75V, PWM Mode)

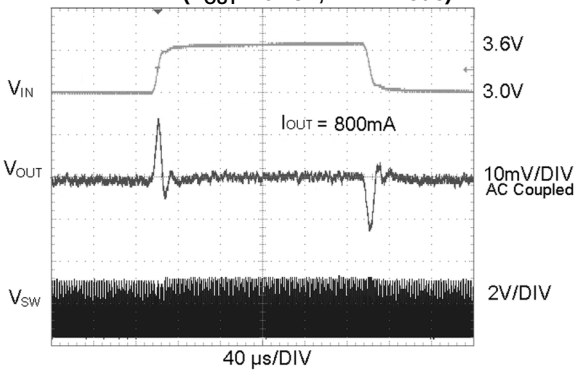

Figure 26.

Line Transient Reponse (V_{OUT} = 1.8V, PWM Mode)

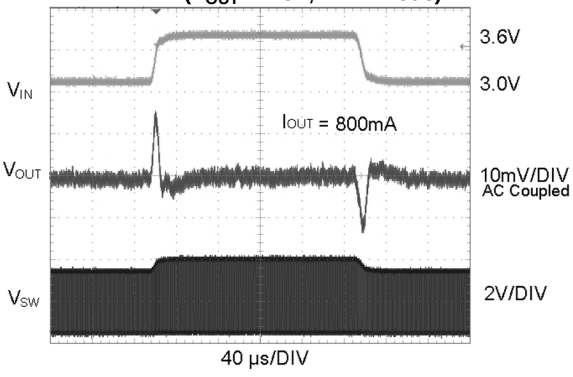

Figure 27.

Typical Performance Characteristics (continued)

LM3691TL Typical Application Circuit (page 1), V_{IN} = 3.6V, V_{OUT} = 1.8V, T_A = 25°, L = 1.0 µH, 2520, (LQM2HP1R0), C_{IN} = C_{OUT} = 4.7 µF, 0603(1608), 6.3V, (C1608X5R0J475K) unless otherwise noted.

Load Transient Reponse (V_{OUT} = 0.75V, ECO Mode 1mA to 25 mA)

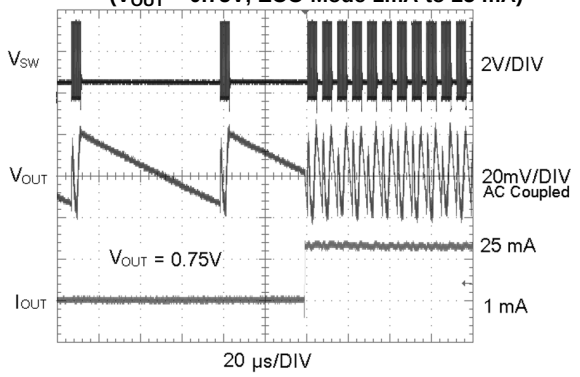

Figure 28.

Load Transient Reponse (V_{OUT} = 0.75V, ECO Mode 25 mA to 1mA)

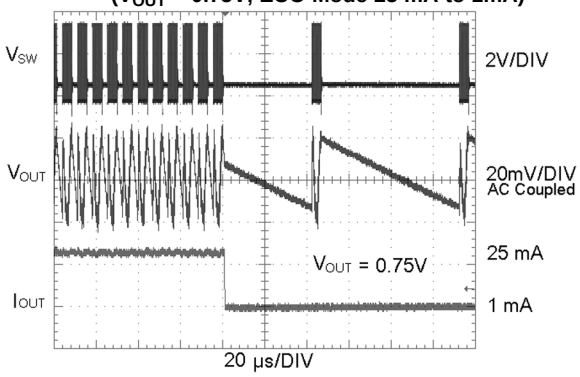

Figure 29.

Load Transient Reponse (V_{OUT} = 1.8V, ECO Mode 1mA to 25 mA)

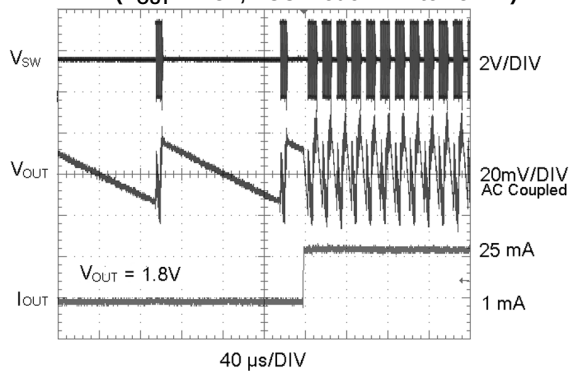

Figure 30.

Load Transient Reponse (V_{OUT} = 1.8V, ECO Mode 25 mA to 1mA)

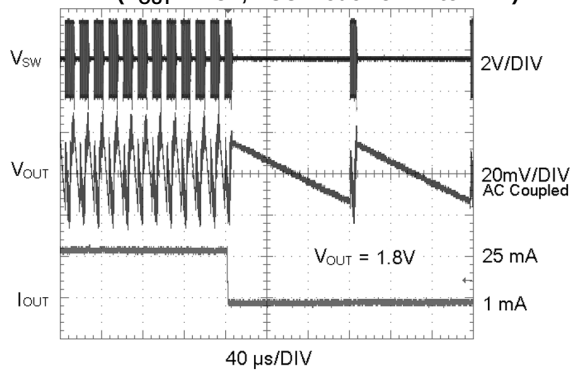

Figure 31.

Load Transient Reponse (V_{OUT} = 0.75V, ECO Mode to PWM Mode)

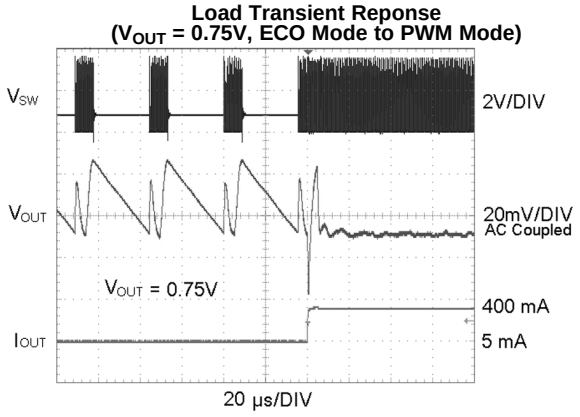

Figure 32.

Load Transient Reponse (V_{OUT} = 0.75V, PWM Mode to ECO Mode)

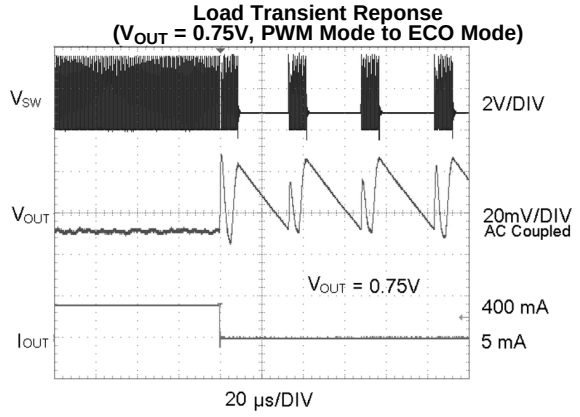

Figure 33.

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Typical Performance Characteristics (continued)

LM3691TL Typical Application Circuit (page 1), V_{IN} = 3.6V, V_{OUT} = 1.8V, T_A = 25°, L = 1.0 µH, 2520, (LQM2HP1R0), C_{IN} = C_{OUT} = 4.7 µF, 0603(1608), 6.3V, (C1608X5R0J475K) unless otherwise noted.

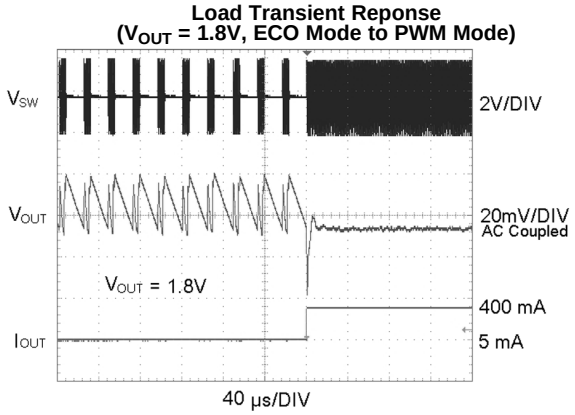

Figure 34.

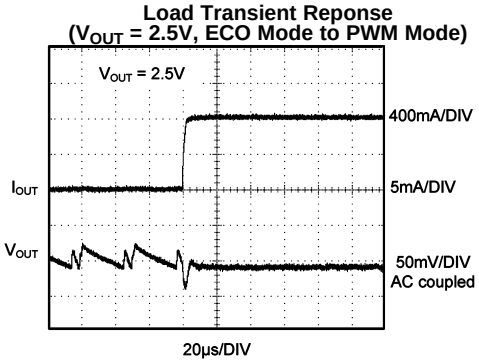

Figure 35.

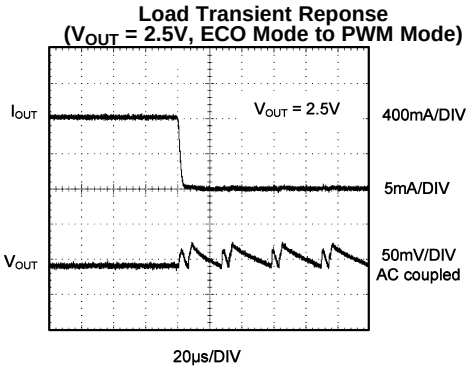

Figure 36.

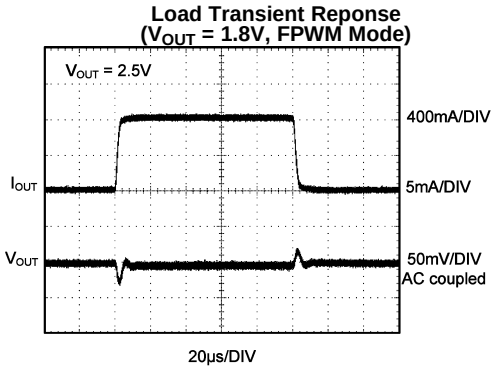

Figure 37.

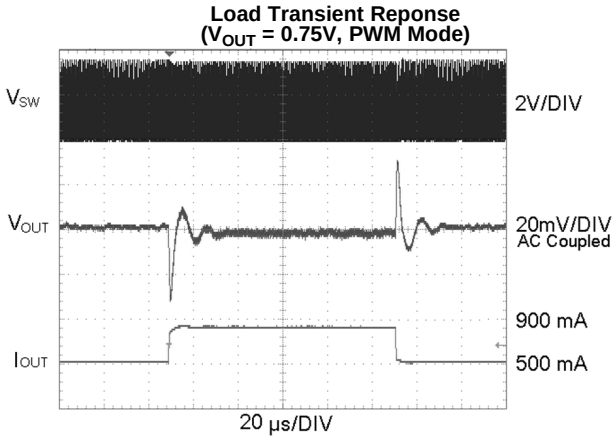

Figure 38.

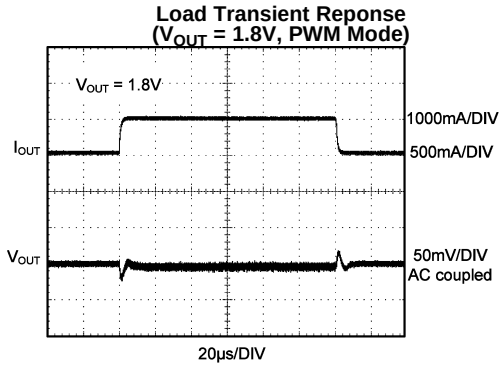

Figure 39.

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Typical Performance Characteristics (continued)

LM3691TL Typical Application Circuit (page 1), V_{IN} = 3.6V, V_{OUT} = 1.8V, T_A = 25°, L = 1.0 µH, 2520, (LQM2HP1R0), C_{IN} = C_{OUT} = 4.7 µF, 0603(1608), 6.3V, (C1608X5R0J475K) unless otherwise noted.

Load Transient Reponse (V_{OUT} = 2.5V, PWM Mode)

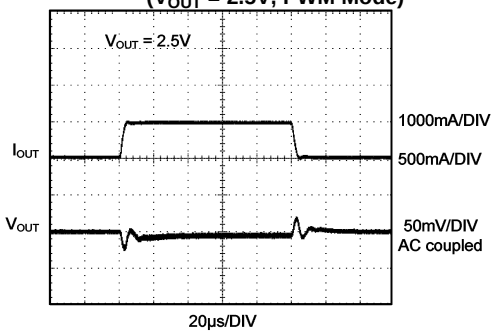

Figure 40.

Start Up into ECO Mode (V_{OUT} = 0.75V, R_{OUT} = 750Ω)

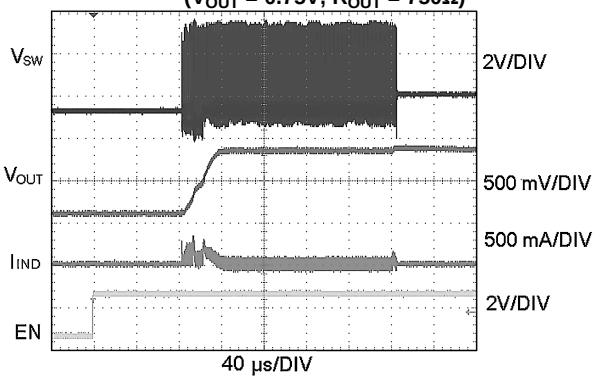

Figure 41.

Start Up into PWM Mode (V_{OUT} = 0.75V, R_{OUT} = 2.5Ω)

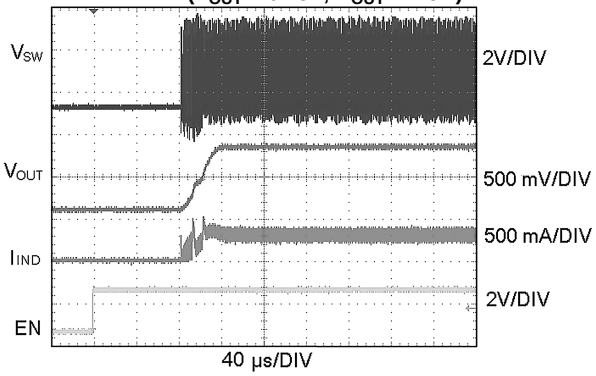

Figure 42.

Start Up into ECO Mode (V_{OUT} = 1.8V, R_{OUT} = 1.8 kΩ)

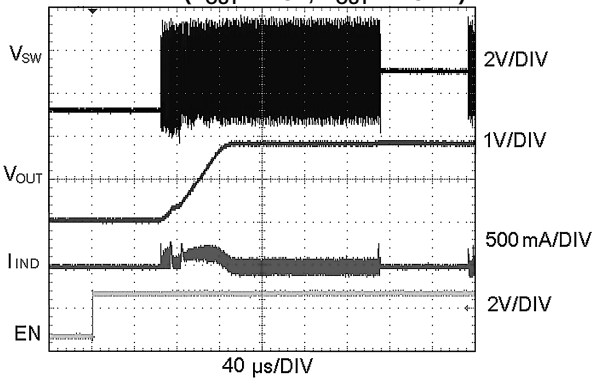

Figure 43.

Start Up into PWM Mode (V_{OUT} = 1.8V, R_{OUT} = 6Ω)

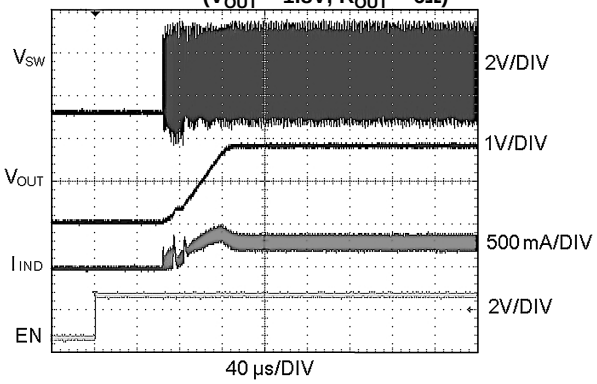

Figure 44.

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OPERATION DESCRIPTION

DEVICE INFORMATION

The LM3691, a high-efficiency, step-down DC-DC switching buck converter, delivers a constant voltage from either a single Li-Ion or three cell NiMH/NiCd battery to portable devices such as cell phones and PDAs. Using a voltage mode architecture with synchronous rectification, the LM3691 has the ability to deliver up to 1000 mA depending on the input voltage and output voltage, ambient temperature, and the inductor chosen.

There are three modes of operation depending on the current required - PWM (Pulse Width Modulation), ECO, and shutdown. The device operates in PWM mode at load currents of approximately 50 mA (typ.) or higher. Lighter output current loads cause the device to automatically switch into ECO mode for reduced current consumption and a longer battery life. Shutdown mode turns off the device, offering the lowest current consumption ($I_{SHUTDOWN}$ = 0.03 µA typ.). Additional features include soft-start, under voltage protection, current overload protection, and thermal shutdown protection. As shown in Figure 1, only three external power components are required for implementation.

CIRCUIT OPERATION

The LM3691 operates as follows. During the first portion of each switching cycle, the control block in the LM3691 turns on the internal PFET switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of (V_{IN}–V_{OUT})/L, by storing energy in a magnetic field. During the second portion of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. The inductor draws current from ground through the NFET to the output filter capacitor and load, which ramps the inductor current down with a slope of –V_{OUT}/L.

The output filter stores charge when the inductor current is high, and releases it when low, smoothing the voltage across the load. The output voltage is regulated by modulating the PFET switch on time to control the average current sent to the load. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the switch and synchronous rectifier at the SW pin to a low-pass filter formed by the inductor and output filter capacitor. The output voltage is equal to the average voltage at the SW pin.

PWM OPERATION

During PWM operation, the converter operates as a voltage-mode controller with input voltage feed forward. This allows the converter to achieve excellent load and line regulation. The DC gain of the power stage is proportional to the input voltage. To eliminate this dependence, feed forward inversely proportional to the input voltage is introduced. While in PWM mode, the output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control power to the load. At the beginning of each clock cycle the PFET switch is turned on and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator can also turn off the switch in case the current limit of the PFET is exceeded. Then the NFET switch is turned on and the inductor current ramps down. The next cycle is initiated by the clock turning off the NFET and turning on the PFET.

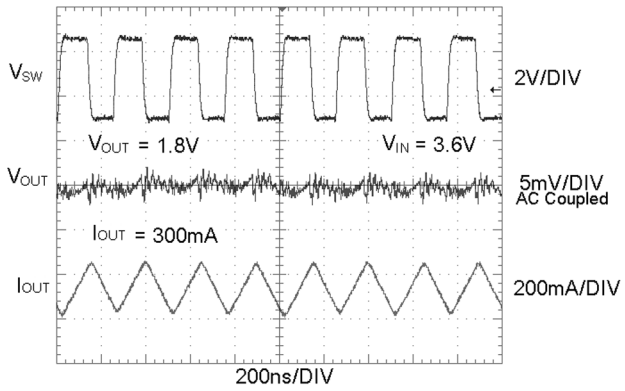

Figure 45. Typical PWM Operation

Internal Synchronous Rectification

While in PWM mode, the LM3691 uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

Current Limiting

A current limit feature allows the LM3691 to protect itself and external components during overload conditions. PWM mode implements current limit using an internal comparator that trips at 1500 mA (typ). If the output is shorted to ground and output voltage becomes lower than 0.3V (typ.), the device enters a timed current limit mode where the switching frequency will be one fourth, and NFET synchronous rectifier is disabled, thereby preventing excess current and thermal runaway.

ECO OPERATION

Setting mode pin low places the LM3691 in Auto mode. By doing so the part switches from ECO (ECOnomy) state to FPWM (Forced Pulse Width Modulation) state based on output load current. At light loads (less than 50 mA), the converter enters ECO mode. In this mode the part operates with low Iq. During ECO operation, the converter positions the output voltage slightly higher (+30 mV typ.) than the nominal output voltage in FPWM operation. Because the reference is set higher, the output voltage increases to reach the target voltage when the part goes from sleep state to switching state. Once this voltage is reached the converter enters sleep mode, thereby reducing switching losses and improving light load efficiency. The output voltage ripple is slightly higher in ECO mode (30 mV peak–peak ripple typ.).

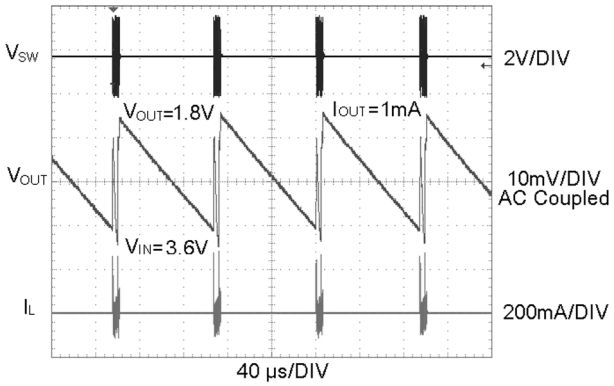

Figure 46. Typical ECO Operation

FORCED PWM MODE

Setting Mode pin high (>1.2V) places the LM3691 in Forced PWM. The part is in forced PWM regardless of the load.

SHUTDOWN MODE

Setting the EN input pin low (<0.4V) places the LM3691 in shutdown mode. During shutdown the PFET switch, NFET switch, reference, control and bias circuitry of the LM3691 are turned off. Setting EN high (>1.2V) enables normal operation. When turning on the device with EN soft-start is activated. EN pin should be set low to turn off the LM3691 during system power up and under-voltage conditions when the supply is less than 2.3V. Do not leave the EN pin floating.

SOFT-START

The LM3691 has a soft-start circuit that limits in-rush current during startup. Output voltage increase rate is 30 mV/µsec (at V_{OUT} = 1.8V typ.) during soft-start.

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THERMAL SHUTDOWN PROTECTION

The LM3691 has a thermal overload protection function that operates to protect itself from short-term misuse and overload conditions. When the junction temperature exceeds around 150°C, the device inhibits operation. Both the PFET and the NFET are turned off. When the temperature drops below 130°C, normal operation resumes. Prolonged operation in thermal overload conditions may damage the device and is considered bad practice.

OVER-TEMPERATURE MAXIMUM LOAD RECOMMENDATIONS

VIN	Maximum Load
2.5V to 5.5V	1000 mA
2.3V to 2.5V	650 mA

APPLICATION INFORMATION

INDUCTOR SELECTION

DC bias current characteristics of inductors must be considered. Different manufacturers follow different saturation current rating specifications, so attention must be given to details. DC bias curves should be requested from them as part of the inductor selection process.

Minimum value of inductance to specify good performance is 0.5 µH at 1.5A (I_{LIM} typ.) bias current over the ambient temp range. The inductor's DC resistance should be less than 0.1Ω for good efficiency at high current condition. The inductor AC loss (resistance) also affects conversion efficiency. Higher Q factor at switching frequency usually gives better efficiency at light load to middle load.

Table 1 lists suggested inductors and suppliers.

INPUT CAPACITOR SELECTION

A ceramic input capacitor of 4.7 µF, 6.3V/10V is sufficient for most applications. Place the input capacitor as close as possible to the V_{IN} pin and GND pin of the device. A larger value or higher voltage rating may be used to improve input voltage filtering. Use X7R, X5R or B types; do not use Y5V or F. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0402. **Minimum input capacitance to ensure good performance is 2.2 µF at maximum input voltage DC bias including tolerances and over ambient temp range.**

The input filter capacitor supplies current to the PFET (high-side) switch in the first half of each cycle and reduces voltage ripple imposed on the input power source. A ceramic capacitor's low ESR provides the best noise filtering of the input voltage spikes due to this rapidly changing current. Select an input filter capacitor with sufficient ripple current rating. The input current ripple can be calculated as:

$$I_{RMS} = I_{OUTMAX} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}} + \frac{r^2}{12}\right)}$$

$$r = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{L \times f \times I_{OUTMAX} \times V_{IN}}$$

(1)

OUTPUT CAPACITOR SELECTION

Use a 4.7µF, 6.3V ceramic capacitor, X7R, X5R or B types; do not use Y5V or F. DC bias voltage characteristics of ceramic capacitors must be considered. DC bias characteristics vary from manufacturer to manufacturer, and DC bias curves should be requested from them as part of the capacitor selection process. The output filter capacitor smooths out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR to perform these functions. **Minimum output capacitance to specify good performance is 2.2 µF at the output voltage DC bias including tolerances and over ambient temp range.**

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The output voltage ripple is caused by the charging and discharging of the output capacitor and also due to its R_{ESR} and can be calculated as:

Voltage peak-to-peak ripple due to capacitance =

$$V_{PP-C} = \frac{I_{RIPPLE}}{4*f*C} \quad (2)$$

Voltage peak-to-peak ripple due to ESR =

$$V_{PP-ESR} = (2 * I_{RIPPLE}) * R_{ESR} \quad (3)$$

Because these two components are out of phase the rms value can be used to get an approximate value of peak-to-peak ripple.

Voltage peak-to-peak ripple, root mean squared =

$$V_{PP-RMS} = \sqrt{V_{PP-C}^2 + V_{PP-ESR}^2} \quad (4)$$

Note that the output voltage ripple is dependent on the current ripple and the equivalent series resistance of the output capacitor (R_{ESR}). The R_{ESR} is frequency dependent (as well as temperature dependent); make sure the value used for calculations is at the switching frequency of the part.

Table 2 lists suggested capacitors and suppliers.

Table 1. Suggested Inductors and Their Suppliers

Model	Vendor	Dimensions LxWxH (mm)	D.C.R (mΩ)
LQM2HPN1R0MG0	Murata	2.5 x 2.0 x 1.0	55
MLP2520S1R0L	TDK	2.5 x 2.0 x 1.0	60
KSLI252010BG1R0	HItachi Metals	2.5 x 2.0 x 1.0	80
MIPSZ2012D1R0	FDK	2.0 x 1.25 x 1.0	90

Table 2. Suggested Capacitors and Their Suppliers

Model	Type	Vendor	Voltage Rating (V)	Case Size Inch (mm)
4.7 µF for C_{IN} and C_{OUT}				
C1608X5R0J475K	Ceramic	TDK	6.3	0603 (1608)
C1608X5R1A475K	Ceramic	TDK	10.0	0603 (1608)

PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter IC, resulting in poor regulation or instability. In particular parasitic inductance from extra-long PCB trace lengths can cause additional noise voltages through L*di/dt that adversely affect the DC-DC converter IC circuitry. Good layout for the LM3691 can be implemented by following a few simple design rules.

1. Place the inductor and filter capacitors close together and make the traces short. The traces between these components carry relatively high switching currents and act as antennas. Following this rule reduces radiated noise.
2. Place the capacitors and inductor close to the LM3691. Place the C_{IN} capacitor as close as possible to the V_{IN} and GND pads. Place the C_{OUT} capacitor as close as possible to the VOUT and GND connections.
3. Arrange the components so that the switching current loops curl in the same direction. During the first half of each cycle, current flows from the input filter capacitor, through the buck and inductor to the output filter capacitor and back through ground, forming a current loop. In the second half of each cycle, current is pulled up from ground, through the buck by the inductor, to the output filter capacitor and then back through ground, forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
4. Connect the ground pins of the buck and filter capacitors together using generous component-side copper fill as a pseudo-ground plane. Connect this to the ground-plane (if one is used) with several vias. This reduces

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ground-plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at the buck by giving it a low-impedance ground connection.

5. Use wide traces between the power components and for power connections to the DC-DC converter circuit. This reduces voltage errors by resistive losses across the traces. Even 1mm of fine trace creates parasitic inductance that can undesirably affect performance from increased L*di/dt noise voltages.
6. Route noise sensitive traces, such as the voltage feedback path, away from noisy traces between the power components. The voltage feedback trace must remain close to the buck circuit and should be routed directly from FB to VOUT at the output capacitor and should be routed opposite to noise components. This reduces EMI radiated onto the DC-DC converter's own voltage feedback trace.

DSBGA PACKAGE ASSEMBLY AND USE

Use of the DSBGA package requires specialized board layout, precision mounting and careful re-flow techniques, as detailed in Texas Instruments Application Note AN-1112 (Literature Number SNVA009). Refer to the section *Surface Mount Assembly Considerations*. For best results in assembly, alignment ordinals on the PC board should be used to facilitate placement of the device. The pad style used with DSBGA package must be the NSMD (Non-Solder Mask Defined) type. This means that the solder-mask opening is larger than the pad size. This prevents a lip that otherwise forms if the solder-mask and pad overlap, from holding the device off the surface of the board and interfering with mounting. See Application Note AN-1112 (Literature Number SNVA009) for specific instructions how to do this.

The 6-bump package used for LM3691 has 300-micron solder balls and requires 10.82 mils pads for mounting on the circuit board. The trace to each pad should enter the pad with a 90° entry angle to prevent debris from being caught in deep corners. Initially, the trace to each pad should be 7 mil wide, for a section approximately 7 mil long or longer, as a thermal relief. Then each trace should neck up or down to its optimal width. The important criteria is symmetry. This ensures the solder bumps on the LM3691 re-flow evenly and that the device solders level to the board. In particular, special attention must be paid to the pads for bumps A2 and C2, because GND and V_{IN} are typically connected to large copper planes.

The DSBGA package is optimized for the smallest possible size in applications with red or infrared opaque cases. Because the DSBGA package lacks the plastic encapsulation characteristic of larger devices, it is vulnerable to light. Backside metallization and/or epoxy coating, along with front side shading by the printed circuit board, reduce this sensitivity. However, the package has exposed die edges. In particular, DSBGA devices are sensitive to light, in the red and infrared range, shining on the package's exposed die edges.

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REVISION HISTORY

Changes from Revision H (April 2013) to Revision I	Page
• Changed layout of National Data Sheet to TI format	17

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM3691TL-0.75/NOPB	ACTIVE	DSBGA	YZR	6	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	V	Samples
LM3691TL-1.0/NOPB	ACTIVE	DSBGA	YZR	6	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		F	Samples
LM3691TL-1.2/NOPB	ACTIVE	DSBGA	YZR	6	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	X	Samples
LM3691TL-1.5/NOPB	ACTIVE	DSBGA	YZR	6	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	Y	Samples
LM3691TL-1.8/NOPB	ACTIVE	DSBGA	YZR	6	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	Z	Samples
LM3691TL-2.5/NOPB	ACTIVE	DSBGA	YZR	6	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		8	Samples
LM3691TL-3.3/NOPB	ACTIVE	DSBGA	YZR	6	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		T	Samples
LM3691TLX-0.75/NOPB	ACTIVE	DSBGA	YZR	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	V	Samples
LM3691TLX-1.0/NOPB	ACTIVE	DSBGA	YZR	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		F	Samples
LM3691TLX-1.2/NOPB	ACTIVE	DSBGA	YZR	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	X	Samples
LM3691TLX-1.5/NOPB	ACTIVE	DSBGA	YZR	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	Y	Samples
LM3691TLX-1.8/NOPB	ACTIVE	DSBGA	YZR	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	Z	Samples
LM3691TLX-2.5/NOPB	ACTIVE	DSBGA	YZR	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		8	Samples
LM3691TLX-3.3/NOPB	ACTIVE	DSBGA	YZR	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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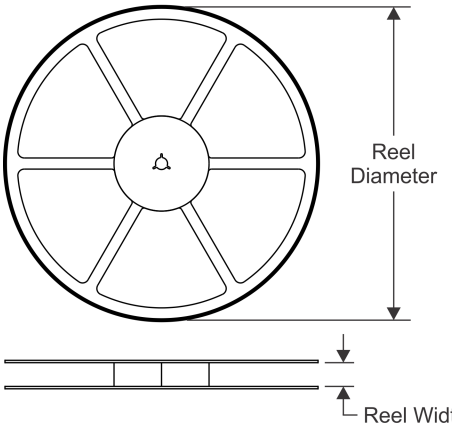
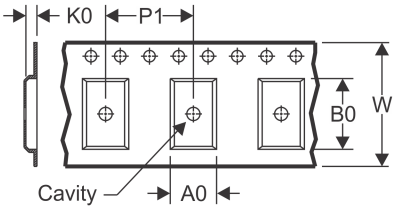
TAPE AND REEL INFORMATION

REEL DIMENSIONS

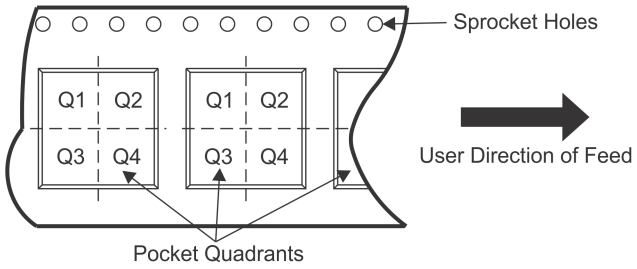


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

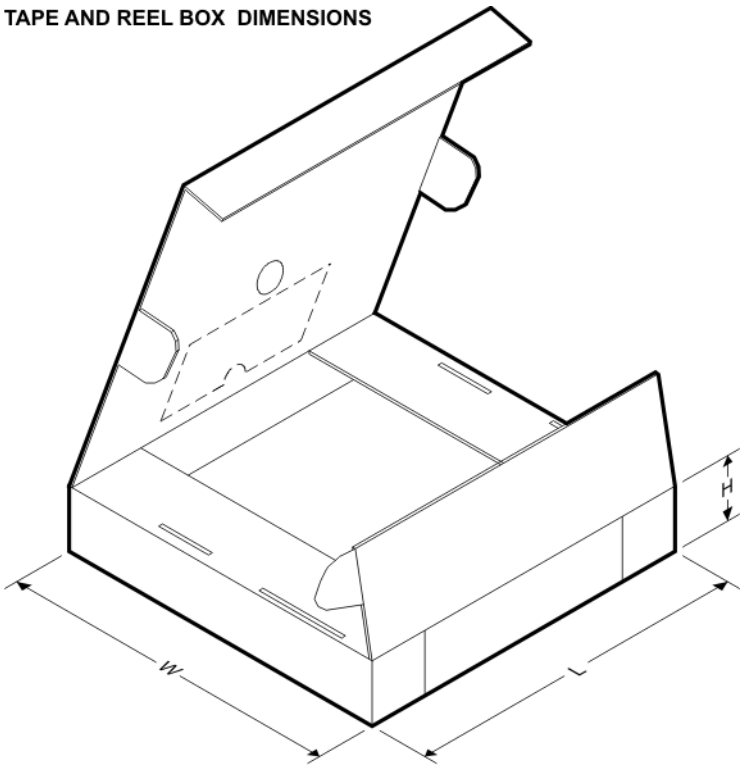
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3691TL-0.75/NOPB	DSBGA	YZR	6	250	178.0	8.4	1.35	1.75	0.76	4.0	8.0	Q1
LM3691TL-1.0/NOPB	DSBGA	YZR	6	250	178.0	8.4	1.35	1.75	0.76	4.0	8.0	Q1
LM3691TL-1.2/NOPB	DSBGA	YZR	6	250	178.0	8.4	1.35	1.75	0.76	4.0	8.0	Q1
LM3691TL-1.5/NOPB	DSBGA	YZR	6	250	178.0	8.4	1.35	1.75	0.76	4.0	8.0	Q1
LM3691TL-1.8/NOPB	DSBGA	YZR	6	250	178.0	8.4	1.35	1.75	0.76	4.0	8.0	Q1
LM3691TL-2.5/NOPB	DSBGA	YZR	6	250	178.0	8.4	1.35	1.75	0.76	4.0	8.0	Q1
LM3691TL-3.3/NOPB	DSBGA	YZR	6	250	178.0	8.4	1.35	1.75	0.76	4.0	8.0	Q1
LM3691TLX-0.75/NOPB	DSBGA	YZR	6	3000	178.0	8.4	1.35	1.75	0.76	4.0	8.0	Q1
LM3691TLX-1.0/NOPB	DSBGA	YZR	6	3000	178.0	8.4	1.35	1.75	0.76	4.0	8.0	Q1
LM3691TLX-1.2/NOPB	DSBGA	YZR	6	3000	178.0	8.4	1.35	1.75	0.76	4.0	8.0	Q1
LM3691TLX-1.5/NOPB	DSBGA	YZR	6	3000	178.0	8.4	1.35	1.75	0.76	4.0	8.0	Q1
LM3691TLX-1.8/NOPB	DSBGA	YZR	6	3000	178.0	8.4	1.35	1.75	0.76	4.0	8.0	Q1
LM3691TLX-2.5/NOPB	DSBGA	YZR	6	3000	178.0	8.4	1.35	1.75	0.76	4.0	8.0	Q1
LM3691TLX-3.3/NOPB	DSBGA	YZR	6	3000	178.0	8.4	1.35	1.75	0.76	4.0	8.0	Q1

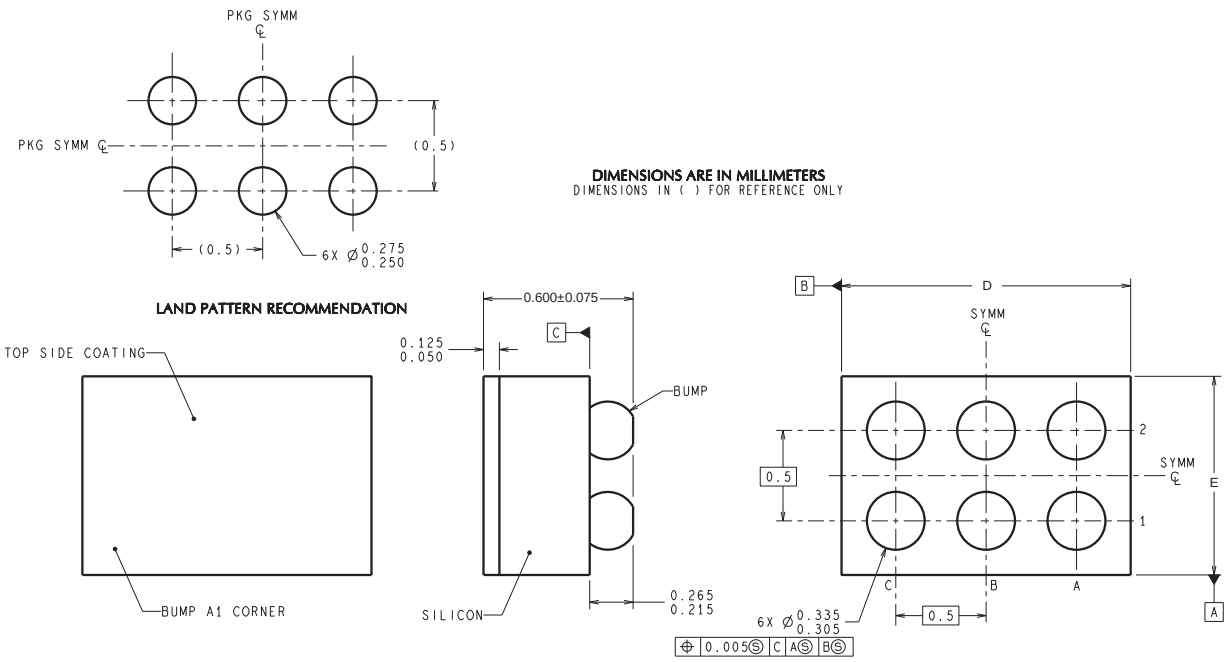
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3691TL-0.75/NOPB	DSBGA	YZR	6	250	210.0	185.0	35.0
LM3691TL-1.0/NOPB	DSBGA	YZR	6	250	210.0	185.0	35.0
LM3691TL-1.2/NOPB	DSBGA	YZR	6	250	210.0	185.0	35.0
LM3691TL-1.5/NOPB	DSBGA	YZR	6	250	210.0	185.0	35.0
LM3691TL-1.8/NOPB	DSBGA	YZR	6	250	210.0	185.0	35.0
LM3691TL-2.5/NOPB	DSBGA	YZR	6	250	210.0	185.0	35.0
LM3691TL-3.3/NOPB	DSBGA	YZR	6	250	210.0	185.0	35.0
LM3691TLX-0.75/NOPB	DSBGA	YZR	6	3000	210.0	185.0	35.0
LM3691TLX-1.0/NOPB	DSBGA	YZR	6	3000	210.0	185.0	35.0
LM3691TLX-1.2/NOPB	DSBGA	YZR	6	3000	210.0	185.0	35.0
LM3691TLX-1.5/NOPB	DSBGA	YZR	6	3000	210.0	185.0	35.0
LM3691TLX-1.8/NOPB	DSBGA	YZR	6	3000	210.0	185.0	35.0
LM3691TLX-2.5/NOPB	DSBGA	YZR	6	3000	210.0	185.0	35.0
LM3691TLX-3.3/NOPB	DSBGA	YZR	6	3000	210.0	185.0	35.0

YZR0006



TLA06XXX (Rev C)

D: Max = 1.59 mm, Min = 1.53 mm

E: Max = 1.295 mm, Min =1.235 mm

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NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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