

LMC7111

LMC7111 Tiny CMOS Operational Amplifier with Rail-to-Rail Input and Output



Literature Number: SNOS753D

LMC7111

Tiny CMOS Operational Amplifier with Rail-to-Rail Input and Output

General Description

The LMC7111 is a micropower CMOS operational amplifier available in the space saving SOT 23-5 package. This makes the LMC7111 ideal for space and weight critical designs. The wide common-mode input range makes it easy to design battery monitoring circuits which sense signals above the V^+ supply. The main benefits of the Tiny package are most apparent in small portable electronic devices, such as mobile phones, pagers, and portable computers. The tiny amplifiers can be placed on a board where they are needed, simplifying board layout.

Features

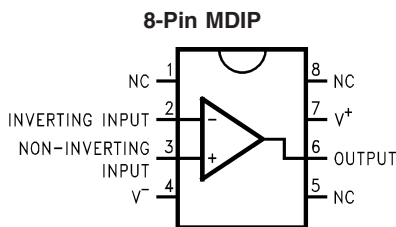
- Tiny 5-Pin SOT23 package saves space
- Very wide common mode input range

- Specified at 2.7V, 5V, and 10V
- Typical supply current 25 μ A at 5V
- 50 kHz gain-bandwidth at 5V
- Similar to popular LMC6462
- Output to within 20 mV of supply rail at 100k load
- Good capacitive load drive

Applications

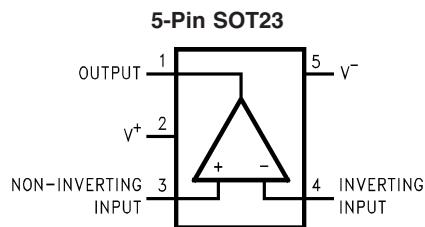
- Mobile communications
- Portable computing
- Current sensing for battery chargers
- Voltage reference buffering
- Sensor interface
- Stable bias for GaAs RF amps

Connection Diagrams



Top View

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Top View

01235202

Actual Size



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Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
8-Pin MDIP	LMC7111AIN	LMC7111AIN	40 Units/Rail	N08E
	LMC7111BIN	LMC7111BIN	40 Units/Rail	
5-Pin SOT23	LMC7111BIM5	A01B	1k units Tape and Reel	MF05A
	LMC7111BIM5X		3k Units Tape and Reel	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

ESD Tolerance (Note 2)	
SOT23 Package	2000V
MDIP Package	1500V
Differential Input Voltage	\pm Supply Voltage
Voltage at Input/Output Pin	$(V^+) + 0.3V, (V^-) - 0.3V$
Supply Voltage ($V^+ - V^-$)	11V
Current at Input Pin	± 5 mA
Current at Output Pin (Note 3)	± 30 mA
Current at Power Supply Pin	30 mA

Lead Temp. (Soldering, 10 sec.)	260°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature (Note 4)	150°C

Operating Ratings (Note 1)

Supply Voltage	$2.5V \leq V^+ \leq 11V$
Junction Temperature Range	$-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$
LMC7111AI, LMC7111BI	
Thermal Resistance (θ_{JA})	
8-Pin MDIP	115°C/W
5-Pin SOT23	325°C/W

2.7V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 2.7V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1$ M Ω . **Bold-face** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7111AI Limit (Note 6)	LMC7111BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage	$V^+ = 2.7V$	0.9	3 5	7 9	mV max
TCV_{OS}	Input Offset Voltage Average Drift		2.0			$\mu\text{V}/^\circ\text{C}$
I_B	Input Bias Current	(Note 9)	0.1	1 20	1 20	pA max
I_{OS}	Input Offset Current	(Note 9)	0.01	0.5 10	0.5 10	pA max
R_{IN}	Input Resistance		>10			Tera Ω
+PSRR	Positive Power Supply Rejection Ratio	$2.7V \leq V^+ \leq 5.0V$, $V^- = 0V, V_O = 2.5V$	60	55 50	55 50	dB min
-PSRR	Negative Power Supply Rejection Ratio	$-2.7V \leq V^- \leq -5.0V$, $V^+ = 0V, V_O = 2.5V$	60	55 50	55 50	dB min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 2.7V$ For CMRR ≥ 50 dB	-0.10	0.0 0.40	0.0 0.40	V min
			2.8	2.7 2.25	2.7 2.25	V max
C_{IN}	Common-Mode Input Capacitance		3			pF
V_O	Output Swing	$V^+ = 2.7V$ $R_L = 100$ k Ω	2.69	2.68 2.4	2.68 2.4	V min
			0.01	0.02 0.08	0.02 0.08	V max
		$V^+ = 2.7V$ $R_L = 10$ k Ω	2.65	2.6 2.4	2.6 2.4	V min
			0.03	0.1 0.3	0.1 0.3	V max
I_{SC}	Output Short Circuit Current	Sourcing, $V_O = 0V$	7	1 0.7	1 0.7	mA min
		Sinking, $V_O = 2.7V$	7	1 0.7	1 0.7	mA min

2.7V DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 2.7\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = V_O = V^+/2$ and $R_L > 1\text{M}\Omega$. **Bold-face** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7111AI Limit (Note 6)	LMC7111BI Limit (Note 6)	Units
A_{VOL}	Voltage Gain	Sourcing	400			V/mv min
		Sinking	150			V/mv min
I_S	Supply Current	$V^+ = +2.7\text{V}$, $V_O = V^+/2$	20	45 60	50 65	μA max

2.7V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 2.7\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = V_O = V^+/2$ and $R_L > 1\text{M}\Omega$. **Bold-face** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7111AI Limit (Note 6)	LMC7111BI Limit (Note 6)	Units
SR	Slew Rate	(Note 8)	0.015			V/ μs
GBW	Gain-Bandwidth Product		40			kHz

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human Body Model is 1.5 k Ω in series with 100 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C.

Note 4: The maximum power dissipation is a function of $T_{\text{J(MAX)}}$, θ_{JA} and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{\text{J(MAX)}} - T_A)/\theta_{\text{JA}}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: $V^+ = 2.7\text{V}$, $V_{\text{CM}} = 1.35\text{V}$ and R_L connected to 1.35V. For Sourcing tests, $1.35\text{V} \leq V_O \leq 2.7\text{V}$. For Sinking tests, $0.5\text{V} \leq V_O \leq 1.35\text{V}$.

Note 8: Connected as Voltage Follower with 1.0V step input. Number specified is the slower of the positive and negative slew rates. Input referred, $V^+ = 2.7\text{V}$ and $R_L = 100\text{k}\Omega$ connected to 1.35V. Amp excited with 1 kHz to produce $V_O = 1 V_{\text{PP}}$.

Note 9: Bias Current guaranteed by design and processing.

3V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 3\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = V_O = V^+/2$ and $R_L > 1\text{M}\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7111AI Limit (Note 6)	LMC7111BI Limit (Note 6)	Units
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 3\text{V}$ For $\text{CMRR} \geq 50\text{ dB}$	-0.25	0.0	0.0	V min
			3.2	3.0 2.8	3.0 2.8	V max

3.3V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 3.3\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = V_O = V^+/2$ and $R_L > 1\text{ M}\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7111AI Limit (Note 6)	LMC7111BI Limit (Note 6)	Units
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 3.3\text{V}$ For $\text{CMRR} \geq 50\text{ dB}$	-0.25	-0.1 0.00	-0.1 0.00	V min
			3.5	3.4 3.2	3.4 3.2	V max

5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = V_O = V^+/2$ and $R_L > 1\text{ M}\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7111AI Limit (Note 6)	LMC7111BI Limit (Note 6)	Units	
V_{OS}	Input Offset Voltage	$V^+ = 5\text{V}$	0.9			mV max	
TCV_{OS}	Input Offset Voltage Average Drift		2.0			$\mu\text{V}/^\circ\text{C}$	
I_{B}	Input Bias Current	(Note 9)	0.1	1 20	1 20	pA max	
I_{OS}	Input Offset Current	(Note 9)	0.01	0.5 10	0.5 10	pA max	
R_{IN}	Input Resistance		>10			Tera Ω	
CMRR	Common Mode Rejection Ratio	$0\text{V} \leq V_{\text{CM}} \leq 5\text{V}$	85	70	60	dB min	
+PSRR	Positive Power Supply Rejection Ratio	$5\text{V} \leq V^+ \leq 10\text{V}$, $V^- = 0\text{V}$, $V_O = 2.5\text{V}$	85	70	60	dB min	
-PSRR	Negative Power Supply Rejection Ratio	$-5\text{V} \leq V^- \leq -10\text{V}$, $V^+ = 0\text{V}$, $V_O = -2.5\text{V}$	85	70	60	dB min	
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5\text{V}$ For $\text{CMRR} \geq 50\text{ dB}$	-0.3	-0.20 0.00	-0.20 0.00	V min	
			5.25	5.20 5.00	5.20 5.00	V max	
C_{IN}	Common-Mode Input Capacitance		3			pF	
V_O	Output Swing	$V^+ = 5\text{V}$ $R_L = 100\text{ k}\Omega$	4.99	4.98	4.98	Vmin	
			0.01	0.02	0.02	Vmax	
			$V^+ = 5\text{V}$ $R_L = 10\text{ k}\Omega$	4.98	4.9	4.9	Vmin
				0.02	0.1	0.1	Vmin
I_{SC}	Output Short Circuit Current	Sourcing, $V_O = 0\text{V}$	7	5 3.5	5 3.5	mA min	
			Sinking, $V_O = 3\text{V}$	7	5 3.5	5 3.5	mA min
A_{VOL}	Voltage Gain	Sourcing	500			V/mv min	
		Sinking	200			V/mv min	
I_{S}	Supply Current	$V^+ = +5\text{V}$, $V_O = V^+/2$	25			μA max	

5V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = V_O = V^+/2$ and $R_L > 1\text{M}\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7111AI Limit (Note 6)	LMC7111BI Limit (Note 6)	Units
SR	Slew Rate	Positive Going Slew Rate (Note 8)	0.027	0.015	0.010	V/ μs
GBW	Gain-Bandwidth Product		50			kHz

Note 10: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 11: Human body model, 1.5 k Ω in series with 100 pF.

Note 12: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C.

Note 13: The maximum power dissipation is a function of $T_{J(\text{max})}$, θ_{JA} and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(\text{max})} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 14: Typical Values represent the most likely parametric norm.

Note 15: All limits are guaranteed by testing or statistical analysis.

Note 16: $V^+ = 5\text{V}$, $V_{\text{CM}} = 2.5\text{V}$ and R_L connected to 2.5V. For Sourcing tests, $2.5\text{V} \leq V_O \leq 5.0\text{V}$. For Sinking tests, $0.5\text{V} \leq V_O \leq 2.5\text{V}$.

Note 17: Connected as Voltage Follower with 1.0V step input. Number specified is the slower of the positive slew rate. The negative slew rate is faster. Input referred, $V^+ = 5\text{V}$ and $R_L = 100\text{ k}\Omega$ connected to 1.5V. Amp excited with 1 kHz to produce $V_O = 1\text{ V}_{\text{pp}}$.

Note 18: Bias Current guaranteed by design and processing.

10V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 10\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = V_O = V^+/2$ and $R_L > 1\text{M}\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7111AI Limit (Note 6)	LMC7111BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage	$V^+ = 10\text{V}$	0.9	3 5	7 9	mV max
TCV_{OS}	Input Offset Voltage Average Drift		2.0			$\mu\text{V}/^\circ\text{C}$
I_B	Input Bias Current		0.1	1 20	1 20	pA max
I_{OS}	Input Offset Current		0.01	0.5 10	0.5 10	pA max
R_{IN}	Input Resistance		>10			Tera Ω
+PSRR	Positive Power Supply Rejection Ratio	$5\text{V} \leq V^+ \leq 10\text{V}$, $V^- = 0\text{V}$, $V_O = 2.5\text{V}$	80			dB min
-PSRR	Negative Power Supply Rejection Ratio	$-5\text{V} \leq V^- \leq -10\text{V}$, $V^- = 0\text{V}$, $V_O = 2.5\text{V}$	80			dB min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 10\text{V}$ For $\text{CMRR} \geq 50\text{ dB}$	-0.2	-0.15 0.00	-0.15 0.00	V min
			10.2	10.15 10.00	10.15 10.00	V max
C_{IN}	Common-Mode Input Capacitance		3			pF
I_{SC}	Output Short Circuit Current (Note 9)	Sourcing, $V_O = 0\text{V}$	30	20 7	20 7	mA min
		Sinking, $V_O = 10\text{V}$	30	20 7	20 7	mA min

10V DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 10\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = V_O = V^+/2$ and $R_L > 1\text{ M}\Omega$. **Bold-face** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7111AI Limit (Note 6)	LMC7111BI Limit (Note 6)	Units
A_{VOL}	Voltage Gain 100 k Ω Load	Sourcing	500			V/mv min
		Sinking	200			V/mv min
I_S	Supply Current	$V^+ = +10\text{V}$, $V_O = V^+/2$	25	50 65	60 75	μA max
V_O	Output Swing	$V^+ = 10\text{V}$	9.99	9.98	9.98	Vmin
		$R_L = 100\text{ k}\Omega$	0.01	0.02	0.02	Vmax
		$V^+ = 10\text{V}$	9.98	9.9	9.9	Vmin
		$R_L = 10\text{ k}\Omega$	0.02	0.1	0.1	Vmin

10V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 10\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = V_O = V^+/2$ and $R_L > 1\text{ M}\Omega$. **Bold-face** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7111AI Limit (Note 6)	LMC7111BI Limit (Note 6)	Units
SR	Slew Rate	(Note 8)	0.03			V/ μs
GBW	Gain-Bandwidth Product		50			kHz
ϕ_m	Phase Margin		50			deg
G_m	Gain Margin		15			dB
	Input-Referred Voltage Noise	$f = 1\text{ kHz}$ $V_{\text{CM}} = 1\text{V}$	110			$\frac{\text{nV}}{\sqrt{\text{Hz}}}$
	Input-Referred Current Noise	$f = 1\text{ kHz}$	0.03			$\frac{\text{pA}}{\sqrt{\text{Hz}}}$

Note 19: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 20: Human body model, 1.5 k Ω in series with 100 pF.

Note 21: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C.

Note 22: The maximum power dissipation is a function of $T_{J(\text{max})}$, θ_{JA} and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(\text{max})} - T_A)/\theta_{\text{JA}}$. All numbers apply for packages soldered directly into a PC board.

Note 23: Typical Values represent the most likely parametric norm.

Note 24: All limits are guaranteed by testing or statistical analysis.

Note 25: $V^+ = 10\text{V}$, $V_{\text{CM}} = 5\text{V}$ and R_L connected to 5V. For Sourcing tests, $5\text{V} \leq V_O \leq 10\text{V}$. For Sinking tests, $0.5\text{V} \leq V_O \leq 5\text{V}$.

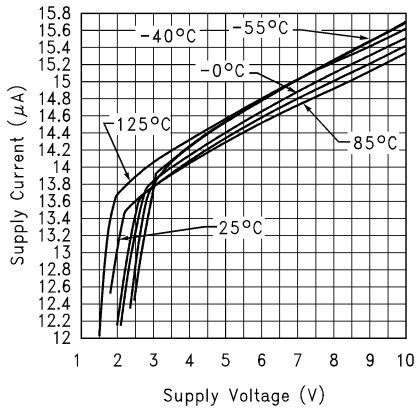
Note 26: Connected as Voltage Follower with 1.0V step input. Number specified is the slower of the positive and negative slew rates. Input referred, $V^+ = 10\text{V}$ and $R_L = 100\text{ k}\Omega$ connected to 5V. Amp excited with 1 kHz to produce $V_O = 2\text{ V}_{\text{PP}}$.

Note 27: Operation near absolute maximum limits will adversely affect reliability.

Typical Performance Characteristics

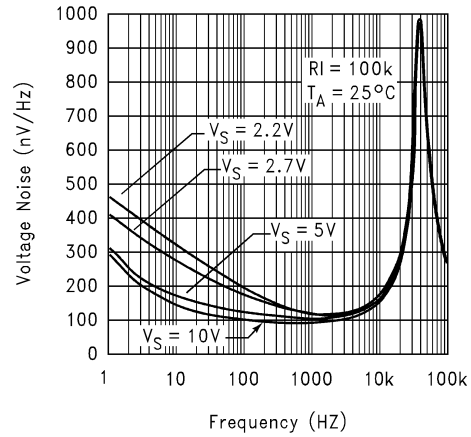
$T_A = 25^\circ\text{C}$ unless specified, Single Supply

Supply Current vs. Supply Voltage



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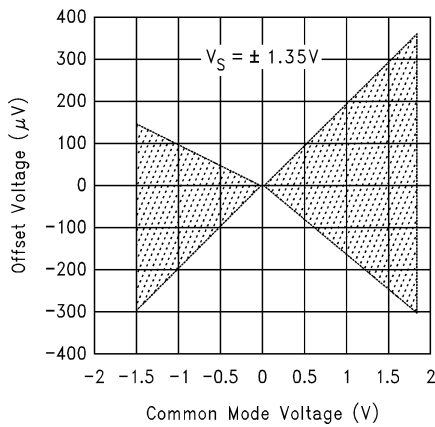
Voltage Noise vs. Frequency



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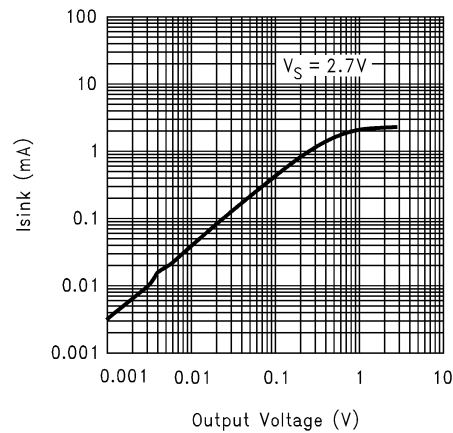
2.7V Performance

Offset Voltage vs. Common Mode Voltage @ 2.7V



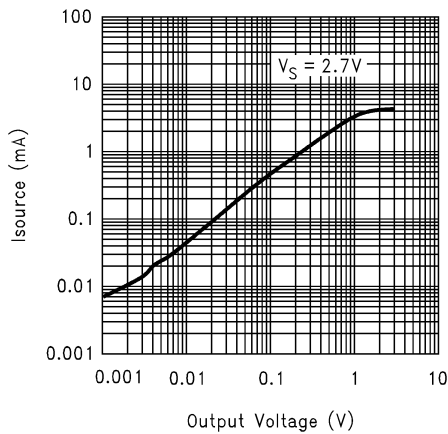
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Sinking Output vs. Output Voltage



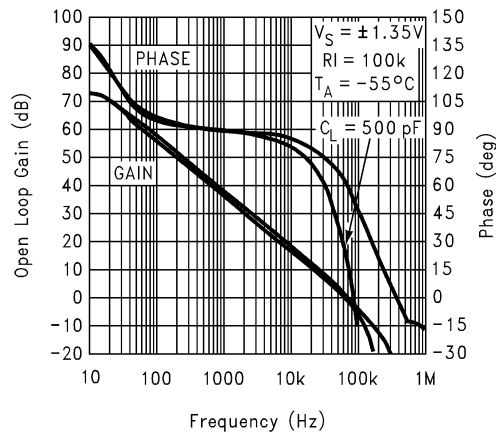
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Sourcing Output vs. Output Voltage



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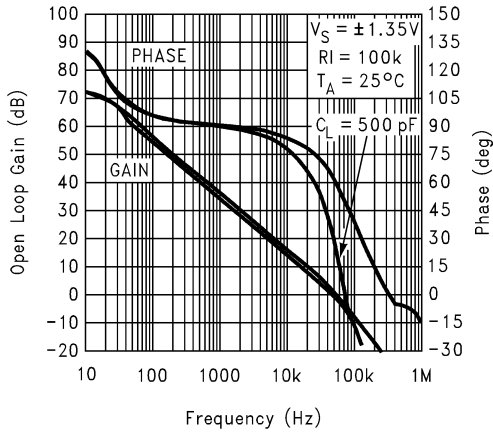
Gain and Phase vs. Capacitive Load @ 2.7V



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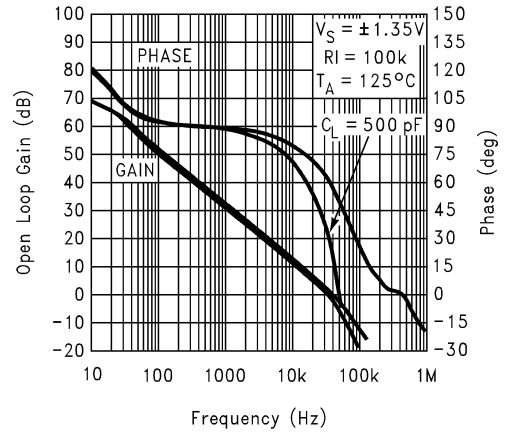
2.7V Performance (Continued)

Gain and Phase vs. Capacitive Load @ 2.7V



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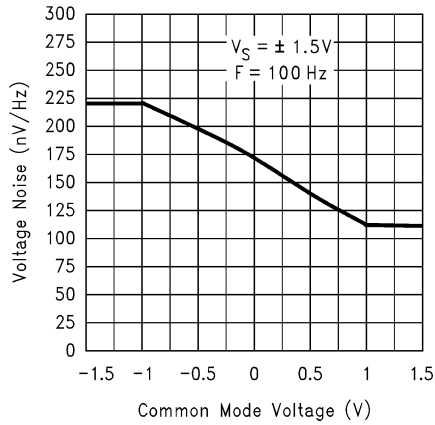
Gain and Phase vs. Capacitive Load @ 2.7V



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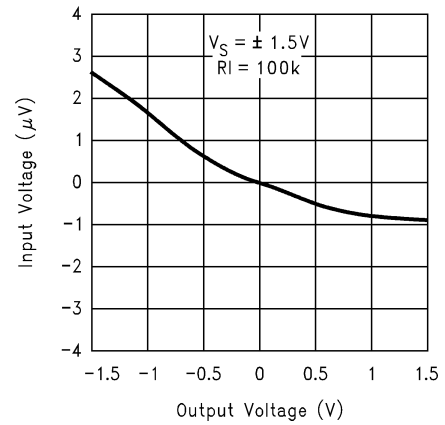
3V Performance

Voltage Noise vs. Common Mode Voltage @ 3V



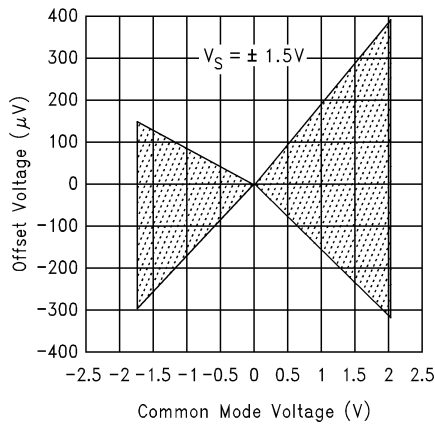
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Output Voltage vs. Input Voltage @ 3V



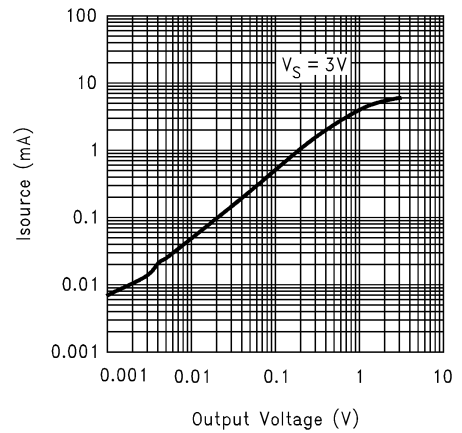
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Offset Voltage vs. Common Mode Voltage @ 3V



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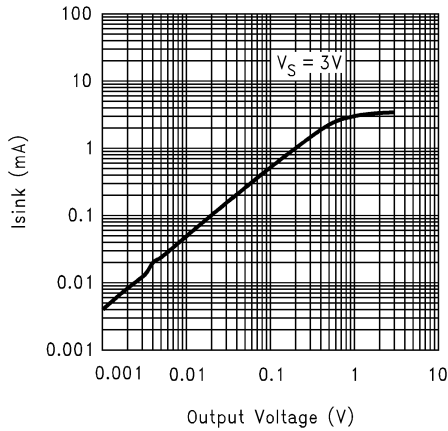
Sourcing Output vs. Output Voltage



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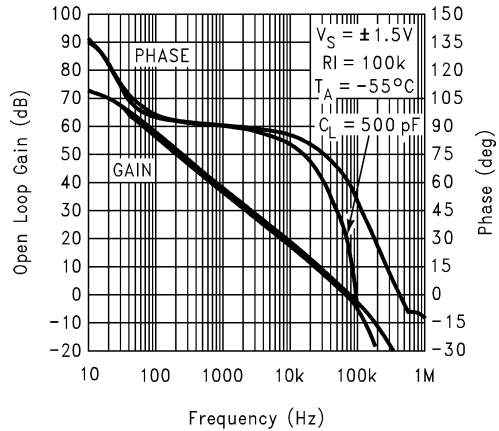
3V Performance (Continued)

Sinking Output vs. Output Voltage



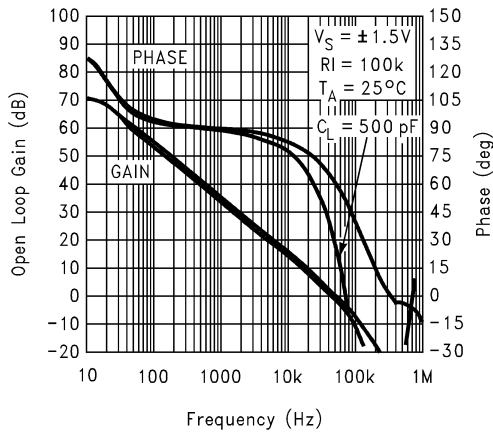
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Gain and Phase vs. Capacitive Load @ 3V



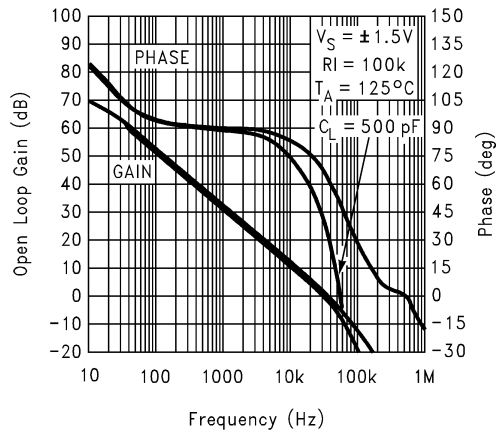
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Gain and Phase vs. Capacitive Load @ 3V



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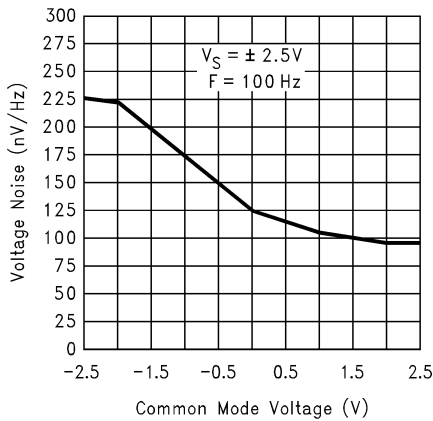
Gain and Phase vs. Capacitive Load @ 3V



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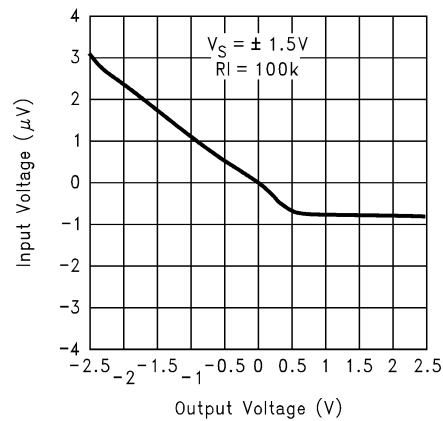
5V Performance

Voltage Noise vs. Common Mode Voltage @ 5V



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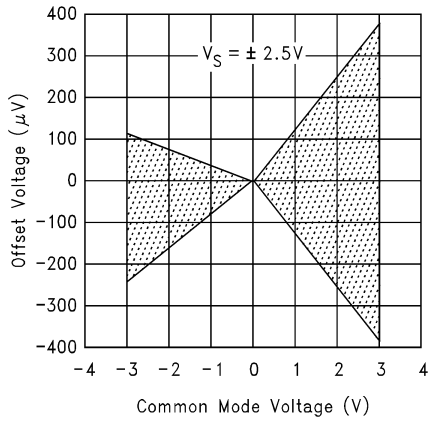
Output Voltage vs. Input Voltage @ 5V



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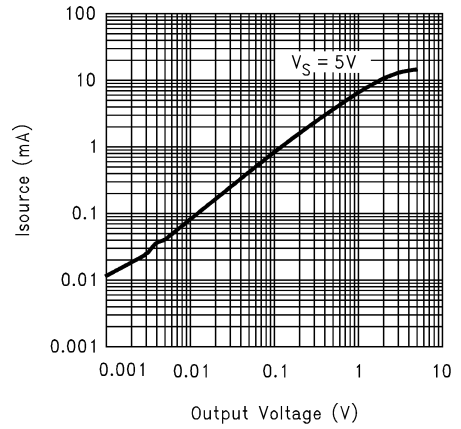
5V Performance (Continued)

Offset Voltage vs. Common Mode Voltage @ 5V



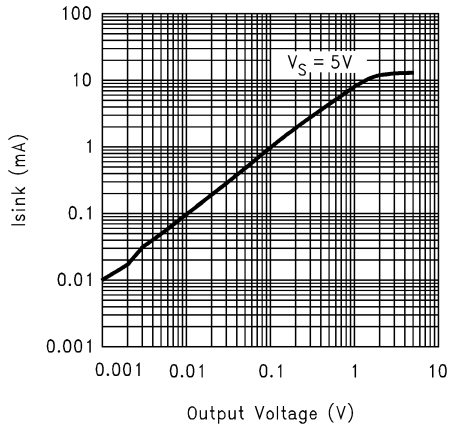
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Sourcing Output vs. Output Voltage



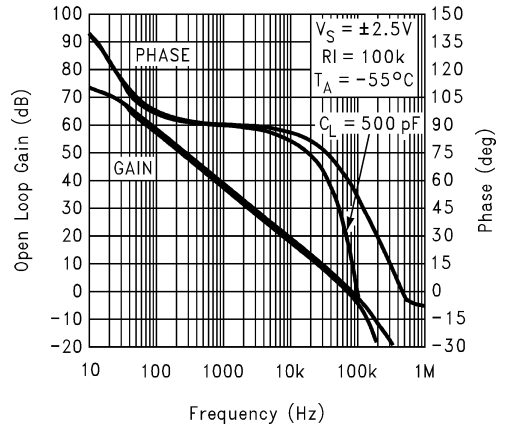
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Sinking Output vs. Output Voltage



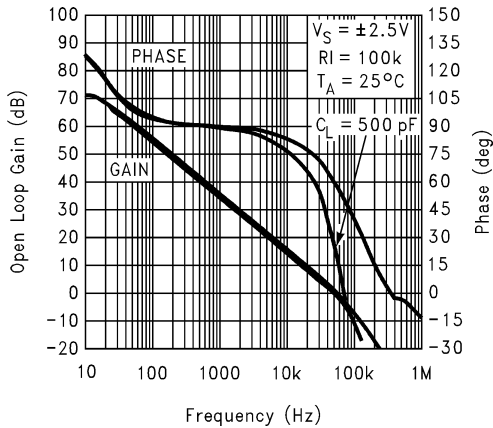
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Gain and Phase vs. Capacitive Load @ 5V



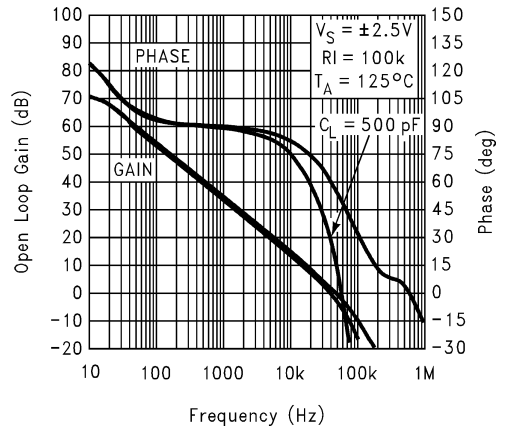
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Gain and Phase vs. Capacitive Load @ 5V



01235239

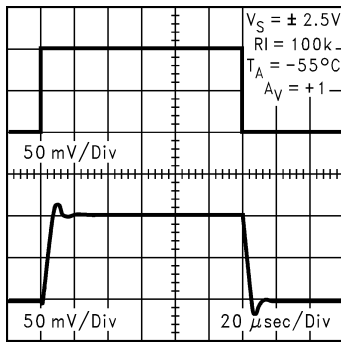
Gain and Phase vs. Capacitive Load @ 5V



01235240

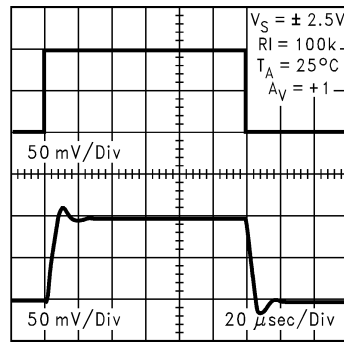
5V Performance (Continued)

Non-Inverting Small Signal Pulse Response at 5V



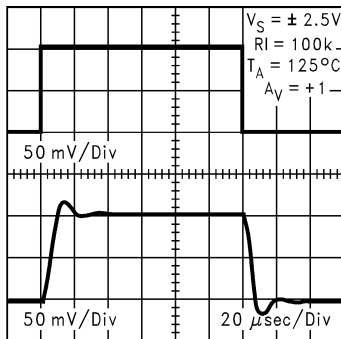
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Non-Inverting Small Signal Pulse Response at 5V



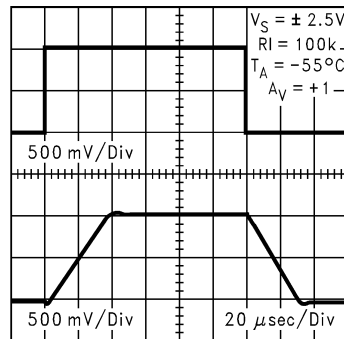
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Non-Inverting Small Signal Pulse Response at 5V



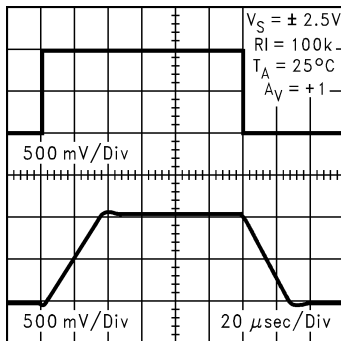
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Non-Inverting Large Signal Pulse Response at 5V



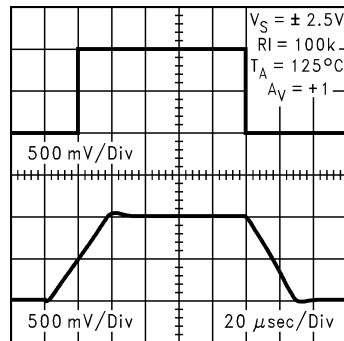
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Non-Inverting Large Signal Pulse Response at 5V



01235245

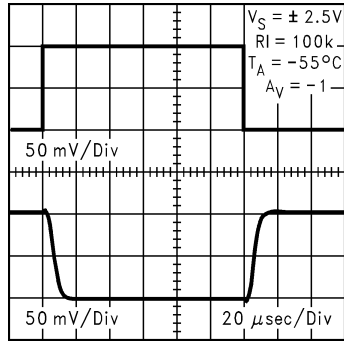
Non-Inverting Large Signal Pulse Response at 5V



01235246

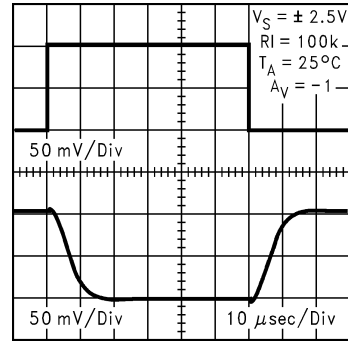
5V Performance (Continued)

Inverting Small Signal Pulse Response at 5V



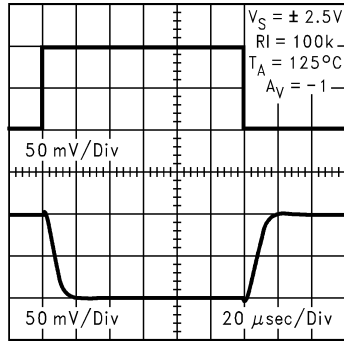
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Inverting Small Signal Pulse Response at 5V



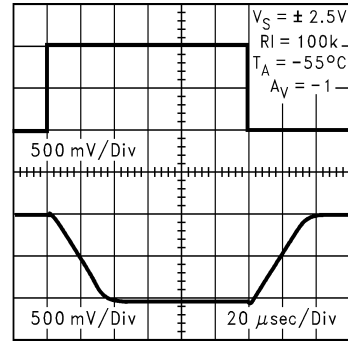
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Inverting Small Signal Pulse Response at 5V



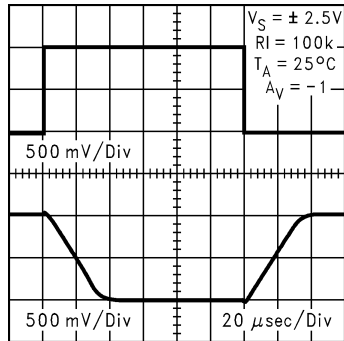
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Inverting Large Signal Pulse Response at 5V



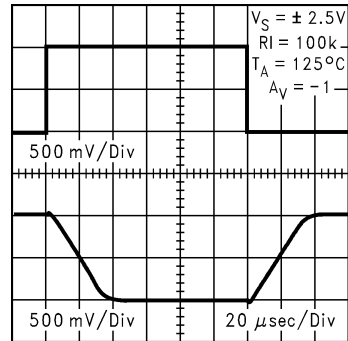
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Inverting Large Signal Pulse Response at 5V



01235251

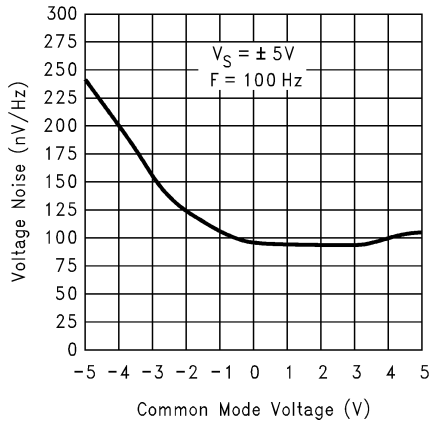
Inverting Large Signal Pulse Response at 5V



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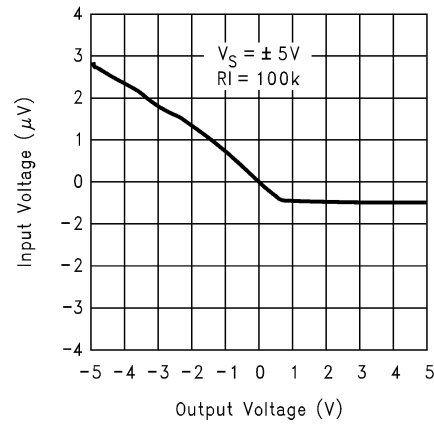
10V Performance

Voltage Noise vs. Common Mode Voltage @ 10V



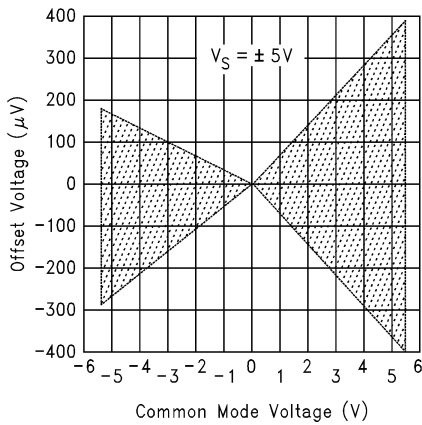
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Output Voltage vs. Input Voltage @ 10V



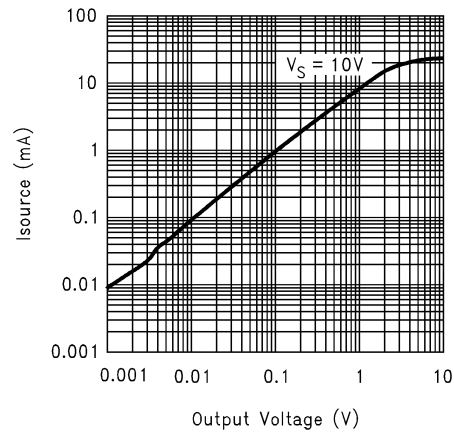
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Offset Voltage vs. Common Mode Voltage @ 10V



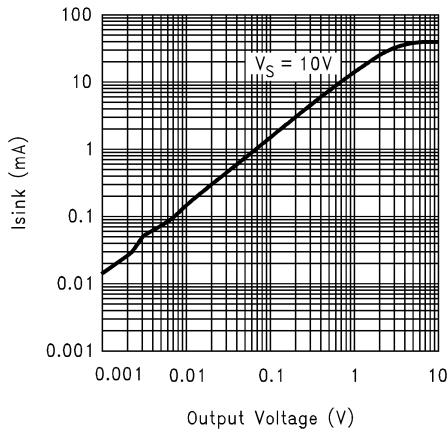
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Sourcing Output vs. Output Voltage



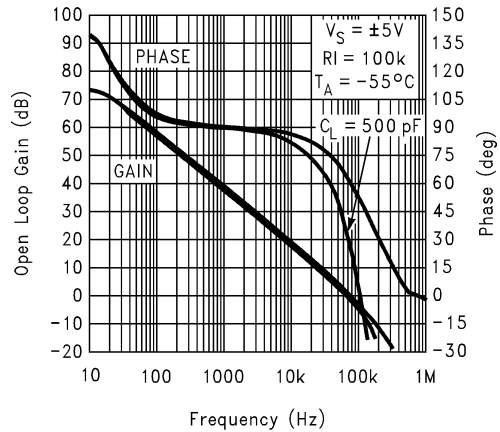
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Sinking Output vs. Output Voltage



01235257

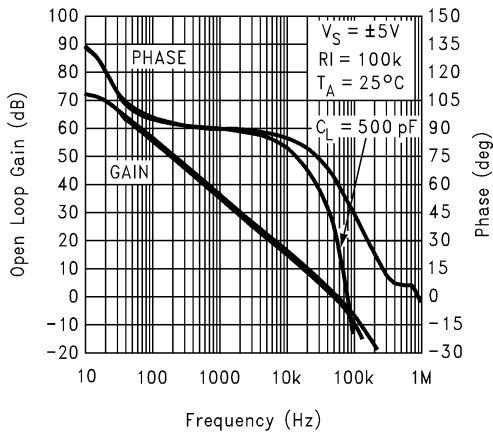
Gain and Phase vs. Capacitive Load @ 10V



01235258

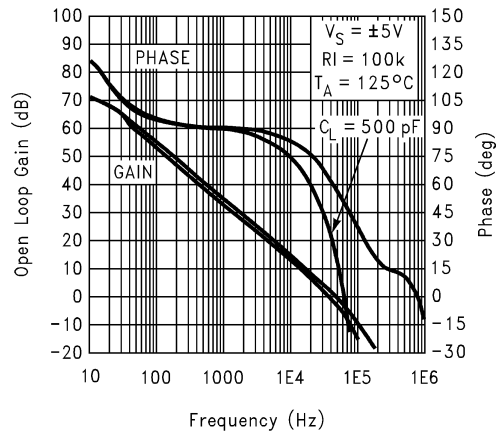
10V Performance (Continued)

Gain and Phase vs. Capacitive Load @ 10V



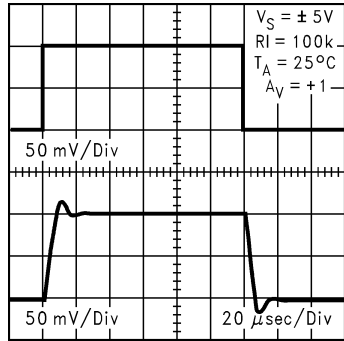
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Gain and Phase vs. Capacitive Load @ 10V



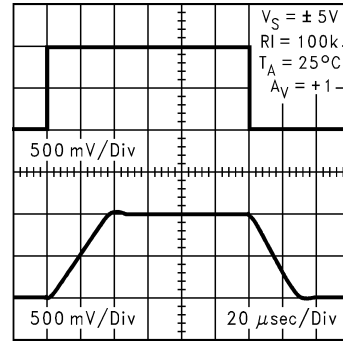
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Non-Inverting Small Signal Pulse Response at 10V



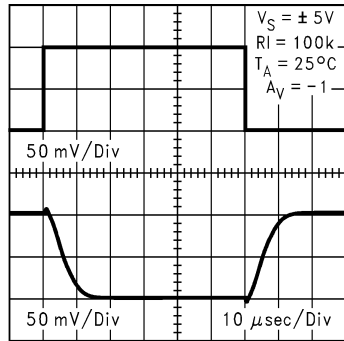
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Non-Inverting Large Signal Pulse Response at 10V



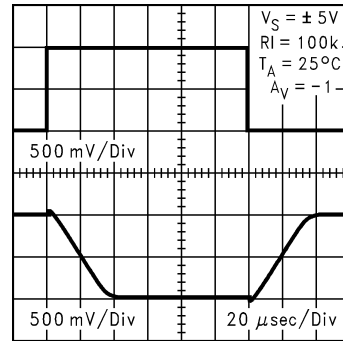
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Inverting Small Signal Pulse Response at 10V



01235263

Inverting Large Signal Pulse Response at 10V



01235264

Application Information

1.0 BENEFITS OF THE LMC7111 TINY AMP

Size

The small footprint of the SOT 23-5 packaged Tiny amp, (0.120 x 0.118 inches, 3.05 x 3.00 mm) saves space on printed circuit boards, and enable the design of smaller electronic products. Because they are easier to carry, many customers prefer smaller and lighter products.

Height

The height (0.056 inches, 1.43 mm) of the Tiny amp makes it possible to use it in PCMCIA type III cards.

Signal Integrity

Signals can pick up noise between the signal source and the amplifier. By using a physically smaller amplifier package, the Tiny amp can be placed closer to the signal source, reducing noise pickup and increasing signal integrity. The Tiny amp can also be placed next to the signal destination, such as a buffer for the reference of an analog to digital converter.

Simplified Board Layout

The Tiny amp can simplify board layout in several ways. First, by placing an amp where amps are needed, instead of routing signals to a dual or quad device, long pc traces may be avoided.

By using multiple Tiny amps instead of duals or quads, complex signal routing and possibly crosstalk can be reduced.

DIPs available for prototyping

LMC7111 amplifiers packaged in conventional 8-pin dip packages can be used for prototyping and evaluation without the need to use surface mounting in early project stages.

Low Supply Current

The typical 25 μ A supply current of the LMC7111 extends battery life in portable applications, and may allow the reduction of the size of batteries in some applications.

Wide Voltage Range

The LMC7111 is characterized at 2.7V, 3V, 3.3V, 5V and 10V. Performance data is provided at these popular voltages. This wide voltage range makes the LMC7111 a good choice for devices where the voltage may vary over the life of the batteries.

2.0 INPUT COMMON MODE VOLTAGE RANGE

The LMC7111 does not exhibit phase inversion when an input voltage exceeds the negative supply voltage.

The absolute maximum input voltage is 300 mV beyond either rail at room temperature. Voltages greatly exceeding this maximum rating can cause excessive current to flow in or out of the input pins, adversely affecting reliability.

Applications that exceed this rating must externally limit the maximum input current to ± 5 mA with an input resistor as shown in *Figure 1*.

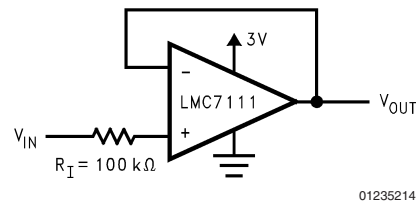


FIGURE 1. R_I Input Current Protection for Voltages Exceeding the Supply Voltage

3.0 CAPACITIVE LOAD TOLERANCE

The LMC7111 can typically directly drive a 300 pF load with $V_S = 10V$ at unity gain without oscillating. The unity gain follower is the most sensitive configuration. Direct capacitive loading reduces the phase margin of op-amps. The combination of the op-amp's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation.

Capacitive load compensation can be accomplished using resistive isolation as shown in *Figure 2*. This simple technique is useful for isolating the capacitive input of multiplexers and A/D converters.

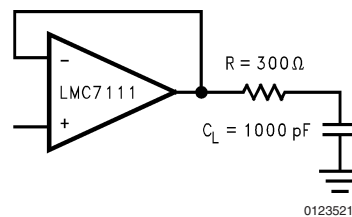


FIGURE 2. Resistive Isolation of a 330 pF Capacitive Load

4.0 COMPENSATING FOR INPUT CAPACITANCE WHEN USING LARGE VALUE FEEDBACK RESISTORS

When using very large value feedback resistors, (usually > 500 k Ω) the large feedback resistance can react with the input capacitance due to transducers, photodiodes, and circuit board parasitics to reduce phase margins.

The effect of input capacitance can be compensated for by adding a feedback capacitor. The feedback capacitor (as in *Figure 3*), C_f is first estimated by:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f}$$

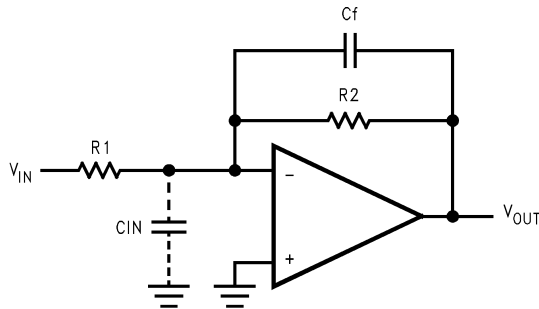
or

$$R_1 C_{IN} \leq R_2 C_f$$

which typically provides significant overcompensation.

Printed circuit board stray capacitance may be larger or smaller than that of a breadboard, so the actual optimum value for C_f may be different. The values of C_f should be checked on the actual circuit. (Refer to the LMC660 quad CMOS amplifier data sheet for a more detailed discussion.)

Application Information (Continued)



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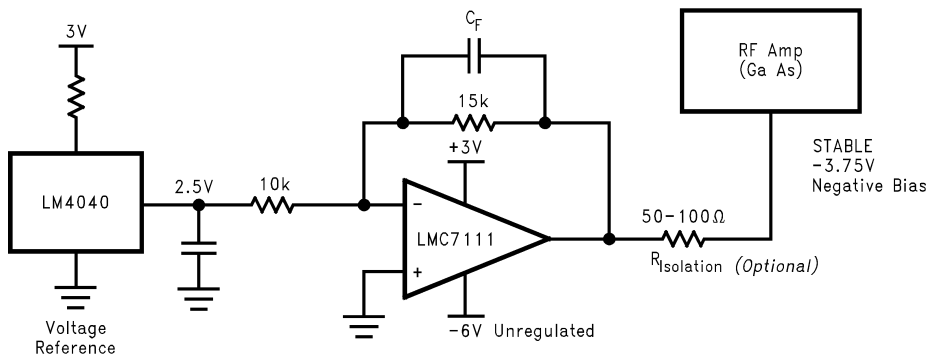
FIGURE 3. Cancelling the Effect of Input Capacitance

5.0 OUTPUT SWING

The output of the LMC7111 will go to within 100 mV of either power supply rail for a 10 kΩ load and to 20 mV of the rail for a 100 kΩ load. This makes the LMC7111 useful for driving transistors which are connected to the same power supply. By going very close to the supply, the LMC7111 can turn the transistors all the way on or all the way off.

6.0 BIASING GaAs RF AMPLIFIERS

The capacitive load capability, low current draw, and small size of the SOT23-5 LMC7111 make it a good choice for providing a stable negative bias to other integrated circuits. The very small size of the LMC7111 and the LM4040 reference take up very little board space.



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C_F and $R_{isolation}$ prevent oscillations when driving capacitive loads.

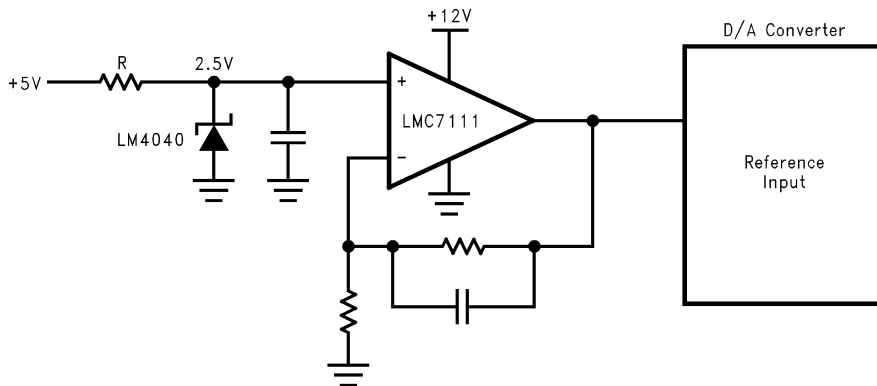
FIGURE 4. Stable Negative Bias

7.0 REFERENCE BUFFER FOR A-TO-D CONVERTERS

The LMC7111 can be used as a voltage reference buffer for analog-to-digital converters. This works best for A-to-D converters whose reference input is a static load, such as dual slope integrating A-to-Ds. Converters whose reference input is a dynamic load (the reference current changes with time) may need a faster device, such as the LMC7101 or the LMC7131.

The small size of the LMC7111 allows it to be placed close to the reference input. The low supply current (25 μA typical) saves power.

For A-to-D reference inputs which require higher accuracy and lower offset voltage, please see the LMC6462 datasheet. The LMC6462 has performance similar to the LMC7111. The LMC6462 is available in two grades with reduced input voltage offset.



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Application Information (Continued)

8.0 DUAL AND QUAD DEVICES WITH SIMILAR PERFORMANCE

The LMC6462 and LMC6464 are dual and quad devices with performance similar to the LMC7111. They are available in both conventional through-hole and surface mount packaging. Please see the LMC6462/4 datasheet for details.

9.0 SPICE MACROMODEL

A SPICE macromodel is available for the LMC7111. This model includes simulation of:

- Input common-mode voltage range
- Frequency and transient response
- Quiescent and dynamic supply current
- Output swing dependence on loading conditions and many more characteristics as listed on the macro model disk. Contact your local National Semiconductor sales office to obtain an operational amplifier spice model library disk.

10.0 ADDITIONAL SOT23-5 TINY DEVICES

National Semiconductor has additional parts available in the space saving SOT23 Tiny package, including amplifiers, voltage references, and voltage regulators. These devices

include—

- LMC7101** 1 MHz gain-bandwidth rail-to-rail input and output amplifier—high input impedance and high gain, 700 μ A typical current 2.7V, 3V, 5V and 15V specifications.
- LM7131** Tiny Video amp with 70 MHz gain bandwidth. Specified at 3V, 5V and \pm 5V supplies.
- LMC7211** Comparator in a tiny package with rail-to-rail input and push-pull output. Typical supply current of 7 μ A. Typical propagation delay of 7 μ s. Specified at 2.7V, 5V and 15V supplies.
- LMC7221** Comparator with an open drain output for use in mixed voltage systems. Similar to the LMC7211, except the output can be used with a pull-up resistor to a voltage different than the supply voltage.
- LP2980** Micropower SOT 50 mA Ultra Low-Dropout Regulator.
- LM4040** Precision micropower shunt voltage reference. Fixed voltages of 2.5000V, 4.096V, 5.000V, 8.192V and 10.000V.
- LM4041** Precision micropower shunt voltage reference 1.225V and adjustable.

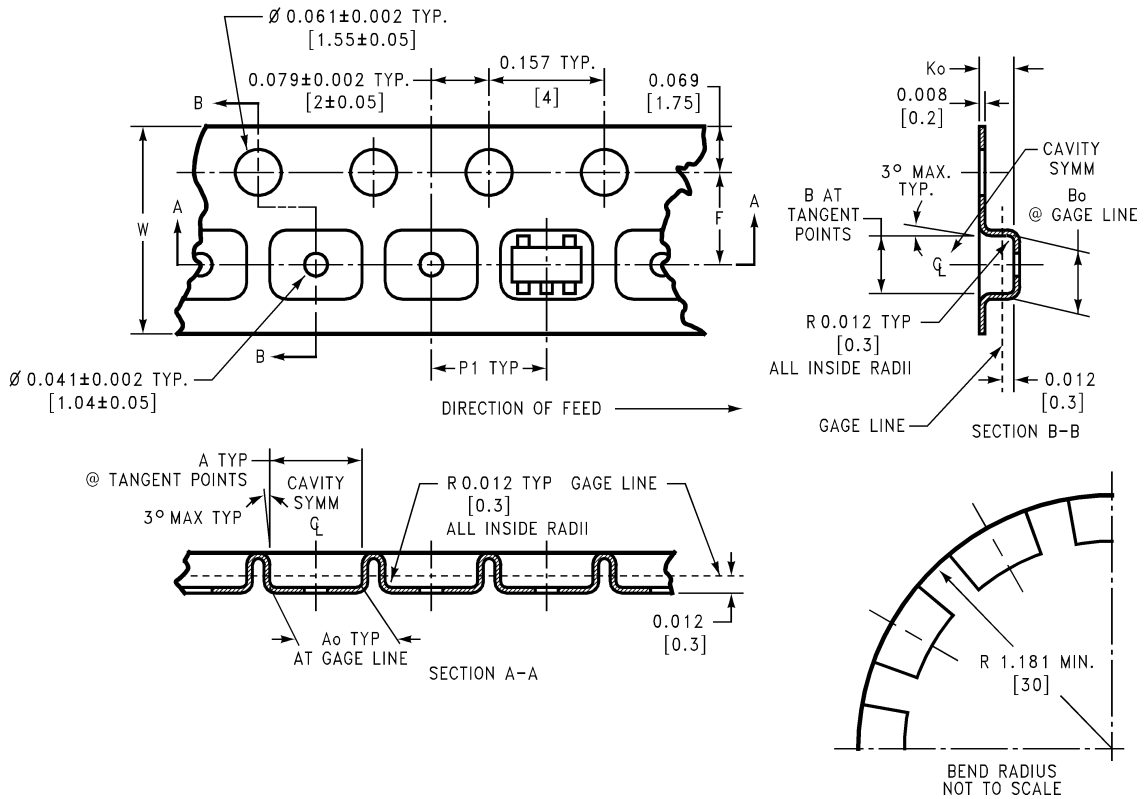
Contact your National Semiconductor representative for the latest information.

SOT-23-5 Tape and Reel Specification

TAPE FORMAT

Tape Section	# Cavities	Cavity Status	Cover Tape Status
Leader (Start End)	0 (min)	Empty	Sealed
	75 (min)	Empty	Sealed
Carrier	3000	Filled	Sealed
	1000	Filled	Sealed
Trailer (Hub End)	125 (min)	Empty	Sealed
	0 (min)	Empty	Sealed

TAPE DIMENSIONS

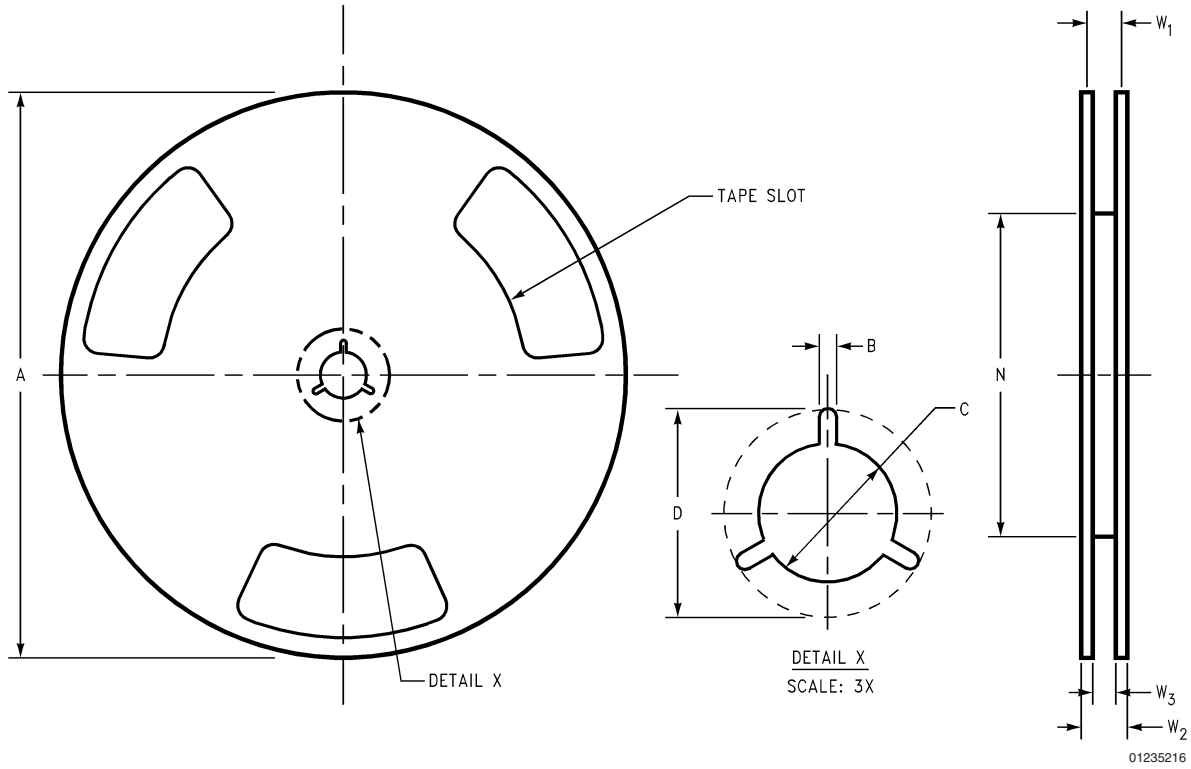


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8 mm	0.130	0.124	0.130	0.126	0.138 ± 0.002	0.055 ± 0.004	0.157	0.315 ± 0.012
	(3.3)	(3.15)	(3.3)	(3.2)	(3.5 ± 0.05)	(1.4 ± 0.11)	(4)	(8 ± 0.3)
Tape Size	DIM A	DIM A _o	DIM B	DIM B _o	DIM F	DIM K _o	DIM P ₁	DIM W

SOT-23-5 Tape and Reel Specification (Continued)

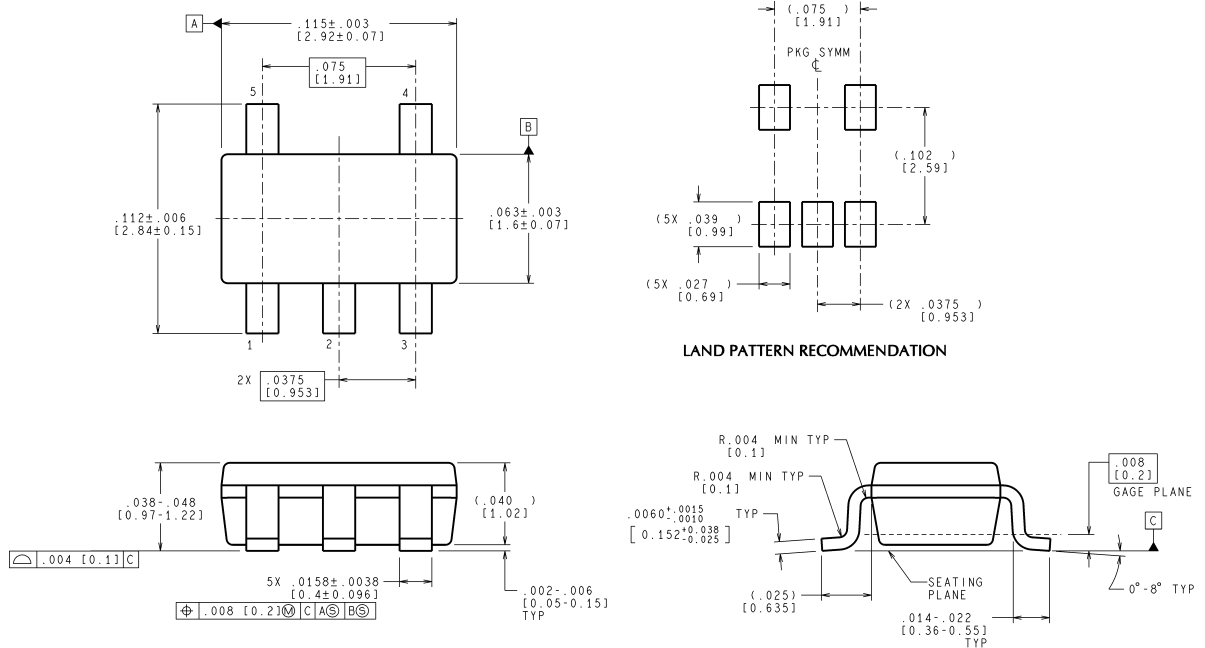
REEL DIMENSIONS



8 mm	7.00	0.059	0.512	0.795	2.165	0.331 + 0.059/-0.000	0.567	W1 + 0.078/-0.039
	330.00	1.50	13.00	20.20	55.00	8.40 + 1.50/-0.00	14.40	W1 + 2.00/-1.00
Tape Size	A	B	C	D	N	W1	W2	W3

Physical Dimensions inches (millimeters)

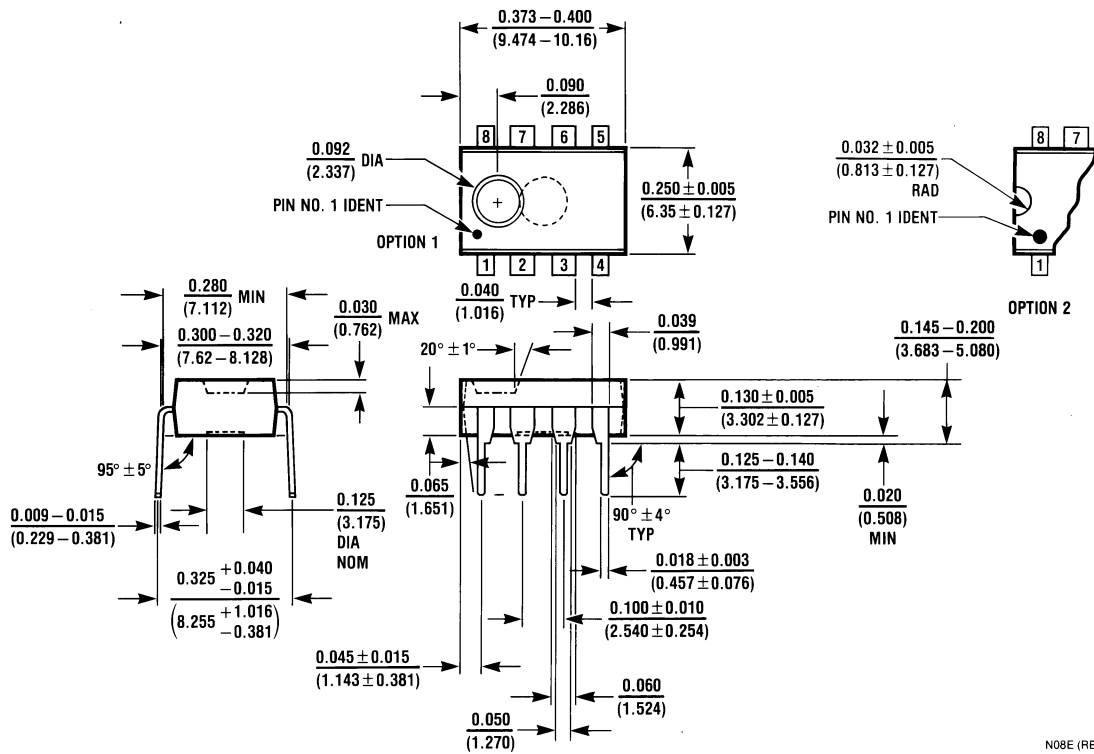
unless otherwise noted



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MF05A (Rev C)

5-Pin SOT23 NS Package Number MF05A



N08E (REV F)

8-Pin Molded DIP 8-Lead (0.300" Wide) Molded Dual-In-Line Package NS Package Number N08E

Notes

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