

MOTOROLA

SEMICONDUCTOR

TECHNICAL DATA

Product Preview

9-Bit Translators

- 9-Bit Ideal for Byte-Parity Applications
- Flow-Through Configuration
- Extra TTL and ECL Power/Ground Pins to Minimize Switching Noise
- Dual Supply
- PNP TTL Inputs for Low Loading
- Choice of ECL Compatibility: MECL 10KH (10Hxxx) or 100K (100Hxxx)

MC10H/100H600
MC10H/100H601
MC10H/100H602
MC10H/100H603

9-BIT
TTL-ECL/ECL-TTL
TRANSLATORS

These MECL 10KH ECL-TTL and TTL-ECL translators are ideally suited for byte-parity data transmission across the ECL/TTL interface, in applications such as interfacing to main memory or a TTL peripheral bus in ECL based computers and instrumentation.

The 28-lead PLCC package allows adequate power and ground pinning for the nine-wide functions, and its quad configuration allows for sensible flow-through design, reduced parasitic inductance and superior skew characteristics compared to a dual package of similar size such as DIP. It is also space efficient and cost effective.

AC performance is specified at two values of load capacitance due to the high capacitance nature of many DRAM-driving applications. The user is reminded to include the dynamic power taken by the load capacitance when calculating system power consumption.

The following pages show device-specific DC and AC characteristics of the family. Common DC characteristics appear on page 10.

AC Parameter Measurements

Measurement points for the AC parameters specified in this data sheet conform to the following convention:

Propagation Delay

ECL: To/From 50% point of swing
 TTL: To/From 1.5 V

Output Rise/Fall Time

ECL: 20%–80% points of swing
 TTL: 1.0 V–2.0 V

Switching Waveforms and General Information

The standard parameter definitions and switching waveforms are not repeated here. For information on these, the user is referred to the following Motorola Inc. publications:

MECL Device Data Book, DL122/D.

FAST and LS TTL Data Book, DL121/D.

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Product Preview

- 9-Bit Ideal for Byte-Parity Applications
- Flow-Through Configuration
- Extra TTL and ECL Power/Ground Pins to Minimize Switching Noise
- ECL and TTL Enable Inputs
- Dual Supply
- 3.5 ns max. D to Q
- PNP TTL Inputs for Low Loading
- Choice of ECL Compatibility: MECL 10KH (10Hxxx) or 100K (100Hxxx)

The MC10H/100H600 is a 9-bit, dual supply TTL to ECL translator. Devices in the Motorola 9-bit translator series utilize the 28-lead PLCC for optimal power pinning, signal flow-through and electrical performance.

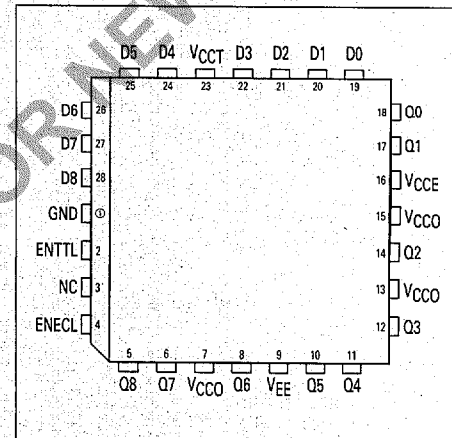
The H600 features both ECL and TTL logic enable controls for maximum flexibility.

The 10H version is compatible with MECL 10KH ECL logic levels. The 100H version is compatible with 100K levels.

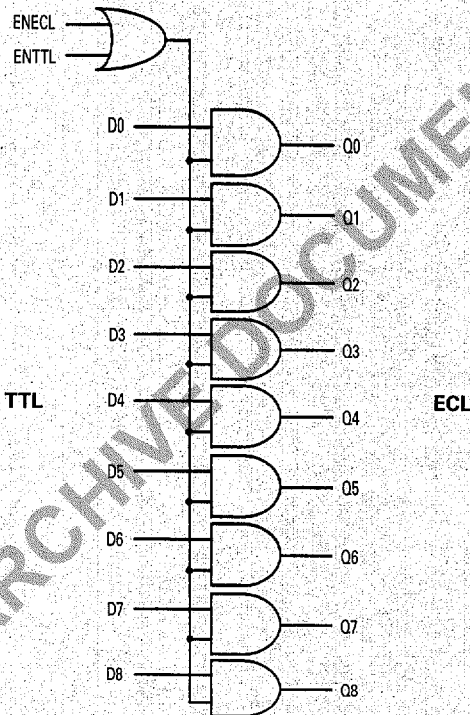
MC10H600
MC100H600

9-BIT
TTL-ECL
TRANSLATOR

PINOUT: 28-LEAD PLCC (TOP VIEW)



LOGIC SYMBOL



PIN NAMES

Pin	Function
GND	TTL Ground (0 V)
VCCE	ECL VCC (0 V)
VCC0	ECL VCC (0 V) — Outputs
VCCT	TTL Supply (+5.0 V)
VEE	ECL Supply (-5.2/-4.5 V)
D0-D8	Data Inputs (TTL)
Q0-Q8	Data Outputs (ECL)
ENECL	Enable Control (ECL)
ENTTL	Enable Control (TTL)

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DC CHARACTERISTICS: $V_{CC} = 5.0 \text{ V} \pm 10\%$; $V_{EE} = -5.2 \text{ V} \pm 5\%$ (10H version)
 $V_{EE} = -4.5 \text{ V} \pm 0.3 \text{ V}$ (100H version)

SYMBOL	PARAMETER		0°C		25°C		75°C		UNIT	CONDITION
			MIN	MAX	MIN	MAX	MIN	MAX		
I_{EE}	Power Supply Current	ECL		60		55		60	mA	
I_{CCH}		TTL		72		72		72	mA	
I_{CCL}				80		80		80	mA	

AC CHARACTERISTICS: $V_{CC} = 5.0 \text{ V} \pm 10\%$; $V_{EE} = -5.2 \text{ V} \pm 5\%$ (10H version)
 $V_{EE} = -4.5 \text{ V} \pm 0.3 \text{ V}$ (100H version)

SYMBOL	PARAMETER		0°C		25°C		75°C		UNIT	CONDITION
			MIN	MAX	MIN	MAX	MIN	MAX		
t_{PLH} t_{PHL}	Propagation Delay to Output			3.0		3.2		3.5	ns	50 Ω to -2.0 V
t_R t_F	Output Rise/Fall Time 20%–80%		0.5	1.5	0.5	1.5	0.5	1.5	ns	50 Ω to -2.0 V

TRUTH TABLE

ENECL	ENTTL	D	Q
H	X	H	H
H	X	L	L
X	H	H	H
X	H	L	L
L	L	X	L

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Product Preview

- 9-Bit Ideal for Byte-Parity Applications
- 3-State TTL Outputs
- Flow-Through Configuration
- Extra TTL and ECL Power Pins to Minimize Switching Noise
- ECL and TTL 3-State Control Inputs
- Dual Supply
- 4.0 ns max. Delay into 50 pF, 8.0 ns into 200 pF
- PNP TTL Inputs for Low Loading
- Choice of ECL Compatibility: MECL 10KH (10Hxxx) or 100K (100Hxxx)

The MC10H/100H601 is a 9-bit, dual supply ECL to TTL translator. Devices in the Motorola 9-bit translator series utilize the 28-lead PLCC for optimal power pinning, signal flow-through and electrical performance.

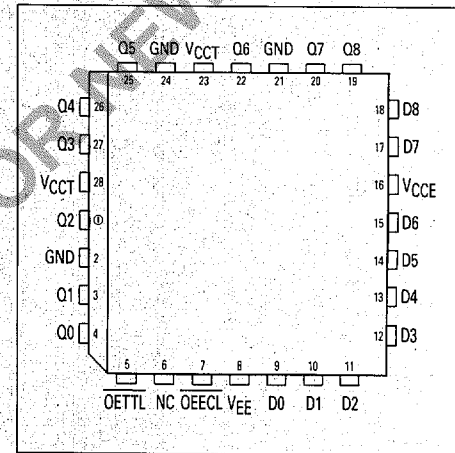
The devices feature a 48 mA TTL output stage, and AC performance is specified into both a 50 pF and 200 pF load capacitance. For the 3-state output disable, both ECL and TTL control inputs are provided, allowing maximum design flexibility.

The 10H version is compatible with MECL 10KH ECL logic levels. The 100H version is compatible with 100K levels.

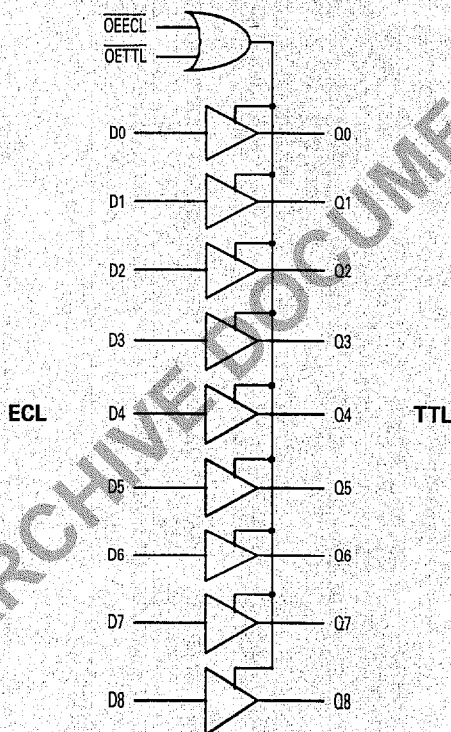
MC10H601
MC100H601

9-BIT
ECL-TTL
TRANSLATOR

PINOUT: 28-LEAD PLCC (TOP VIEW)



LOGIC SYMBOL



PIN NAMES

Pin	Function
GND	TTL Ground (0 V)
VCCE	ECL VCC (0 V)
VCCT	TTL Supply (+5.0 V)
VEE	ECL Supply (-5.2/-4.5 V)
D0-D8	Data Inputs (ECL)
Q0-Q8	Data Outputs (TTL)
OEEL	3-State Control (ECL)
OETTL	3-State Control (TTL)

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DC CHARACTERISTICS: $V_{CCT} = 5.0\text{ V} \pm 10\%$; $V_{EE} = -5.2\text{ V} \pm 5\%$ (10H version)
 $V_{EE} = -4.5\text{ V} \pm 0.3\text{ V}$ (100H version)

SYMBOL	PARAMETER		0°C		25°C		75°C		UNIT	CONDITION
			MIN	MAX	MIN	MAX	MIN	MAX		
I_{EE}	Power Supply Current	ECL		46		41		46	mA	
I_{CCH}		TTL		84		84		84	mA	
I_{CCL}				84		84		84	mA	
I_{CCZ}				88		88		88	mA	
I_{OS}	Output Short Circuit Current		-100	-225	-100	-225	-100	-225	mA	$V_{OUT} = 0\text{ V}$
I_{OZH}	Output Disable Current	HIGH		50		50		50	μA	$V_{OUT} = 2.7\text{ V}$
I_{OZL}		LOW		-50		-50		-50	μA	$V_{OUT} = 0.5\text{ V}$

See Page 10 for common DC characteristics.

AC CHARACTERISTICS: $V_{CCT} = 5.0\text{ V} \pm 10\%$; $V_{EE} = -5.2\text{ V} \pm 5\%$ (10H version)
 $V_{EE} = -4.5\text{ V} \pm 0.3\text{ V}$ (100H version)

SYMBOL	PARAMETER		0°C		25°C		75°C		UNIT	CONDITION
			MIN	MAX	MIN	MAX	MIN	MAX		
t_{PLH} t_{PHL}	Propagation Delay to Output			4.0		4.0		4.0	ns	$C_L = 50\text{ pF}$
				8.0		8.0		8.0	ns	$C_L = 200\text{ pF}$
t_{PLZ} t_{PHZ}	Output Disable Time			4.0		4.0		4.0	ns	$C_L = 50\text{ pF}$
				8.0		8.0		8.0	ns	$C_L = 200\text{ pF}$
t_{PZL} t_{PZH}	Output Enable Time			4.0		4.0		4.0	ns	$C_L = 50\text{ pF}$
				8.0		8.0		8.0	ns	$C_L = 200\text{ pF}$
t_R t_F	Output Rise/Fall Time 1.0 V–2.0 V			1.2		1.2		1.2	ns	$C_L = 50\text{ pF}$
				3.0		3.0		3.0	ns	$C_L = 200\text{ pF}$

TRUTH TABLE

OEECL	OETTL	D	Q
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

Product Preview

- 9-Bit Ideal for Byte-Parity Applications
- Flow-Through Configuration
- Extra TTL and ECL Power/Ground Pins to Minimize Switching Noise
- Dual Supply
- 4.0 ns max. D to Q
- PNP TTL Inputs for Low Loading
- Choice of ECL Compatibility: MECL 10KH (10Hxxx) or 100K (100Hxxx)

The MC10H/100H602 is a 9-bit, dual supply TTL to ECL translator with latch. Devices in the Motorola 9-bit translator series utilize the 28-lead PLCC for optimal power pinning, signal flow-through and electrical performance.

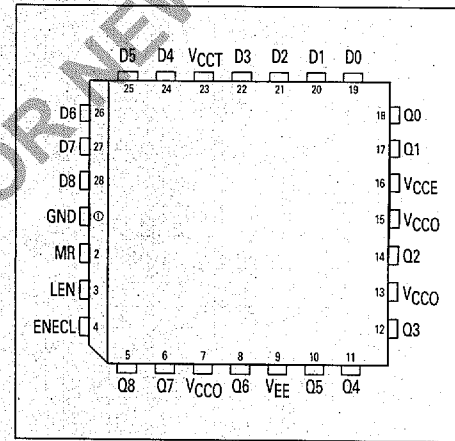
The H602 features D-type latches. Latching is controlled by Latch Enable (LEN), while the Master Reset input resets the latches. A post-latch logic enable is also provided (ENECL), allowing control of the output state without destroying latch data. All control inputs are ECL level.

The 10H version is compatible with MECL 10KH ECL logic levels. The 100H version is compatible with 100K levels.

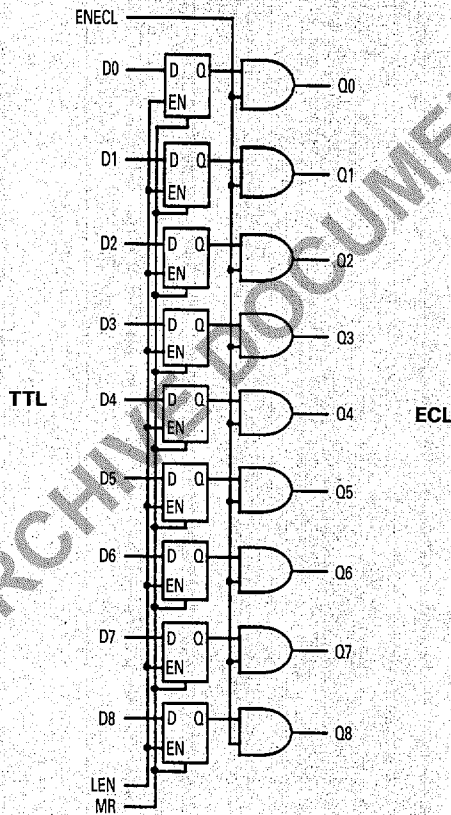
MC10H602
MC100H602

**9-BIT LATCH/
TTL-ECL
TRANSLATOR**

PINOUT: 28-LEAD PLCC (TOP VIEW)



LOGIC SYMBOL



PIN NAMES

Pin	Function
GND	TTL Ground (0 V)
VCC0	ECL VCC (0 V)
VCC0	ECL VCC (0 V) — Outputs
VCCT	TTL Supply (+5.0 V)
VEE	ECL Supply (-5.2/-4.5 V)
D0-D8	Data Inputs (TTL)
Q0-Q8	Data Outputs (ECL)
ENECL	Enable Control (ECL)
LEN	Latch Enable (ECL)
MR	Master Reset (ECL)

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DC CHARACTERISTICS: $V_{CCT} = 5.0\text{ V} \pm 10\%$; $V_{EE} = -5.2\text{ V} \pm 5\%$ (10H version)
 $V_{EE} = -4.5\text{ V} \pm 0.3\text{ V}$ (100H version)

SYMBOL	PARAMETER		0°C		25°C		75°C		UNIT	CONDITION
			MIN	MAX	MIN	MAX	MIN	MAX		
I_{EE}	Power Supply Current	ECL		66		61		66	mA	
I_{CCH}		TTL		72		72		72	mA	
I_{CCL}				80		80		80	mA	

See Page 10 for common DC characteristics.

AC CHARACTERISTICS: $V_{CCT} = 5.0\text{ V} \pm 10\%$; $V_{EE} = -5.2\text{ V} \pm 5\%$ (10H version)
 $V_{EE} = -4.5\text{ V} \pm 0.3\text{ V}$ (100H version)

SYMBOL	PARAMETER		0°C		25°C		75°C		UNIT	CONDITION
			MIN	MAX	MIN	MAX	MIN	MAX		
t_{PLH} t_{PHL}	Propagation Delay to Output	D		3.5		3.7		4.0	ns	
		LEN		4.5		4.2		4.5		
		MR		4.0		4.2		4.5		
		ENECL		2.0		2.2		2.5		
t_s	Set-Up Time, D to LEN		2.0		2.0		2.0		ns	
t_h	Hold Time, D to LEN		1.0		1.0		1.0		ns	
$t_w(L)$	LEN Pulse Width, LOW		2.0		2.0		2.0		ns	
t_R t_F	Output Rise/Fall Time 20%–80%		0.5	1.5	0.5	1.5	0.5	1.5	ns	

TRUTH TABLE

D	LEN	MR	ENECL	Q
L	L	X	H	L
H	L	X	H	H
X	H	L	H	Q_0
X	X	H	H	L
X	X	X	L	L

Product Preview

- 9-Bit Ideal for Byte-Parity Applications
- 3-State TTL Outputs
- Flow-Through Configuration
- Extra TTL and ECL Power Pins to Minimize Switching Noise
- Dual Supply
- 4.5 ns max. Delay into 50 pF, 9.0 ns into 200 pF
- PNP TTL Inputs for Low Loading
- Choice of ECL Compatibility: MECL 10KH (10Hxxx) or 100K (100Hxxx)

The MC10H/100H603 is a 9-bit, dual supply ECL to TTL translator. Devices in the Motorola 9-bit translator series utilize the 28-lead PLCC for optimal power pinning, signal flow-through and electrical performance.

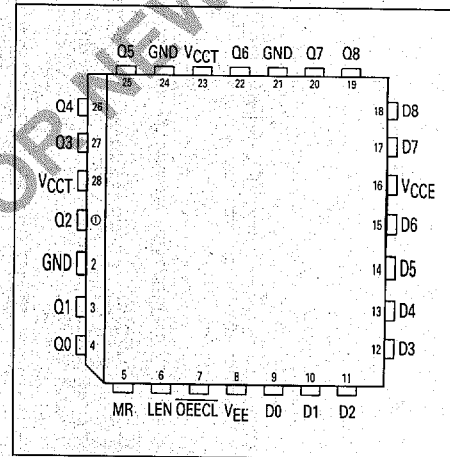
The devices feature a 48 mA TTL output stage, and AC performance is specified into both a 50 pF and 200 pF load capacitance. Latching is controlled by Latch Enable (LEN), and Master Reset (MR) resets the latches. A HIGH on $\overline{OE}ECL$ sends the outputs into the high impedance state. All control inputs are ECL level.

The 10H version is compatible with MECL 10KH ECL logic levels. The 100H version is compatible with 100K levels.

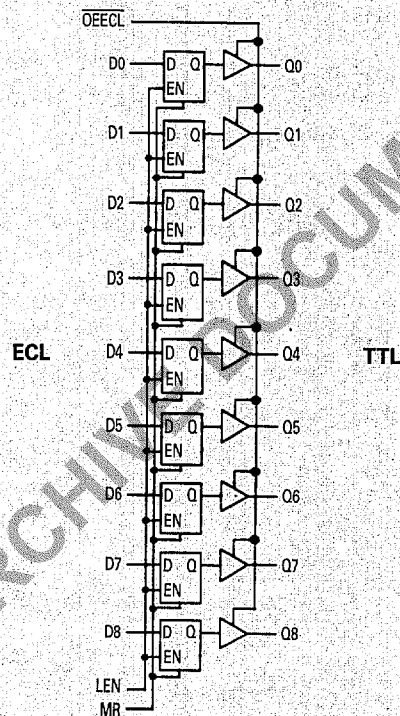
MC10H603 MC100H603

9-BIT LATCH/ ECL-TTL TRANSLATOR

PINOUT: 28-LEAD PLCC (TOP VIEW)



LOGIC SYMBOL



PIN NAMES

Pin	Function
GND	TTL Ground (0 V)
VCCE	ECL VCC (0 V)
VCCT	TTL Supply (+5.0 V)
VEE	ECL Supply (-5.2/-4.5 V)
D0-D8	Data Inputs (ECL)
Q0-Q8	Data Outputs (TTL)
$\overline{OE}ECL$	3-State Control (ECL)
LEN	Latch Enable (ECL)
MR	Master Reset (ECL)

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DC CHARACTERISTICS: $V_{CCT} = 5.0\text{ V} \pm 10\%$; $V_{EE} = -5.2\text{ V} \pm 5\%$ (10H version)
 $V_{EE} = -4.5\text{ V} \pm 0.3\text{ V}$ (100H version)

SYMBOL	PARAMETER		0°C		25°C		75°C		UNIT	CONDITION
			MIN	MAX	MIN	MAX	MIN	MAX		
I_{EE}	Power Supply Current	ECL		65		61		65	mA	
I_{CCH}		TTL		84		84		84	mA	
I_{CCL}				84		84		84	mA	
I_{CCZ}				88		88		88	mA	
I_{OS}	Output Short Circuit Current		-100	-225	-100	-225	-100	-225	mA	$V_{OUT} = 0\text{ V}$
I_{OZH}	Output Disable Current	HIGH		50		50		50	μA	$V_{OUT} = 2.7\text{ V}$
I_{OZL}		LOW		-50		-50		-50	μA	$V_{OUT} = 0.5\text{ V}$

See Page 10 for common DC characteristics.

AC CHARACTERISTICS: $V_{CCT} = 5.0\text{ V} \pm 10\%$; $V_{EE} = -5.2\text{ V} \pm 5\%$ (10H version)
 $V_{EE} = -4.5\text{ V} \pm 0.3\text{ V}$ (100H version)

SYMBOL	PARAMETER		0°C		25°C		75°C		UNIT	CONDITION
			MIN	MAX	MIN	MAX	MIN	MAX		
t_{PLH} t_{PHL}	Propagation Delay to Output	D		4.5 9.0		4.5 9.0		4.5 9.0	ns	$C_L = 50\text{ pF}$ $C_L = 200\text{ pF}$
		LEN		5.0 9.5		5.0 9.5		5.0 9.5	ns	$C_L = 50\text{ pF}$ $C_L = 200\text{ pF}$
		MR		5.1 9.7		5.1 9.7		5.1 9.7	ns	$C_L = 50\text{ pF}$ $C_L = 200\text{ pF}$
t_s t_h $t_w(L)$	Set-Up Time, D to LEN Hold Time, D to LEN LEN Pulse Width, LOW		1.5 0.8 2.0		1.5 0.8 2.0		1.5 0.8 2.0		ns ns ns	
t_{PLZ} t_{PHZ}	Output Disable Time			4.0 8.0		4.0 8.0		4.0 8.0	ns ns	$C_L = 50\text{ pF}$ $C_L = 200\text{ pF}$
t_{PZL} t_{PZH}	Output Enable Time			4.0 8.0		4.0 8.0		4.0 8.0	ns ns	$C_L = 50\text{ pF}$ $C_L = 200\text{ pF}$
t_R t_F	Output Rise/Fall Time 1.0 V–2.0 V			1.2 3.0		1.2 3.0		1.2 3.0	ns ns	$C_L = 50\text{ pF}$ $C_L = 200\text{ pF}$

TRUTH TABLE

D	LEN	MR	\overline{OEECL}	Q
L	L	X	L	L
H	L	X	L	H
X	H	L	L	Q_0
X	X	H	L	L
X	X	X	H	Z

**MC10H/100H600
MC10H/100H601
MC10H/100H602
MC10H/100H603**

COMMON DC SPECIFICATIONS

10H ECL DC CHARACTERISTICS: $V_{CCT} = 5.0 \text{ V} \pm 10\%$; $V_{EE} = -5.2 \text{ V} \pm 5\%$

SYMBOL	PARAMETER	0°C		25°C		75°C		UNIT	CONDITION
		MIN	MAX	MIN	MAX	MIN	MAX		
I_{IH} I_{IL}	Input HIGH Current Input LOW Current		225 1.5		145 1.0		145 1.0	μA mA	
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	-1170 -1950	-840 -1480	-1130 -1950	-810 -1480	-1070 -1950	-735 -1450	mV	
V_{OH} V_{OL}	Output HIGH Voltage Output LOW Voltage	-1020 -1950	-840 -1630	-980 -1950	-810 -1630	-920 -1950	-735 -1600	mV	50 Ω to -2.0 V

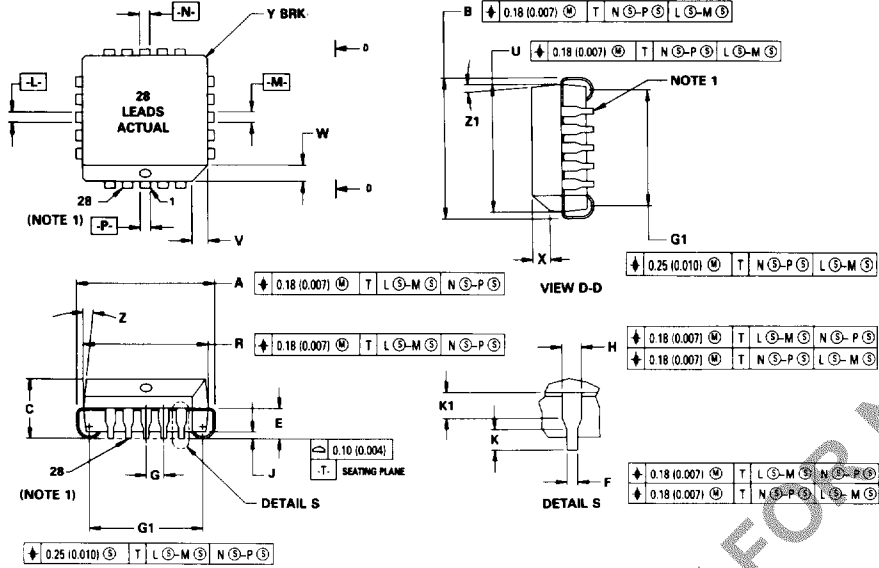
100H ECL DC CHARACTERISTICS: $V_{CCT} = 5.0 \text{ V} \pm 10\%$; $V_{EE} = -4.5 \text{ V} \pm 0.3 \text{ V}$

SYMBOL	PARAMETER	0°C		25°C		75°C		UNIT	CONDITION
		MIN	MAX	MIN	MAX	MIN	MAX		
I_{IH} I_{IL}	Input HIGH Current Input LOW Current		225 1.5		145 1.0		145 1.0	μA mA	
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	-1165 -1810	-880 -1475	-1165 -1810	-880 -1475	-1165 -1810	-880 -1475	mV	
V_{OH} V_{OL}	Output HIGH Voltage Output LOW Voltage	-1025 -1810	-880 -1620	-1025 -1810	-880 -1620	-1025 -1810	-880 -1620	mV	50 Ω to -2.0 V

TTL DC CHARACTERISTICS: $V_{CCT} = 5.0 \text{ V} \pm 10\%$; $V_{EE} = -5.2 \text{ V} \pm 5\%$ (10H version)
 $V_{EE} = -4.5 \text{ V} \pm 0.3 \text{ V}$ (100H version)

SYMBOL	PARAMETER	0°C		25°C		75°C		UNIT	CONDITION
		MIN	MAX	MIN	MAX	MIN	MAX		
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	2.0	0.8	2.0	0.8	2.0	0.8	V V	
I_{IH}	Input HIGH Current		20 100		20 100		20 100	μA	$V_{IN} = 2.7 \text{ V}$ $V_{IN} = 7.0 \text{ V}$
I_{IL}	Input LOW Current		-0.6		-0.6		-0.6	mA	$V_{IN} = 0.5 \text{ V}$
V_{IK}	Input Clamp Voltage		-1.2		-1.2		-1.2	V	$I_{IN} = -18 \text{ mA}$
V_{OH}	Output HIGH Voltage	2.0	2.5	2.0	2.5	2.0	2.5	V V	$I_{OH} = -3.0 \text{ mA}$ $I_{OH} = -15 \text{ mA}$
V_{OL}	Output LOW Voltage		0.55		0.55		0.55	V	$I_{OL} = 48 \text{ mA}$

OUTLINE DIMENSIONS



- NOTES:
1. DUE TO SPACE LIMITATION, CASE 776-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 28 LEADS.
 2. DATUMS -L-, -M-, -N- AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
 3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
 4. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
 5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 6. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.32	12.57	0.485	0.495
B	12.32	12.57	0.485	0.495
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51		0.020	
K	0.64		0.025	
R	11.43	11.58	0.450	0.456
U	11.43	11.58	0.450	0.456
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y		0.50		0.020
Z	2°	10°	2°	10°
G1	10.42	10.92	0.410	0.430
K1	1.02		0.040	
Z1	2°	10°	2°	10°

FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

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