MSP430F13x/14x/14x1 Device Erratasheet

1 Current Version

See Appendix A for prior silicon revisions.

✓ The checkmark means that the issue is present in that revision.

* Devices with revisions marked with (*) use BSL version 1.61. For specific information on this version of the BSL and its proper usage, see the *MSP430 Memory Programming User's Guide* (SLAU265).

Device	Rev:	ADC1	ADC5	ADC7	ADC8	ADC9	ADC10	ADC18	ADC25	BCL5	BSL3	BSL4	BSL5	CPU4	PORT3	RES3	RES4	TA12	TA16	TAB22	TB1	TB2
MSP430F133	N	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	S	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AA*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AB*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AD*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AE	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F135	N	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	S	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AA*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AB*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AD*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AE	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F147	N	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	S	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AA*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AB*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AD*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AE	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F1471	N								✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	S								✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AA*								✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AB*								✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AD*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AE	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F148	N	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	S	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AA*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AB*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AD*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AE	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Device	Rev:	ADC1	ADC5	ADC7	ADC8	ADC9	ADC10	ADC18	ADC25	BCL5	BSL3	BSL4	BSL5	CPU4	PORT3	RES3	RES4	TA12	TA16	TAB22	TB1	TB2
MSP430F1481	N								✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	S								✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AA*								✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AB*								✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AD*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AE	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F149	N	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	S	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AA*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AB*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AD*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AE	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F1491	N								✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	S								✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AA*								✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AB*								✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AD*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AE	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

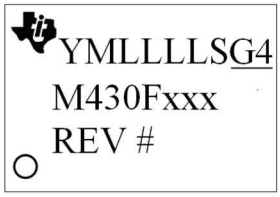
Devices	Rev:	TB2	TB3	TB4	TB14	TB16	US13	US14	US15	WDG2
MSP430F133	N	✓	✓	✓	✓	✓	✓	✓	✓	✓
	S	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AA*	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AB*	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AD*	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AE	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F135	N	✓	✓	✓	✓	✓	✓	✓	✓	✓
	S	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AA*	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AB*	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AD*	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AE	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F147	N	✓	✓	✓	✓	✓	✓	✓	✓	✓
	S	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AA*	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AB*	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AD*	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AE	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F1471	N	✓	✓	✓	✓	✓	✓	✓	✓	✓
	S	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AA*	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AB*	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AD*	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AE	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F148	N	✓	✓	✓	✓	✓	✓	✓	✓	✓
	S	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AA*	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AB*	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AD*	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AE	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F1481	N	✓	✓	✓	✓	✓	✓	✓	✓	✓
	S	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AA*	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AB*	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AD*	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AE	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F149	N	✓	✓	✓	✓	✓	✓	✓	✓	✓
	S	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AA*	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AB*	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AD*	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AE	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F1491	N	✓	✓	✓	✓	✓	✓	✓	✓	✓
	S	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AA*	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AB*	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AD*	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AE	✓	✓	✓	✓	✓	✓	✓	✓	✓

2 Package Markings

PAG64

TQFP (PAG), 64 Pin

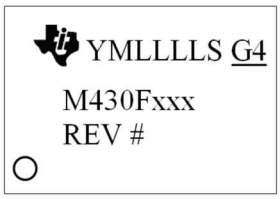
YM = Year and Month Date Code
LLLL = LOT Trace Code
S = Assembly Site Code
# = DIE Revision
o = PIN 1



YM = Year and Month Date Code
LLLL = LOT Trace Code
S = Assembly Site Code
# = DIE Revision
o = PIN 1

PM64

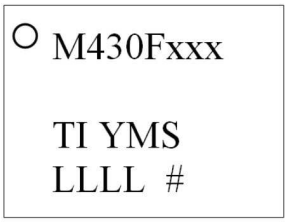
LQFP (PM), 64 Pin



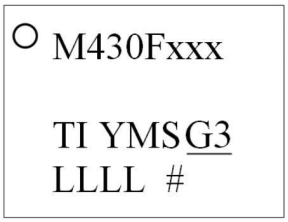
YM = Year and Month Date Code
LLLL = LOT Trace Code
S = Assembly Site Code
# = DIE Revision
o = PIN 1

RTD64

QFN (RTD), 64 Pin



TI = TI
YM = Year and Month Date Code
LLLL = LOT Trace Code
S = Assembly Site Code
# = DIE Revision
o = PIN 1



TI = TI
YM = Year and Month Date Code
LLLL = LOT Trace Code
S = Assembly Site Code
# = DIE Revision
o = PIN 1

3 Detailed Bug Description

ADC1 *ADC12 Module*

Function Start of conversion

Description In single conversion/sequence mode (CONSEQ = 0/1), the next conversion can be started with ADC12SC. It is not necessary to clear ENC before setting ADC12SC. This is contrary to the specification.

Workaround None

ADC5 *ADC12 Module*

Function Interrupt flag register

Description ADC12 interrupt flag may not be set when the CPU simultaneously accesses the ADC12IFG register.

Workaround There is no need to access the interrupt flag register to process interrupt situations. Use the ADC12IV register to identify the interrupt event. The corresponding flag bits are reset automatically. Additional details are discussed in the device family user's guide.

ADC7 *ADC12 Module*

Function Conversion time overflow

Description The timing overflow flag is set when the device is in sequence mode (CONSEQ = 1 or 3) and MSC = 0, even if no overflow has occurred.

Workaround Verify correct timing and do not enable Conversion-Time Overflow interrupt.

ADC8 *ADC12 Module*

Function Interrupt flag register

Description Clearing flags in the interrupt flag register with a CPU instruction does not clear the latest interrupt flag.

Workaround Clear interrupt flags by accessing the conversion memory registers.

ADC9 *ADC12 Module*

Function Interrupt vector register

Description If the ADC12 uses a different clock than the CPU (MCLK) and more than one ADC interrupt is enabled, the ADC12IV register content may be unpredictable for one clock cycle. This happens if, during the execution of an ADC interrupt, another ADC interrupt with higher priority occurs.

Workaround

- Read out ADC12IV twice and use only when values are equal.
  or
- Use ADC12IFG to determine which interrupt has occurred.

ADC10 *ADC12 Module*

Function Unintended start of conversion

Description Accessing ADC12OVIE or ADC12TOVIE at the end of an ADC12 conversion with BIS/BIC commands can cause the ADC12SC bit to be set again immediately after it was cleared. This might start another conversion, if ADC12SC is configured to trigger the ADC (SHS = 0).

Workaround If ADC12SC is configured to trigger the ADC, the control bits ADC12OVIE and ADC12TOVIE should be modified only when the ADC is not busy (ADC12BUSY = 0).

ADC18 *ADC12 Module*

Function Incorrect conversion result in extended sample mode

Description The ADC12 conversion result can be incorrect if the extended sample mode is selected (SHP = 0), the conversion clock is not the internal ADC12 oscillator (ADC12SSEL > 0), and one of the following two conditions is true:

- The extended sample input signal SHI is asynchronous to the clock source used for ADC12CLK and the undivided ADC12 input clock frequency exceeds 3.15 MHz.
  or
- The extended sample input signal SHI is synchronous to the clock source used for ADC12CLK and the undivided ADC12 input clock frequency exceeds 6.3 MHz.

Workaround

- Use the pulse sample mode (SHP = 1).
  or
- Use the ADC12 internal oscillator as the ADC12 clock source.
  or
- Limit the undivided ADC12 input clock frequency to 3.15 MHz.
  or
- Use the same clock source (such as ACLK or SMCLK) to derive both SHI and ADC12CLK, to achieve synchronous operation, and also limit the undivided ADC12 input clock frequency to 6.3 MHz.

ADC25 *ADC12 Module*

Function Write to ADC12CTL0 triggers ADC12 when CONSEQ = 00

Description If ADC conversions are triggered by the Timer_B module and the ADC12 is in single-channel single-conversion mode (CONSEQ = 00), ADC sampling is enabled by write access to any bit(s) in the ADC12CTL0 register. This is contrary to the expected behavior that only the ADC12 enable conversion bit (ADC12ENC) triggers a new ADC12 sample.

Workaround When operating the ADC12 in CONSEQ = 00 and a Timer_B output is selected as the sample and hold source, temporarily clear the ADC12ENC bit before writing to other bits in the ADC12CTL0 register. The following capture trigger can then be re-enabled by setting ADC12ENC = 1.

BCL5 *Basic Clock Module*

Function RSELx bit modifications can generate high-frequency spikes on MCLK

Description When DIVMx = 00 or 01, the RSELx bits of the Basic Clock module are incremented or decremented in steps of 2 or greater, the DCO output may momentarily generate high-frequency spikes on MCLK, which may corrupt CPU operation. This is not an issue when DIVMx = 10 or 11.

Workaround Set DIVMx = 10 or 11 to divide the MCLK input prior to modifying RSELx. After the RSELx bits are configured as desired, the DIVMx setting can be changed back to the original selection.

BSL3 *Bootstrap Loader Module*

Function Receiving frames

Description Receiving frames with a checksum value equal to a legal address can change the content of this address or the bootstrap loader may stop operation.

Workaround Software workaround is available.

BSL4 *Bootstrap Loader Module*

Function Flash memory cannot be programmed

Description The bootstrap loader software cannot program the flash memory.

Workaround Software workaround is available.

BSL5 *Bootstrap Loader Module*

Function $\overline{\text{RST}}$/NMI configured as NMI

Description If the $\overline{\text{RST}}$/NMI pin is configured to NMI, the bootstrap loader may not be started. Unpredictable operation results.

Workaround None

CPU4 *CPU Module*

Function PUSH #4, PUSH #8

Description The single operand instruction PUSH cannot use the internal constants (CG) 4 and 8. The other internal constants (0, 1, 2, –1) can be used. The number of clock cycles is different:

PUSH #CG uses address mode 00, requiring 3 cycles, 1-word instruction

PUSH #4/#8 uses address mode 11, requiring 5 cycles, 2-word instruction

Workaround Workaround implemented in assembler. No fix planned.

PORT3 — *Digital I/O Module, Port 1/2*

Function Port interrupts can be lost

Description Port interrupts can be lost if they occur during CPU access of the P1IFG and P2IFG registers.

Workaround None

RES3 — *General, Reset*

Function Reset

Description When $\overline{\text{RST}}$/NMI is held low during power up of V_{CC}, some internal drivers are not reset correctly. This may result in a high I_{CC} current until the internal power-on signal has generated one clock cycle to reset the internal drivers. This limits the time when the excess current can occur to the time the power-up circuit is active.

Workaround None

RES4 — *General, Reset*

Function No reset if external resistor exceeds certain value

Description No reset of the device is performed if the external pulldown resistor on $\overline{\text{RST}}$/NMI pin is above a certain limit. The limits are:

V_{CC} = 1.8 V: maximum pulldown resistor = 12 kΩ
V_{CC} = 3.0 V: maximum pulldown resistor = 5 kΩ
V_{CC} = 3.6 V: maximum pulldown resistor = 2.5 kΩ

In addition, a higher current consumption occurs during high/low $\overline{\text{RST}}$/NMI signal transition when using improper resistors.

Workaround Use external pulldown resistors below the listed values or directly drive $\overline{\text{RST}}$/NMI low to generate a reset.

TA12 — *Timer_A Module*

Function Interrupt is lost (slow ACLK)

Description Timer_A counter is running with slow clock (external TACLK or ACLK) compared to MCLK. The compare mode is selected for the capture/compare channel and the CCRx register is incremented by one with the occurring compare interrupt (if TAR = CCRx).

Due to the fast MCLK, the CCRx register increment (CCRx = CCRx + 1) happens before the Timer_A counter has incremented again. Therefore, the next compare interrupt should happen at once with the next Timer_A counter increment (if TAR = CCRx + 1). This interrupt is lost.

Workaround Switch capture/compare mode to capture mode before the CCRx register increment. Switch back to compare mode afterward.

TA16 *Timer_A Module*

Function First increment of TAR erroneous when IDx > 00

Description The first increment of TAR after any timer clear event (POR/TACLR) happens immediately following the first positive edge of the selected clock source (INCLK, SMCLK, ACLK, or TACLK). This is independent of the clock input divider settings (ID0, ID1). All following TAR increments are performed correctly with the selected IDx settings.

Workaround None

TAB22 *Timer_A/Timer_B Module*

Function Timer_A/B register modification after Watchdog Timer PUC

Description Unwanted modification of the Timer_A/B registers TACTL and TAIV can occur when a PUC is generated by the Watchdog Timer (WDT) in watchdog mode and any Timer_A/B counter register TACCRx/TBCCRx is incremented/decremented (Timer_A/B does not need to be running).

Workaround Initialize TACTL/TBCTL register after the reset occurs using a MOV instruction (BIS/BIC may not fully initialize the register). TAIV/TBIV is automatically cleared following this initialization.

Example code:

```
MOV.W #VAL, &TACTL
```

or

```
MOV.W #VAL, &TBCTL
```

Where, VAL = 0, if Timer is not used in application; otherwise, user defined per desired function.

TB1 *Timer_B Module*

Function "Equal mode" when grouping compare latches

Description The "equal mode" for loading the compare latches (CLLD = 3) cannot be used when compare latches are grouped (TBCLGRP > 0).

Workaround None

TB2 *Timer_B Module*

Function Interrupt is lost (slow ACLK)

Description Timer_B counter is running with slow clock (external TBCLK or ACLK) compared to MCLK. The compare mode is selected for the capture/compare channel and the CCRx register is incremented by 1 with the occurring compare interrupt (if TBR = CCRx).

Due to the fast MCLK, the CCRx register increment (CCRx = CCRx + 1) happens before the Timer_B counter has incremented again. Therefore, the next compare interrupt should happen at once with the next Timer_B counter increment (if TBR = CCRx + 1). This interrupt is lost.

Workaround Switch capture/compare mode to capture mode before the CCRx register increment. Switch back to compare mode afterward.

TB3 *Timer_B Module*

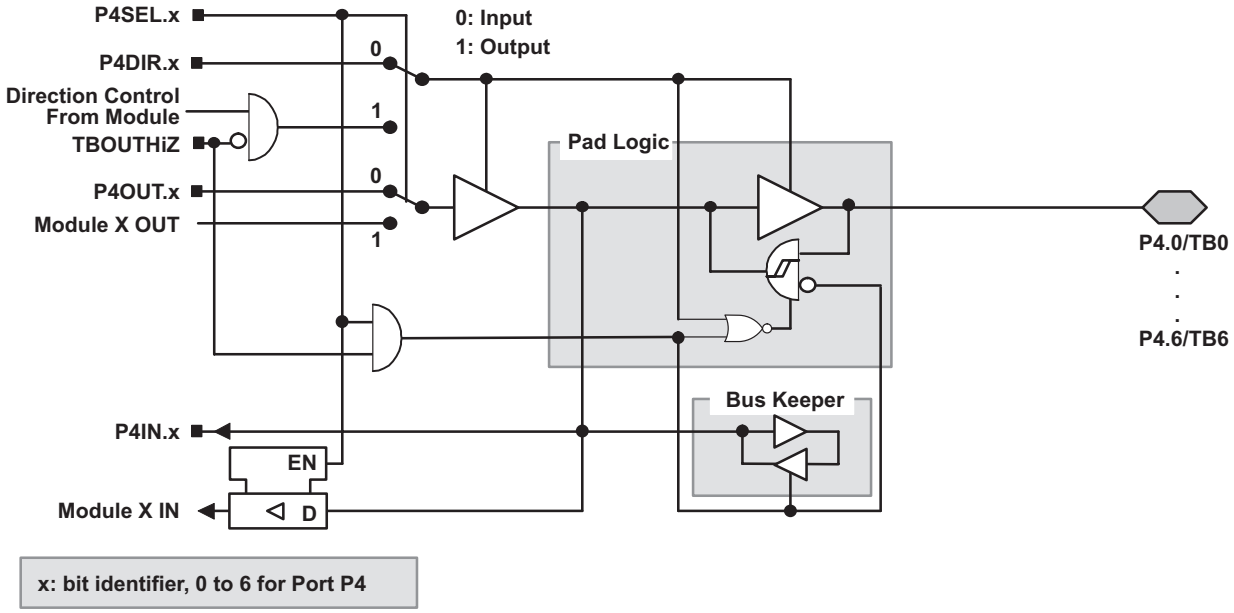
Function Port is switched to 3-state independent of selected function

Description Incorrect 3-state function of Ports P4.0/TB0 through P4.6/TB6 (TBoutHiZ control). If TBoutHiZ is set to high, all ports P4.0/TB0 through P4.6/TB6 are set to 3-state, independent of the P4SEL.x control signals. This means a port P4.x is switched to 3-state with TBoutHiZ, even if it is not selected for Timer_B function. In addition, the ports P4.0/TB0 through P4.6/TB6 are switched to 3-state with TBoutHiZ, even if the port direction (direction control from module) is set to input. This is in accordance with the specification description but, nevertheless, is an unexpected behavior.

Workaround None

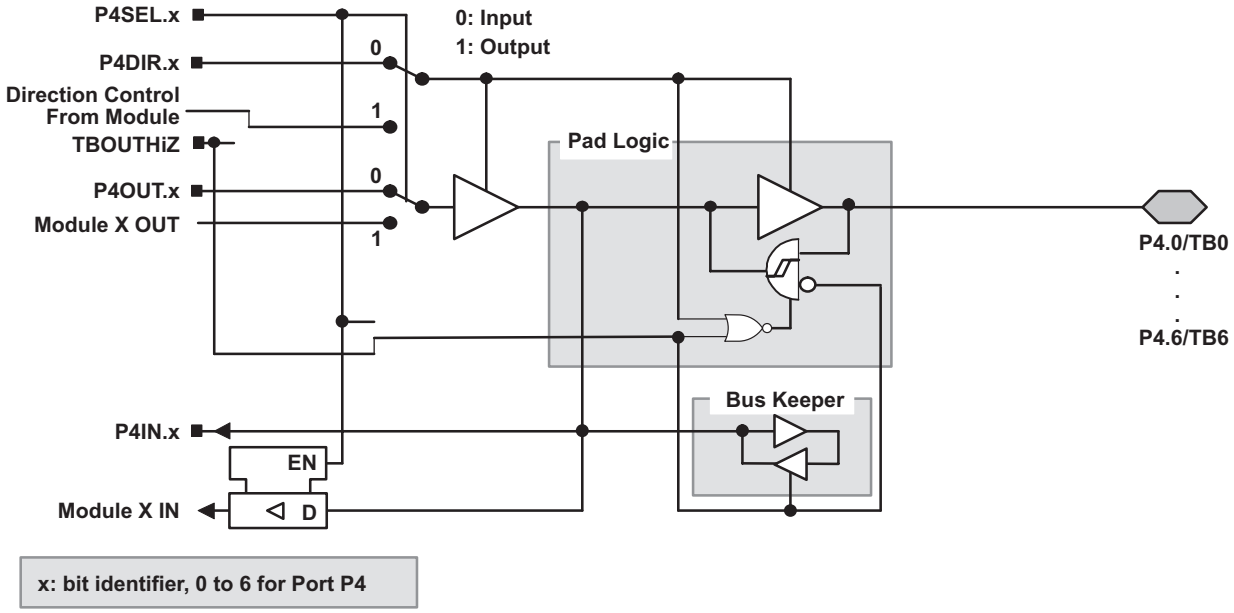
Port Function as Specified

port P4, P4.0 to P4.6, input/output with Schmitt-trigger



Port Realization With TB3 Bug

port P4, P4.0 to P4.6, input/output with Schmitt-trigger



TB4 *Timer_B Module*

Function Group function

Description If the shadow registers are organized in groups (SHR = 1, 2, or 3), one shadow register is not loaded correctly. This happens when the last CCRx register within a group is loaded at exactly the same time that the timer counter reaches the event for loading the shadow registers (TBR = 0 or TBR = CCR0).

Workaround Ensure that all CCRx registers within a group are loaded before the shadow register load event occurs.

TB14 *Timer_B Module*

Function PWM output

Description The PWM output unit may behave erroneously if the condition for changing the PWM output (EQUx or EQU0) and the condition for loading the shadow register TBCLx happen at the same time. Depending on the load condition for the shadow registers (CLLD bits in TBCCTLx), there are four possible error conditions:

1. Change CCRx register from any value to CCRx = 0
   (for example, sequence for CCRx = 4 3 2 0 0 0)
2. Change CCRx register from CCRx = 0 to any value
   (for example, sequence for CCRx = 0 0 0 2 3 4)
3. Change CCRx register from any value to current SHD0 (CCR0) value
   (for example, sequence for CCRx = 4 2 5 SHD0 3 8)
4. Change CCRx register from current SHD0 (CCR0) value to any value
   (for example, sequence for CCRx = 4 2 SHD0 5 3 8)

Workaround No general workaround available

TB16 *Timer_B Module*

Function First increment of TBR erroneous when IDx > 00

Description The first increment of TBR after any timer clear event (POR/TBCLR) happens immediately following the first positive edge of the selected clock source (INCLK, SMCLK, ACLK, or TBCLK). This is independent of the clock input divider settings (ID0, ID1). All following TBR increments are performed correctly with the selected IDx settings.

Workaround None

US13 *USART0, USART1 Module*

Function Unpredictable program execution

Description USART interrupts requested by URXS can result in unpredictable program execution if this request is not served within two bit times of the received data.

Workaround Ensure that the interrupt service routine is entered within two bit times of the received data.

US14 *USART0, USART1 Module*

Function Lost character start edge

Description When using the USART in UART mode with UxBR0 = 0x03 and UxBR1 = 0x00, the start edge of received characters may be ignored due to internal timing conflicts within the UART state machine. This condition does not apply when UxBR0 > 0x03.

Workaround None

US15 *USART0, USART1 Module*

Function UART receive with two stop bits

Description USART hardware does not detect a missing second stop bit when SPB = 1. The framing error flag (FE) is not set under this condition, and erroneous data reception may occur.

Workaround None (configure USART for a single stop bit, SPB = 0)

WDG2 *Watchdog Module*

Function Incorrectly accessing a flash control register

Description If a key violation is caused by incorrectly accessing a flash control register, the watchdog interrupt flag is set in addition to a correctly generated PUC.

Workaround None

Appendix A Prior Versions

✓ The checkmark means that the issue is present in that revision.

* Devices with revisions marked with (*) use BSL version 1.61. For specific information on this version of the BSL and its proper usage, see the *Memory Programming User's Guide* (SLAU265).

Device	Rev:	ADC1	ADC5	ADC7	ADC8	ADC9	ADC10	ADC11	ADC18	ADC25	BCL5	BSL3	BSL4	BSL5	CPU4	PORT3	RES3	RES4	TA12	TA16	TAB22
MSP430F133	L	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	M	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	N	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Q	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	O	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	S	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AA*	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AB*	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AD*	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AE	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F135	L	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	M	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	N	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Q	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	O	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	S	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AA*	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AB*	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AD*	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AE	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F147	L	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	M	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	N	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Q	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	O	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	S	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AA*	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AB*	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AD*	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AE	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F1471	L									✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	M									✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	N									✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Q									✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	O									✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	S									✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AA*									✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AB*									✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AD*									✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AE									✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Device	Rev:	ADC1	ADC5	ADC7	ADC8	ADC9	ADC10	ADC11	ADC18	ADC25	BCL5	BSL3	BSL4	BSL5	CPU4	PORT3	RES3	RES4	TA12	TA16	TAB22
MSP430F148	L	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	M	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	N	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Q	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	O	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	S	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AA*	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AB*	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AD*	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AE	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F1481	L									✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	M									✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	N									✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Q									✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	O									✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	S									✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AA*									✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AB*									✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AD*									✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AE									✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F149	L	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	M	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	N	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Q	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	O	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	S	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AA*	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AB*	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AD*	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AE	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F1491	L									✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	M									✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	N									✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Q									✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	O									✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	S									✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AA*									✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AB*									✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AD*									✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AE									✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Device	Rev:	TB1	TB2	TB3	TB4	TB14	TB16	US13	US14	US15	WDG2
MSP430F133	L	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	M	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	N	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Q	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	O	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	S	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AA*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AB*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AD*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AE	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F135	L	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	M	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	N	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Q	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	O	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	S	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AA*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AB*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AD*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AE	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F147	L	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	M	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	N	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Q	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	O	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	S	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AA*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AB*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AD*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AE	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F1471	L	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	M	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	N	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Q	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	O	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	S	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AA*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AB*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AD*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AE	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Device	Rev:	TB1	TB2	TB3	TB4	TB14	TB16	US13	US14	US15	WDG2
MSP430F148	L	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	M	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	N	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Q	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	O	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	S	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AA*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AB*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AD*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AE	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F1481	L	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	M	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	N	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Q	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	O	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	S	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AA*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AB*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AD*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AE	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F149	L	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	M	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	N	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Q	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	O	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	S	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AA*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AB*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AD*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AE	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F1491	L	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	M	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	N	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Q	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	O	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	S	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AA*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AB*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AD*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AE	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

A.1 Detailed Bug Description

ADC11	*ADC12 Module*
Function	Temporary leakage current after conversion
Description	The ADC12 causes temporary leakage current after a completed conversion. Duration and magnitude of the leakage current depends on parasitic effects.
Workaround	None

Revision History

Changes from D Revision (May 2010) to E Revision **Page**

- Added silicon revisions AD and AE to Current Version table; revisions AA, AB, AD marked with BSL version 1.61. 1
- Added silicon revisions AD and AE to Prior Versions table; revisions AA, AB, AD marked with BSL version 1.61. 13

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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