- **Low Supply-Voltage Range: 1.8 V to 3.6 V**
- **Ultralow-Power Consumption:**
  - **Active Mode: 400 μA at 1 MHz, 2.2 V**
  - **Standby Mode: 1.3 μA**
  - **Off Mode (RAM Retention): 0.22 μA**
- **Five Power-Saving Modes**
- **Wake-Up From Standby Mode in Less Than 6 μs**
- **16-Bit RISC Architecture, Extended Memory, 125-ns Instruction Cycle Time**
- **Three Channel Internal DMA**
- **12-Bit A/D Converter With Internal Reference, Sample-and-Hold, and Autoscan Feature**
- **Three Configurable Operational Amplifiers**
- **Dual 12-Bit Digital-to-Analog (D/A) Converters With Synchronization**
- **16-Bit Timer_A With Three Capture/Compare Registers**
- **16-Bit Timer_B With Seven Capture/Compare-With-Shadow Registers**
- **On-Chip Comparator**
- **Supply Voltage Supervisor/Monitor With Programmable Level Detection**
- **Serial Communication Interface (USART1), Select Asynchronous UART or Synchronous SPI by Software**
- **Universal Serial Communication Interface**
  - **Enhanced UART Supporting Auto-Baudrate Detection**
  - **IrDA Encoder and Decoder**
  - **Synchronous SPI**
  - **I2C™**
- **Serial Onboard Programming, Programmable Code Protection by Security Fuse**
- **Brownout Detector**
- **Basic Timer With Real Time Clock Feature**
- **Integrated LCD Driver up to 160 Segments With Regulated Charge Pump**
- **Family Members Include:**
  - **MSP430xG4616:**
    92KB+256B Flash or ROM Memory
    4KB RAM
  - **MSP430xG4617:**
    92KB+256B Flash or ROM Memory,
    8KB RAM
  - **MSP430xG4618:**
    116KB+256B Flash or ROM Memory,
    8KB RAM
  - **MSP430xG4619:**
    120KB+256B Flash or ROM Memory,
    4KB RAM
- **For Complete Module Descriptions, See the *MSP430x4xx Family User's Guide* (literature number SLAU056)**

description

The Texas Instruments MSP430 family of ultralow-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 6 μs.

The MSP430xG461x series are microcontroller configurations with two 16-bit timers, a high-performance 12-bit A/D converter, dual 12-bit D/A converters, three configurable operational amplifiers, one universal serial communication interface (USCI), one universal synchronous/asynchronous communication interface (USART), DMA, 80 I/O pins, and a liquid crystal display (LCD) driver with regulated charge pump.

Typical applications for this device include portable medical applications and e-meter applications.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications. These devices have limited built-in ESD protection.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

AVAILABLE OPTIONS[†]

T_A	PACKAGED DEVICES[‡]	
	PLASTIC 100-PIN TQFP (PZ)	PLASTIC 113-BALL BGA (ZQW)
−40°C to 85°C	MSP430FG4616IPZ	MSP430FG4616IZQW
	MSP430FG4617IPZ	MSP430FG4617IZQW
	MSP430FG4618IPZ	MSP430FG4618IZQW
	MSP430FG4619IPZ	MSP430FG4619IZQW
	MSP430CG4616IPZ	MSP430CG4616IZQW
	MSP430CG4617IPZ	MSP430CG4617IZQW
	MSP430CG4618IPZ	MSP430CG4618IZQW
	MSP430CG4619IPZ	MSP430CG4619IZQW

[†] For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

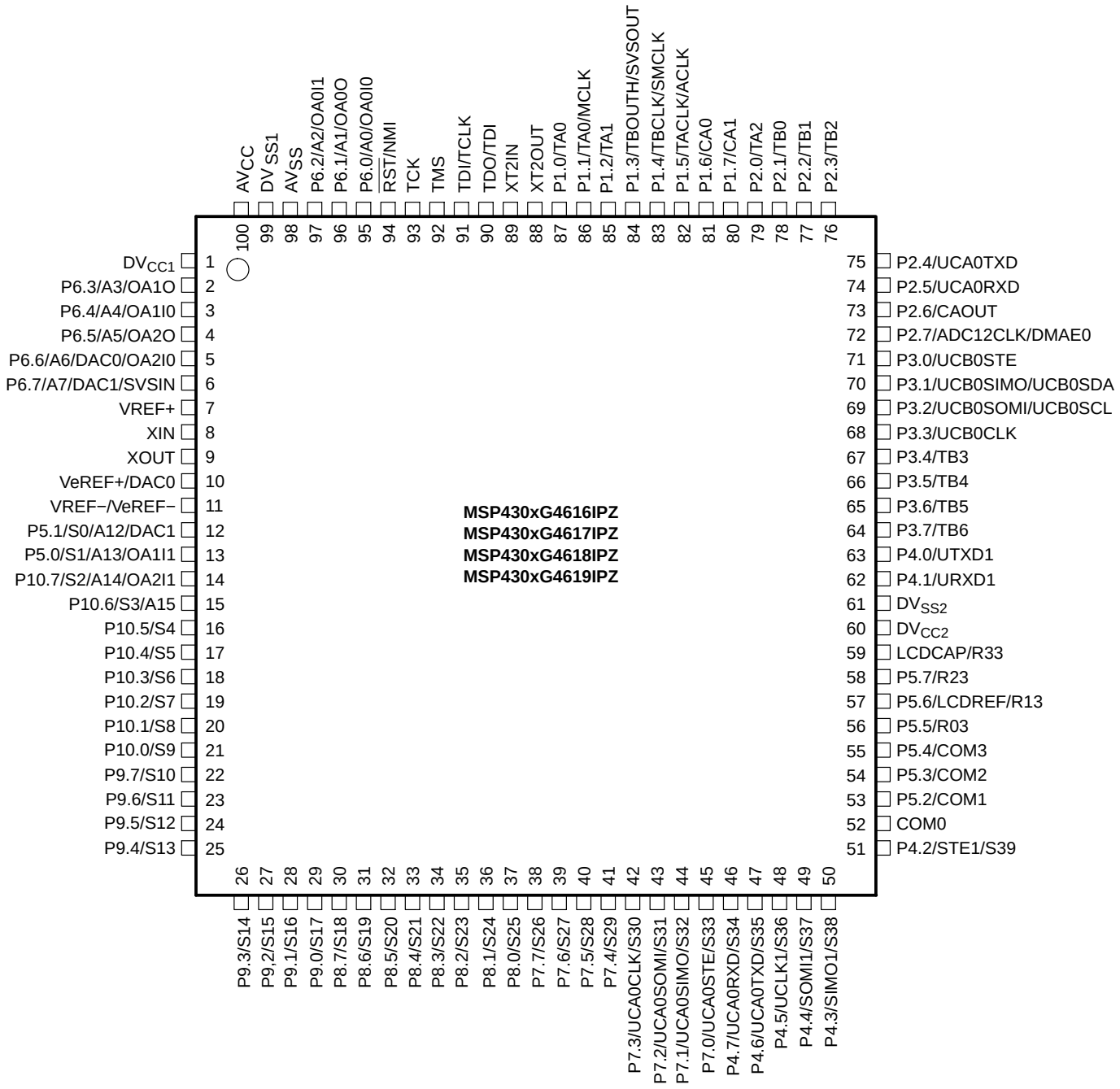
[‡] Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

DEVELOPMENT TOOL SUPPORT

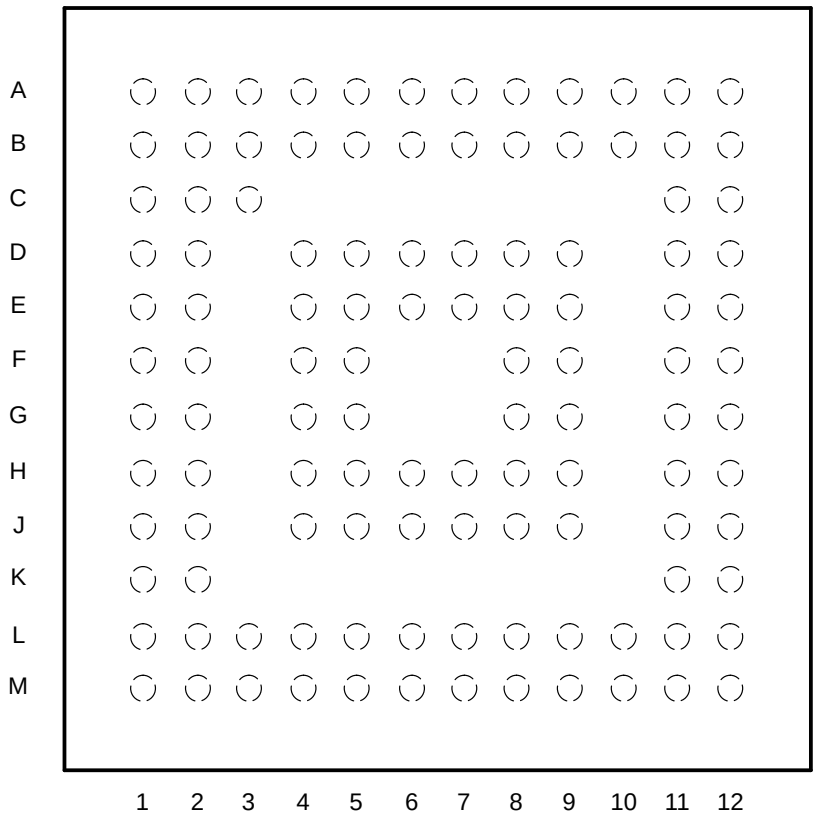
All MSP430 microcontrollers include an Embedded Emulation Module (EEM) allowing advanced debugging and programming through easy-to-use development tools. Recommended hardware options include:

- Debugging and Programming Interface
  - MSP-FET430UIF (USB)
  - MSP-FET430PIF (Parallel Port)
- Debugging and Programming Interface with Target Board
  - MSP-FET430U100 (for PZ package)
- Standalone Target Board
  - MSP-TS430PZ100 (for PZ package)
- Production Programmer
  - MSP-GANG430

pin designation, MSP430xG461xIPZ

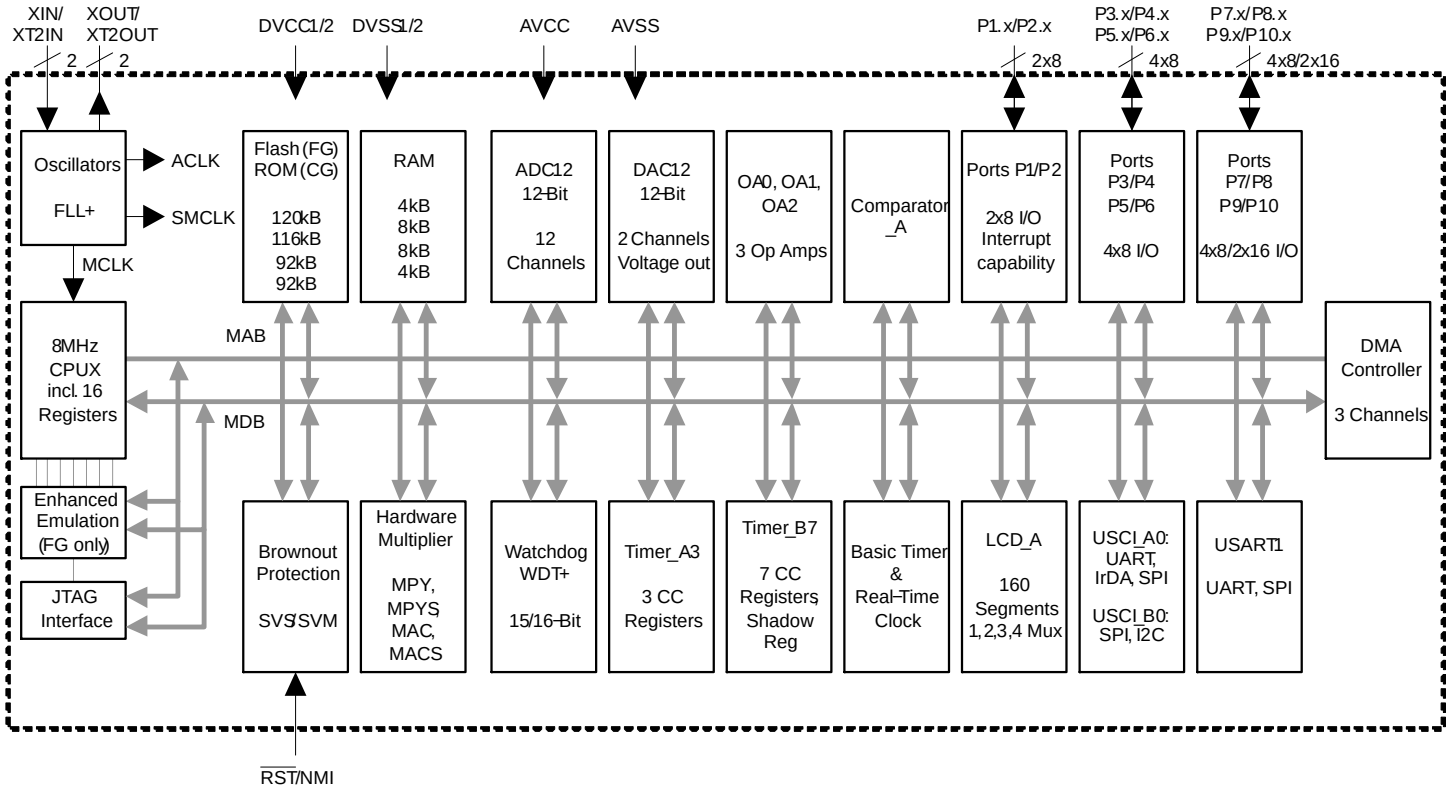


pin designation, MSP430xG461xIZQW (top view)



NOTE: For terminal assignments, see the *MSP430xG461x Terminal Functions* table.

functional block diagram



Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO. PZ	NO. ZQW		
DV_{CC1}	1	A1		Digital supply voltage, positive terminal
P6.3/A3/OA1O	2	B1	I/O	General-purpose digital I/O / analog input a3—12-bit ADC / OA1 output
P6.4/A4/OA1I0	3	B2	I/O	General-purpose digital I/O / analog input a4—12-bit ADC / OA1 input multiplexer on +terminal and −terminal
P6.5/A5/OA2O	4	C2	I/O	General-purpose digital I/O / analog input a5—12-bit ADC / OA2 output
P6.6/A6/DAC0/OA2I0	5	C1	I/O	General-purpose digital I/O / analog input a6—12-bit ADC / DAC12.0 output / OA2 input multiplexer on +terminal and −terminal
P6.7/A7/DAC1/SVSIN	6	C3	I/O	General-purpose digital I/O / analog input a7—12-bit ADC / DAC12.1 output / analog input to brownout, supply voltage supervisor
V_{REF+}	7	D2	O	Output of positive terminal of the reference voltage in the ADC
XIN	8	D1	I	Input port for crystal oscillator XT1. Standard or watch crystals can be connected.
XOUT	9	E1	O	Output terminal of crystal oscillator XT1
Ve_{REF+}/DAC0	10	E2	I/O	Input for an external reference voltage to the ADC / DAC12.0 output
V_{REF-}/Ve_{REF-}	11	E4	I	Negative terminal for the ADC reference voltage for both sources, the internal reference voltage, or an external applied reference voltage
P5.1/S0/A12/DAC1 (see Note 1)	12	F1	I/O	General-purpose digital I/O / LCD segment output 0 / analog input a12 − 12−bit ADC / DAC12.1 output
P5.0/S1/A13/OA1I1 (see Note 1)	13	F2	I/O	General-purpose digital I/O / LCD segment output 1 / analog input a13 − 12−bit ADC/OA1 input multiplexer on +terminal and −terminal
P10.7/S2/A14/OA2I1 (see Note 1)	14	E5	I/O	General-purpose digital I/O / LCD segment output 2 / analog input a14 − 12−bit ADC/OA2 input multiplexer on +terminal and −terminal
P10.6/S3/A15 (see Note 1)	15	G1	I/O	General-purpose digital I/O / LCD segment output 3 / analog input a15 − 12−bit ADC
P10.5/S4	16	G2	I/O	General-purpose digital I/O / LCD segment output 4
P10.4/S5	17	F4	I/O	General-purpose digital I/O / LCD segment output 5
P10.3/S6	18	H1	I/O	General-purpose digital I/O / LCD segment output 6
P10.2/S7	19	H2	I/O	General-purpose digital I/O / LCD segment output 7
P10.1/S8	20	F5	I/O	General-purpose digital I/O / LCD segment output 8
P10.0/S9	21	J1	I/O	General-purpose digital I/O / LCD segment output 9
P9.7/S10	22	J2	I/O	General-purpose digital I/O / LCD segment output 10
P9.6/S11	23	G4	I/O	General-purpose digital I/O / LCD segment output 11
P9.5/S12	24	K1	I/O	General-purpose digital I/O / LCD segment output 12
P9.4/S13	25	L1	I/O	General-purpose digital I/O / LCD segment output 13
P9.3/S14	26	M2	I/O	General-purpose digital I/O / LCD segment output 14
P9.2/S15	27	K2	I/O	General-purpose digital I/O / LCD segment output 15
P9.1/S16	28	L3	I/O	General-purpose digital I/O / LCD segment output 16
P9.0/S17	29	M3	I/O	General-purpose digital I/O / LCD segment output 17
P8.7/S18	30	H4	I/O	General-purpose digital I/O / LCD segment output 18
P8.6/S19	31	L4	I/O	General-purpose digital I/O / LCD segment output 19
P8.5/S20	32	M4	I/O	General-purpose digital I/O / LCD segment output 20
P8.4/S21	33	G5	I/O	General-purpose digital I/O / LCD segment output 21
P8.3/S22	34	L5	I/O	General-purpose digital I/O / LCD segment output 22

NOTES: 1. Segments S0 through S3 are disabled when the LCD charge pump feature is enabled (LCDCPEN = 1) and cannot be used together with the LCD charge pump. In addition, when using segments S0 through S3 with an external LCD voltage supply, $V_{LCD} \le AV_{CC}$.

Terminal Functions (Continued)

TERMINAL			I/O	DESCRIPTION
NAME	NO. PZ	NO. ZQW		
P8.2/S23	35	M5	I/O	General-purpose digital I/O / LCD segment output 23
P8.1/S24	36	H5	I/O	General-purpose digital I/O / LCD segment output 24
P8.0/S25	37	J5	I/O	General-purpose digital I/O / LCD segment output 25
P7.7/S26	38	M6	I/O	General-purpose digital I/O / LCD segment output 26
P7.6/S27	39	L6	I/O	General-purpose digital I/O / LCD segment output 27
P7.5/S28	40	J6	I/O	General-purpose digital I/O / LCD segment output 28
P7.4/S29	41	M7	I/O	General-purpose digital I/O / LCD segment output 29
P7.3/UCA0CLK/S30	42	H6	I/O	General-purpose digital I/O / external clock input − USCI_A0/UART or SPI mode, clock output − USCI_A0/SPI mode / LCD segment 30
P7.2/UCA0SOMI/S31	43	L7	I/O	General-purpose digital I/O / slave out/master in of USCI_A0/SPI mode / LCD segment output 31
P7.1/UCA0SIMO/S32	44	M8	I/O	General-purpose digital I/O / slave in/master out of USCI_A0/SPI mode / LCD segment output 32
P7.0/UCA0STE/S33	45	L8	I/O	General-purpose digital I/O / slave transmit enable—USCI_A0/SPI mode / LCD segment output 33
P4.7/UCA0RXD/S34	46	J7	I/O	General-purpose digital I/O / receive data in − USCI_A0/UART or IrDA mode / LCD segment output 34
P4.6/UCA0TXD/S35	47	M9	I/O	General-purpose digital I/O / transmit data out − USCI_A0/UART or IrDA mode / LCD segment output 35
P4.5/UCLK1/S36	48	L9	I/O	General-purpose digital I/O / external clock input − USART1/UART or SPI mode, clock output − USART1/SPI MODE / LCD segment output 36
P4.4/SOMI1/S37	49	H7	I/O	General-purpose digital I/O / slave out/master in of USART1/SPI mode / LCD segment output 37
P4.3/SIMO1/S38	50	M10	I/O	General-purpose digital I/O / slave in/master out of USART1/SPI mode / LCD segment output 38
P4.2/STE1/S39	51	M11	I/O	General-purpose digital I/O / slave transmit enable—USART1/SPI mode / LCD segment output 39
COM0	52	L10	O	COM0−3 are used for LCD backplanes.
P5.2/COM1	53	L12	I/O	General-purpose digital I/O / common output, COM0−3 are used for LCD backplanes.
P5.3/COM2	54	J8	I/O	General-purpose digital I/O / common output, COM0−3 are used for LCD backplanes.
P5.4/COM3	55	K12	I/O	General-purpose digital I/O / common output, COM0−3 are used for LCD backplanes.
P5.5/R03	56	K11	I/O	General-purpose digital I/O / Input port of lowest analog LCD level (V5)
P5.6/LCDREF/R13	57	J12	I/O	General-purpose digital I/O / External reference voltage input for regulated LCD voltage / Input port of third most positive analog LCD level (V4 or V3)
P5.7/R23	58	J11	I/O	General-purpose digital I/O / Input port of second most positive analog LCD level (V2)
LCDCAP/R33	59	H11	I	LCD capacitor connection / Input/output port of most positive analog LCD level (V1)
DV_{CC2}	60	H12		Digital supply voltage, positive terminal
DV_{SS2}	61	G12		Digital supply voltage, negative terminal
P4.1/URXD1	62	G11	I/O	General-purpose digital I/O / receive data in—USART1/UART mode
P4.0/UTXD1	63	H9	I/O	General-purpose digital I/O / transmit data out—USART1/UART mode
P3.7/TB6	64	F12	I/O	General-purpose digital I/O / Timer_B7 CCR6. Capture: CCI6A/CCI6B input, compare: Out6 output
P3.6/TB5	65	F11	I/O	General-purpose digital I/O / Timer_B7 CCR5. Capture: CCI5A/CCI5B input, compare: Out5 output
P3.5/TB4	66	G9	I/O	General-purpose digital I/O / Timer_B7 CCR4. Capture: CCI4A/CCI4B input, compare: Out4 output

Terminal Functions (Continued)

TERMINAL			I/O	DESCRIPTION
NAME	NO. PZ	NO. ZQW		
P3.4/TB3	67	E12	I/O	General-purpose digital I/O / Timer_B7 CCR3. Capture: CCI3A/CCI3B input, compare: Out3 output
P3.3/UCB0CLK	68	E11	I/O	General-purpose digital I/O / external clock input—USCI_B0/UART or SPI mode, clock output—USCI_B0/SPI mode
P3.2/UCB0SOMI/ UCB0SCL	69	F9	I/O	General-purpose digital I/O / slave out/master in of USCI_B0/SPI mode /I2C clock—USCI_B0/I2C mode
P3.1/UCB0SIMO/ UCB0SDA	70	D12	I/O	General-purpose digital I/O / slave in/master out of USCI_B0/SPI mode, I2C data—USCI_B0/I2C mode
P3.0/UCB0STE	71	D11	I/O	General-purpose digital I/O / slave transmit enable—USCI_B0/SPI mode
P2.7/ADC12CLK/ DMAE0	72	E9	I/O	General-purpose digital I/O / conversion clock—12-bit ADC / DMA Channel 0 external trigger
P2.6/CAOUT	73	C12	I/O	General-purpose digital I/O / Comparator_A output
P2.5/UCA0RXD	74	C11	I/O	General-purpose digital I/O / receive data in—USCI_A0/UART or IrDA mode
P2.4/UCA0TXD	75	B12	I/O	General-purpose digital I/O / transmit data out—USCI_A0/UART or IrDA mode
P2.3/TB2	76	A11	I/O	General-purpose digital I/O / Timer_B7 CCR2. Capture: CCI2A/CCI2B input, compare: Out2 output
P2.2/TB1	77	E8	I/O	General-purpose digital I/O / Timer_B7 CCR1. Capture: CCI1A/CCI1B input, compare: Out1 output
P2.1/TB0	78	D8	I/O	General-purpose digital I/O / Timer_B7 CCR0. Capture: CCI0A/CCI0B input, compare: Out0 output
P2.0/TA2	79	A10	I/O	General-purpose digital I/O / Timer_A Capture: CCI2A input, compare: Out2 output
P1.7/CA1	80	B10	I/O	General-purpose digital I/O / Comparator_A input
P1.6/CA0	81	A9	I/O	General-purpose digital I/O / Comparator_A input
P1.5/TACLK/ACLK	82	B9	I/O	General-purpose digital I/O / Timer_A, clock signal TACLK input / ACLK output (divided by 1, 2, 4, or 8)
P1.4/TBCLK/SMCLK	83	B8	I/O	General-purpose digital I/O / input clock TBCLK—Timer_B7 / submain system clock SMCLK output
P1.3/TBOUTH/SVSOUT	84	A8	I/O	General-purpose digital I/O / switch all PWM digital output ports to high impedance—Timer_B7 TB0 to TB6 / SVS: output of SVS comparator
P1.2/TA1	85	D7	I/O	General-purpose digital I/O / Timer_A, Capture: CCI1A input, compare: Out1 output
P1.1/TA0/MCLK	86	E7	I/O	General-purpose digital I/O / Timer_A. Capture: CCI0B input / MCLK output. Note: TA0 is only an input on this pin / BSL receive
P1.0/TA0	87	A7	I/O	General-purpose digital I/O / Timer_A. Capture: CCI0A input, compare: Out0 output / BSL transmit
XT2OUT	88	B7	O	Output terminal of crystal oscillator XT2
XT2IN	89	B6	I	Input port for crystal oscillator XT2. Only standard crystals can be connected.
TDO/TDI	90	A6	I/O	Test data output port. TDO/TDI data output or programming data input terminal
TDI/TCLK	91	D6	I	Test data input or test clock input. The device protection fuse is connected to TDI/TCLK.
TMS	92	E6	I	Test mode select. TMS is used as an input port for device programming and test.
TCK	93	A5	I	Test clock. TCK is the clock input port for device programming and test.
$\overline{\text{RST}}$/NMI	94	B5	I	Reset input or nonmaskable interrupt input port
P6.0/A0/OA0I0	95	A4	I/O	General-purpose digital I/O / analog input a0—12-bit ADC / OA0 input multiplexer on + terminal and − terminal
P6.1/A1/OA0O	96	D5	I/O	General-purpose digital I/O / analog input a1—12-bit ADC / OA0 output
P6.2/A2/OA0I1	97	B4	I/O	General-purpose digital I/O / analog input a2—12-bit ADC / OA0 input multiplexer on + terminal and − terminal

Terminal Functions (Continued)

TERMINAL			I/O	DESCRIPTION
NAME	NO. PZ	NO. ZQW		
AV_{SS}	98	A3		Analog supply voltage, negative terminal. Supplies SVS, brownout, oscillator, comparator_A, port 1
DV_{SS1} (see Note 1)	99	B3		Digital supply voltage, negative terminal
AV_{CC}	100	A2		Analog supply voltage, positive terminal. Supplies SVS, brownout, oscillator, comparator_A, port 1; must not power up prior to DV_{CC1}/DV_{CC2}.

NOTE 1: All unassigned ball locations on the ZQW package should be electrically tied to the ground supply. The shortest ground return path to the device should be established via ball location B3.

short-form description

CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

The MSP430xG461x device family utilizes the MSP430X CPU and is completely backwards compatible with the MSP430 CPU. For a complete description of the MSP430X CPU, see the *MSP430x4xx Family User's Guide* (SLAU056).

Program Counter	PC/R0
Stack Pointer	SP/R1
Status Register	SR/CG1/R2
Constant Generator	CG2/R3
General-Purpose Register	R4
General-Purpose Register	R5
General-Purpose Register	R6
General-Purpose Register	R7
General-Purpose Register	R8
General-Purpose Register	R9
General-Purpose Register	R10
General-Purpose Register	R11
General-Purpose Register	R12
General-Purpose Register	R13
General-Purpose Register	R14
General-Purpose Register	R15

instruction set

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats; Table 2 shows the address modes.

Table 1. Instruction Word Formats

Dual operands, source-destination	e.g., ADD R4,R5	R4 + R5 −−−> R5
Single operands, destination only	e.g., CALL R8	PC −−>(TOS), R8−−> PC
Relative jump, un/conditional	e.g., JNE	Jump-on-equal bit = 0

Table 2. Address Mode Descriptions

ADDRESS MODE	S	D	SYNTAX	EXAMPLE	OPERATION
Register	●	●	MOV Rs,Rd	MOV R10,R11	R10 —> R11
Indexed	●	●	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5)—> M(6+R6)
Symbolic (PC relative)	●	●	MOV EDE,TONI		M(EDE) —> M(TONI)
Absolute	●	●	MOV & MEM, & TCDAT		M(MEM) —> M(TCDAT)
Indirect	●		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) —> M(Tab+R6)
Indirect autoincrement	●		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) —> R11 R10 + 2—> R10
Immediate	●		MOV #X,TONI	MOV #45,TONI	#45 —> M(TONI)

NOTE: S = source D = destination

operating modes

The MSP430 has one active mode and five software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active. MCLK is disabled
  - FLL+ loop control remains active
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - FLL+ loop control is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK, FLL+ loop control and DCOCLK are disabled
  - DCO’s dc-generator remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK, FLL+ loop control, and DCOCLK are disabled
  - DCO’s dc-generator is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK, FLL+ loop control, and DCOCLK are disabled
  - DCO’s dc-generator is disabled
  - Crystal oscillator is stopped

interrupt vector addresses

The interrupt vectors and the power-up start address are located in the address range 0FFFFh to 0FFC0h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

Table 3. Interrupt Sources, Flags, and Vectors of MSP430xG461x Configurations

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-Up External Reset Watchdog Flash Memory	WDTIFG KEYV (see Note 1 and 5)	Reset	0FFFEh	31, highest
NMI Oscillator Fault Flash Memory Access Violation	NMIIFG (see Notes 1 and 3) OFIFG (see Notes 1 and 3) ACCVIFG (see Notes 1, 2, and 5)	(Non)maskable (Non)maskable (Non)maskable	0FFFCh	30
Timer_B7	TBCCR0 CCIFG0 (see Note 2)	Maskable	0FFFAh	29
Timer_B7	TBCCR1 CCIFG1 ... TBCCR6 CCIFG6, TBIFG (see Notes 1 and 2)	Maskable	0FFF8h	28
Comparator_A	CAIFG	Maskable	0FFF6h	27
Watchdog Timer+	WDTIFG	Maskable	0FFF4h	26
USCI_A0/USCI_B0 Receive	UCA0RXIFG, UCB0RXIFG (see Note 1)	Maskable	0FFF2h	25
USCI_A0/USCI_B0 Transmit	UCA0TXIFG, UCB0TXIFG (see Note 1)	Maskable	0FFF0h	24
ADC12	ADC12IFG (see Notes 1 and 2)	Maskable	0FFEEh	23
Timer_A3	TACCR0 CCIFG0 (see Note 2)	Maskable	0FFECh	22
Timer_A3	TACCR1 CCIFG1 and TACCR2 CCIFG2, TAIFG (see Notes 1 and 2)	Maskable	0FFEAh	21
I/O Port P1 (Eight Flags)	P1IFG.0 to P1IFG.7 (see Notes 1 and 2)	Maskable	0FFE8h	20
USART1 Receive	URXIFG1	Maskable	0FFE6h	19
USART1 Transmit	UTXIFG1	Maskable	0FFE4h	18
I/O Port P2 (Eight Flags)	P2IFG.0 to P2IFG.7 (see Notes 1 and 2)	Maskable	0FFE2h	17
Basic Timer1/RTC	BTIFG	Maskable	0FFE0h	16
DMA	DMA0IFG, DMA1IFG, DMA2IFG (see Notes 1 and 2)	Maskable	0FFDEh	15
DAC12	DAC12.0IFG, DAC12.1IFG (see Notes 1 and 2)	Maskable	0FFDCh	14
Reserved	Reserved (see Note 4)		0FFDAh	13
			...	...
			0FFC0h	0, lowest

NOTES: 1. Multiple source flags
2. Interrupt flags are located in the module.
3. A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh). (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.
4. The interrupt vectors at addresses 0FFDAh to 0FFC0h are not used in this device and can be used for regular program code if necessary.
5. Access and key violations, KEYV and ACCVIFG, only applicable to F devices.

special function registers (SFRs)

The MSP430 SFRs are located in the lowest address space and are organized as byte mode registers. SFRs should be accessed with byte instructions.

interrupt enable 1 and 2

Address	7	6	5	4	3	2	1	0
0h			ACCVIE	NMIIE			OFIE	WDTIE
			rw–0	rw–0			rw–0	rw–0

WDTIE	Watchdog-timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured as a general-purpose timer.
OFIE	Oscillator-fault-interrupt enable
NMIIE	Nonmaskable-interrupt enable
ACCVIE	Flash access violation interrupt enable

Address	7	6	5	4	3	2	1	0
01h	BTIE		UTXIE1	URXIE1	UCB0TXIE	UCB0RXIE	UCA0TXIE	UCA0RXIE
	rw–0		rw–0	rw–0	rw–0	rw–0	rw–0	rw–0

UCA0RXIE	USCI_A0 receive-interrupt enable
UCA0TXIE	USCI_A0 transmit-interrupt enable
UCB0RXIE	USCI_B0 receive-interrupt enable
UCB0TXIE	USCI_B0 transmit-interrupt enable
URXIE1	USART1 UART and SPI receive-interrupt enable
UTXIE1	USART1 UART and SPI transmit-interrupt enable
BTIE	Basic timer interrupt enable

interrupt flag register 1 and 2

Address	7	6	5	4	3	2	1	0
02h				NMIIFG			OFIFG	WDTIFG
				rw–0			rw–1	rw–(0)

WDTIFG: Set on watchdog timer overflow (in watchdog mode) or security key violation
Reset on V_{CC} power-on or a reset condition at the $\overline{RST}$/NMI pin in reset mode

OFIFG: Flag set on oscillator fault

NMIIFG: Set via $\overline{RST}$/NMI pin

Address	7	6	5	4	3	2	1	0
03h	BTIFG		UTXIFG1	URXIFG1	UCB0TXIFG	UCB0RXIFG	UCA0TXIFG	UCA0RXIFG
	rw–0		rw–1	rw–0	rw–0	rw–0	rw–0	rw–0

UCA0RXIFG USCI_A0 receive-interrupt flag

UCA0TXIFG USCI_A0 transmit-interrupt flag

UCB0RXIFG USCI_B0 receive-interrupt flag

UCB0TXIFG USCI_B0 transmit-interrupt flag

URXIFG0: USART1: UART and SPI receive flag

UTXIFG0: USART1: UART and SPI transmit flag

BTIFG: Basic timer flag

module enable registers 1 and 2

Address	7	6	5	4	3	2	1	0
04h								

Address	7	6	5	4	3	2	1	0
05h			UTXE1	URXE1 USPIE1				
			rw–0	rw–0				

URXE1: USART1: UART mode receive enable

UTXE1: USART1: UART mode transmit enable

USPIE1: USART1: SPI mode transmit and receive enable

Legend		
	rw:	Bit can be read and written.
	rw-0,1:	Bit can be read and written. It is Reset or Set by PUC.
	rw-(0,1):	Bit can be read and written. It is Reset or Set by POR.
		SFR bit is not present in device

memory organization

		MSP430FG4616	MSP430FG4617	MSP430FG4618	MSP430FG4619
Memory Main: interrupt vector Main: code memory	Size Flash Flash	92KB 0FFFFh − 0FFC0h 018FFFh − 002100h	92KB 0FFFFh − 0FFC0h 019FFFh − 003100h	116KB 0FFFFh − 0FFC0h 01FFFFh − 003100h	120KB 0FFFFh − 0FFC0h 01FFFFh − 002100h
RAM (Total) Extended Mirrored	Size Size Size	4KB 020FFh − 01100h 2KB 020FFh − 01900h 2KB 018FFh − 01100h	8KB 030FFh − 01100h 6KB 030FFh − 01900h 2KB 018FFh − 01100h	8KB 030FFh − 01100h 6KB 030FFh − 01900h 2KB 018FFh − 01100h	4KB 020FFh − 01100h 2KB 020FFh − 01900h 2KB 018FFh − 01100h
Information memory	Size Flash	256 Byte 010FFh − 01000h	256 Byte 010FFh − 01000h	256 Byte 010FFh − 01000h	256 Byte 010FFh − 01000h
Boot memory	Size ROM	1KB 0FFFh − 0C00h	1KB 0FFFh − 0C00h	1KB 0FFFh − 0C00h	1KB 0FFFh − 0C00h
RAM (mirrored at 018FFh − 01100h)	Size	2KB 09FFh − 0200h	2KB 09FFh − 0200h	2KB 09FFh − 0200h	2KB 09FFh − 0200h
Peripherals	16 bit 8 bit 8-bit SFR	01FFh − 0100h 0FFh − 010h 0Fh − 00h	01FFh − 0100h 0FFh − 010h 0Fh − 00h	01FFh − 0100h 0FFh − 010h 0Fh − 00h	01FFh − 0100h 0FFh − 010h 0Fh − 00h

		MSP430CG4616	MSP430CG4617	MSP430CG4618	MSP430CG4619
Memory Main: interrupt vector Main: code memory	Size ROM ROM	92KB 0FFFFh − 0FFC0h 018FFFh − 002100h	92KB 0FFFFh − 0FFC0h 019FFFh − 003100h	116KB 0FFFFh − 0FFC0h 01FFFFh − 003100h	120KB 0FFFFh − 0FFC0h 01FFFFh − 002100h
RAM (Total) Extended Mirrored	Size Size Size	4KB 020FFh − 01100h 2KB 020FFh − 01900h 2KB 018FFh − 01100h	8KB 030FFh − 01100h 6KB 030FFh − 01900h 2KB 018FFh − 01100h	8KB 030FFh − 01100h 6KB 030FFh − 01900h 2KB 018FFh − 01100h	4KB 020FFh − 01100h 2KB 020FFh − 01900h 2KB 018FFh − 01100h
Information memory	Size ROM	256 Byte 010FFh − 01000h	256 Byte 010FFh − 01000h	256 Byte 010FFh − 01000h	256 Byte 010FFh − 01000h
Boot memory (Optional on CG)	Size ROM	1KB 0FFFh − 0C00h	1KB 0FFFh − 0C00h	1KB 0FFFh − 0C00h	1KB 0FFFh − 0C00h
RAM (mirrored at 018FFh − 01100h)	Size	2KB 09FFh − 0200h	2KB 09FFh − 0200h	2KB 09FFh − 0200h	2KB 09FFh − 0200h
Peripherals	16 bit 8 bit 8-bit SFR	01FFh − 0100h 0FFh − 010h 0Fh − 00h	01FFh − 0100h 0FFh − 010h 0Fh − 00h	01FFh − 0100h 0FFh − 010h 0Fh − 00h	01FFh − 0100h 0FFh − 010h 0Fh − 00h

bootstrap loader (BSL)

The MSP430 BSL enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. A bootstrap loader security key is provided at address 0FFBEh to disable the BSL completely or to disable the erasure of the flash if an invalid password is supplied. The BSL is optional for ROM-based devices. For complete description of the features of the BSL and its implementation, see the application report *Features of the MSP430 Bootstrap Loader*, literature number SLAA089.

BSLKEY	DESCRIPTION
00000h	Erasure of flash disabled if an invalid password is supplied
0AA55h	BSL disabled
any other value	BSL enabled

BSL FUNCTION	PZ/ZQW PACKAGE PINS
Data Transmit	87/A7 − P1.0
Data Receive	86/E7 − P1.1

flash memory

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and two segments of information memory (A and B) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A and B can be erased individually, or as a group with segments 0 to n.
  Segments A and B are also called *information memory.*
- New devices may have some bytes programmed in the information memory (needed for test during manufacturing). The user should perform an erase of the information memory prior to the first use.

peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x4xx Family User's Guide* (SLAU056).

DMA controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC12 conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode without having to awaken to move data to or from a peripheral.

oscillator and system clock

The clock system in the MSP430xG461x family of devices is supported by the FLL+ module, which includes support for a 32768-Hz watch crystal oscillator, an internal digitally controlled oscillator (DCO), and a high-frequency crystal oscillator. The FLL+ clock module is designed to meet the requirements of both low system cost and low power consumption. The FLL+ features digital frequency locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the watch crystal frequency. The internal DCO provides a fast turn-on clock source and stabilizes in less than 6 μs. The FLL+ module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal or a high frequency crystal
- Main clock (MCLK), the system clock used by the CPU
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, or ACLK/8

brownout, supply voltage supervisor

The brownout circuit is implemented to provide the proper internal reset signal to the device during power-on and power-off. The supply voltage supervisor (SVS) circuitry detects if the supply voltage drops below a user selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (SVM, the device is not automatically reset).

The CPU begins code execution after the brownout circuit releases the device reset. However, V_{CC} may not have ramped to $V_{CC(min)}$ at that time. The user must insure the default FLL+ settings are not changed until V_{CC} reaches $V_{CC(min)}$. If desired, the SVS circuit can be used to determine when V_{CC} reaches $V_{CC(min)}$.

digital I/O

There are ten 8-bit I/O ports implemented—ports P1 through P10:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all the eight bits of ports P1 and P2.
- Read/write access to port-control registers is supported by all instructions.
- Ports P7/P8 and P9/P10 can be accessed word-wise as ports PA and PB respectively.

Basic Timer1 and Real-Time Clock

The Basic Timer1 has two independent 8-bit timers that can be cascaded to form a 16-bit timer/counter. Both timers can be read and written by software. Basic Timer1 is extended to provide an integrated real-time clock (RTC). An internal calendar compensates for months with less than 31 days and includes leap-year correction.

LCD_A drive with regulated charge pump

The LCD_A driver generates the segment and common signals required to drive an LCD display. The LCD_A controller has dedicated data memory to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2-MUX, 3-MUX, and 4-MUX LCDs are supported by this peripheral. The module can provide a LCD voltage independent of the supply voltage with its integrated charge pump. Furthermore it is possible to control the level of the LCD voltage and, thus, contrast by software.

watchdog timer (WDT+)

The primary function of the WDT+ module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

universal serial communication interface (USCI)

The USCI modules are used for serial data communication. The USCI module supports synchronous communication protocols like SPI (3 or 4 pin), I2C and asynchronous communication protocols like UART, enhanced UART with automatic baudrate detection, and IrDA.

The USCI_A0 module provides support for SPI (3 or 4 pin), UART, enhanced UART and IrDA.

The USCI_B0 module provides support for SPI (3 or 4 pin) and I2C.

USART1

The hardware universal synchronous/asynchronous receive transmit (USART) peripheral module is used for serial data communication. The USART supports synchronous SPI (3 or 4 pin) and asynchronous UART communication protocols, using double-buffered transmit and receive channels.

hardware multiplier

The multiplication operation is supported by a dedicated peripheral module. The module performs 16×16, 16×8, 8×16, and 8×8 bit operations. The module is capable of supporting signed and unsigned multiplication, as well as signed and unsigned multiply and accumulate operations. The result of an operation can be accessed immediately after the operands have been loaded into the peripheral registers. No additional clock cycles are required.

Timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Timer_A3 Signal Connections					
Input Pin Number PZ/ZQW	Device Input Signal	Module Input Name	Module Block	Module Output Signal	Output Pin Number PZ/ZQW
82/B9 - P1.5	TACLK	TACLK	Timer	NA	
	ACLK	ACLK			
	SMCLK	SMCLK			
82/B9 - P1.5	$\overline{\text{TACLK}}$	INCLK			
87/A7 - P1.0	TA0	CCI0A	CCR0	TA0	87/A7 - P1.0
86/E7 - P1.1	TA0	CCI0B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
85/D7 - P1.2	TA1	CCI1A	CCR1	TA1	85/D7 - P1.2
	CAOUT (internal)	CCI1B			ADC12 (internal)
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
79/A10 - P2.0	TA2	CCI2A	CCR2	TA2	79/A10 - P2.0
	ACLK (internal)	CCI2B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			

Timer_B7

Timer_B7 is a 16-bit timer/counter with seven capture/compare registers. Timer_B7 can support multiple capture/compares, PWM outputs, and interval timing. Timer_B7 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Timer_B7 Signal Connections					
Input Pin Number PZ/ZQW	Device Input Signal	Module Input Name	Module Block	Module Output Signal	Output Pin Number PZ/ZQW
83/B8 - P1.4	TBCLK	TBCLK	Timer	NA	
	ACLK	ACLK			
	SMCLK	SMCLK			
83/B8 - P1.4	$\overline{\text{TBCLK}}$	INCLK			
78/D8 - P2.1	TB0	CCI0A	CCR0	TB0	78/D8 - P2.1
78/D8 - P2.1	TB0	CCI0B			ADC12 (internal)
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
77/E8 - P2.2	TB1	CCI1A	CCR1	TB1	77/E8 - P2.2
77/E8 - P2.2	TB1	CCI1B			ADC12 (internal)
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
76/A11 - P2.3	TB2	CCI2A	CCR2	TB2	76/A11 - P2.3
76/A11 - P2.3	TB2	CCI2B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
67/E12 - P3.4	TB3	CCI3A	CCR3	TB3	67/E12 - P3.4
67/E12 - P3.4	TB3	CCI3B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
66/G9 - P3.5	TB4	CCI4A	CCR4	TB4	66/G9 - P3.5
66/G9 - P3.5	TB4	CCI4B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
65/F11 - P3.6	TB5	CCI5A	CCR5	TB5	65/F11 - P3.6
65/F11 - P3.6	TB5	CCI5B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
64/F12 - P3.7	TB6	CCI6A	CCR6	TB6	64/F12 - P3.7
	ACLK (internal)	CCI6B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			

Comparator_A

The primary function of the comparator_A module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

ADC12

The ADC12 module supports fast, 12-bit analog-to-digital conversions. The module implements a 12-bit SAR core, sample select control, reference generator and a 16 word conversion-and-control buffer. The conversion-and-control buffer allows up to 16 independent ADC samples to be converted and stored without any CPU intervention.

DAC12

The DAC12 module is a 12-bit, R-ladder, voltage output DAC. The DAC12 may be used in 8- or 12-bit mode, and may be used in conjunction with the DMA controller. When multiple DAC12 modules are present, they may be grouped together for synchronous operation.

OA

The MSP430xG461x has three configurable low-current general-purpose operational amplifiers. Each OA input and output terminal is software-selectable and offer a flexible choice of connections for various applications. The OA op amps primarily support front-end analog signal conditioning prior to analog-to-digital conversion.

OA Signal Connections

Input Pin Number	Device Input Signal	Module Input Name	Module Block	Module Output Signal	Device Output Signal	Output Pin Number
PZ						PZ
95 - P6.0	OA0I0	OA0I0	OA0	OA0OUT	OA0O	96 - P6.1
97 - P6.2	OA0I1	OA0I1			OA0O	ADC12 (internal)
	DAC12_0OUT (internal)	DAC12_0OUT				
	DAC12_1OUT (internal)	DAC12_1OUT				
3 - P6.4	OA1I0	OA1I0	OA1	OA1OUT	OA1O	2 - P6.3
13 - P5.0	OA1I1	OA1I1			OA1O	13- P5.0
	DAC12_0OUT (internal)	DAC12_0OUT			OA1O	ADC12 (internal)
	DAC12_1OUT (internal)	DAC12_1OUT				
5 - P6.6	OA2I0	OA2I0	OA2	OA2OUT	OA2O	4 - P6.5
14 - P10.7	OA2I1	OA2I1			OA2O	14 - P10.7
	DAC12_0OUT (internal)	DAC12_0OUT			OA2O	ADC12 (internal)
	DAC12_1OUT (internal)	DAC12_1OUT				

peripheral file map

PERIPHERALS WITH WORD ACCESS			
Watchdog+	Watchdog timer control	WDTCTL	0120h
Timer_B7	Capture/compare register 6	TBCCR6	019Eh
	Capture/compare register 5	TBCCR5	019Ch
	Capture/compare register 4	TBCCR4	019Ah
	Capture/compare register 3	TBCCR3	0198h
	Capture/compare register 2	TBCCR2	0196h
	Capture/compare register 1	TBCCR1	0194h
	Capture/compare register 0	TBCCR0	0192h
	Timer_B register	TBR	0190h
	Capture/compare control 6	TBCCTL6	018Eh
	Capture/compare control 5	TBCCTL5	018Ch
	Capture/compare control 4	TBCCTL4	018Ah
	Capture/compare control 3	TBCCTL3	0188h
	Capture/compare control 2	TBCCTL2	0186h
	Capture/compare control 1	TBCCTL1	0184h
	Capture/compare control 0	TBCCTL0	0182h
	Timer_B control	TBCTL	0180h
	Timer_B interrupt vector	TBIV	011Eh
Timer_A3	Capture/compare register 2	TACCR2	0176h
	Capture/compare register 1	TACCR1	0174h
	Capture/compare register 0	TACCR0	0172h
	Timer_A register	TAR	0170h
	Capture/compare control 2	TACCTL2	0166h
	Capture/compare control 1	TACCTL1	0164h
	Capture/compare control 0	TACCTL0	0162h
	Timer_A control	TACTL	0160h
	Timer_A interrupt vector	TAIV	012Eh
Hardware Multiplier	Sum extend	SUMEXT	013Eh
	Result high word	RESHI	013Ch
	Result low word	RESLO	013Ah
	Second operand	OP2	0138h
	Multiply signed + accumulate/operand1	MACS	0136h
	Multiply + accumulate/operand1	MAC	0134h
	Multiply signed/operand1	MPYS	0132h
	Multiply unsigned/operand1	MPY	0130h
Flash (FG devices only)	Flash control 3	FCTL3	012Ch
	Flash control 2	FCTL2	012Ah
	Flash control 1	FCTL1	0128h

peripheral file map (continued)

PERIPHERALS WITH WORD ACCESS (CONTINUED)			
DMA	DMA module control 0	DMACTL0	0122h
	DMA module control 1	DMACTL1	0124h
	DMA interrupt vector	DMAIV	0126h
DMA Channel 0	DMA channel 0 control	DMA0CTL	01D0h
	DMA channel 0 source address	DMA0SA	01D2h
	DMA channel 0 destination address	DMA0DA	01D6h
	DMA channel 0 transfer size	DMA0SZ	01DAh
DMA Channel 1	DMA channel 1 control	DMA1CTL	01DCh
	DMA channel 1 source address	DMA1SA	01DEh
	DMA channel 1 destination address	DMA1DA	01E2h
	DMA channel 1 transfer size	DMA1SZ	01E6h
DMA Channel 2	DMA channel 2 control	DMA2CTL	01E8h
	DMA channel 2 source address	DMA2SA	01EAh
	DMA channel 2 destination address	DMA2DA	01EEh
	DMA channel 2 transfer size	DMA2SZ	01F2h

peripheral file map (continued)

PERIPHERALS WITH WORD ACCESS (CONTINUED)			
ADC12 See also *Peripherals With Byte Access*	Conversion memory 15	ADC12MEM15	015Eh
	Conversion memory 14	ADC12MEM14	015Ch
	Conversion memory 13	ADC12MEM13	015Ah
	Conversion memory 12	ADC12MEM12	0158h
	Conversion memory 11	ADC12MEM11	0156h
	Conversion memory 10	ADC12MEM10	0154h
	Conversion memory 9	ADC12MEM9	0152h
	Conversion memory 8	ADC12MEM8	0150h
	Conversion memory 7	ADC12MEM7	014Eh
	Conversion memory 6	ADC12MEM6	014Ch
	Conversion memory 5	ADC12MEM5	014Ah
	Conversion memory 4	ADC12MEM4	0148h
	Conversion memory 3	ADC12MEM3	0146h
	Conversion memory 2	ADC12MEM2	0144h
	Conversion memory 1	ADC12MEM1	0142h
	Conversion memory 0	ADC12MEM0	0140h
	Interrupt-vector-word register	ADC12IV	01A8h
	Inerrupt-enable register	ADC12IE	01A6h
	Inerrupt-flag register	ADC12IFG	01A4h
	Control register 1	ADC12CTL1	01A2h
	Control register 0	ADC12CTL0	01A0h
DAC12	DAC12_1 data	DAC12_1DAT	01CAh
	DAC12_1 control	DAC12_1CTL	01C2h
	DAC12_0 data	DAC12_0DAT	01C8h
	DAC12_0 control	DAC12_0CTL	01C0h
Port PA	Port PA selection	PASEL	03Eh
	Port PA direction	PADIR	03Ch
	Port PA output	PAOUT	03Ah
	Port PA input	PAIN	038h
Port PB	Port PB selection	PBSEL	00Eh
	Port PB direction	PBDIR	00Ch
	Port PB output	PBOUT	00Ah
	Port PB input	PBIN	008h

peripheral file map (continued)

PERIPHERALS WITH BYTE ACCESS			
OA2	Operational Amplifier 2 control register 1	OA2CTL1	0C5h
	Operational Amplifier 2 control register 0	OA2CTL0	0C4h
OA1	Operational Amplifier 1 control register 1	OA1CTL1	0C3h
	Operational Amplifier 1 control register 0	OA1CTL0	0C2h
OA0	Operational Amplifier 0 control register 1	OA0CTL1	0C1h
	Operational Amplifier 0 control register 0	OA0CTL0	0C0h
LCD_A	LCD Voltage Control 1	LCDAVCTL1	0AFh
	LCD Voltage Control 0	LCDAVCTL0	0AEh
	LCD Voltage Port Control 1	LCDAPCTL1	0ADh
	LCD Voltage Port Control 0	LCDAPCTL0	0ACh
	LCD memory 20	LCDM20	0A4h
	:	:	:
	LCD memory 16	LCDM16	0A0h
	LCD memory 15	LCDM15	09Fh
	:	:	:
	LCD memory 1	LCDM1	091h
	LCD control and mode	LCDCTL	090h
ADC12 (Memory control registers require byte access)	ADC memory-control register 15	ADC12MCTL15	08Fh
	ADC memory-control register 14	ADC12MCTL14	08Eh
	ADC memory-control register 13	ADC12MCTL13	08Dh
	ADC memory-control register 12	ADC12MCTL12	08Ch
	ADC memory-control register 11	ADC12MCTL11	08Bh
	ADC memory-control register 10	ADC12MCTL10	08Ah
	ADC memory-control register 9	ADC12MCTL9	089h
	ADC memory-control register 8	ADC12MCTL8	088h
	ADC memory-control register 7	ADC12MCTL7	087h
	ADC memory-control register 6	ADC12MCTL6	086h
	ADC memory-control register 5	ADC12MCTL5	085h
	ADC memory-control register 4	ADC12MCTL4	084h
	ADC memory-control register 3	ADC12MCTL3	083h
	ADC memory-control register 2	ADC12MCTL2	082h
	ADC memory-control register 1	ADC12MCTL1	081h
	ADC memory-control register 0	ADC12MCTL0	080h
USART1	Transmit buffer	U1TXBUF	07Fh
	Receive buffer	U1RXBUF	07Eh
	Baud rate	U1BR1	07Dh
	Baud rate	U1BR0	07Ch
	Modulation control	U1MCTL	07Bh
	Receive control	U1RCTL	07Ah
	Transmit control	U1TCTL	079h
	USART control	U1CTL	078h

peripheral file map (continued)

PERIPHERALS WITH BYTE ACCESS (CONTINUED)			
USCI	USCI I2C Slave Address	UCBI2CSA	011Ah
	USCI I2C Own Address	UCBI2COA	0118h
	USCI Synchronous Transmit Buffer	UCBTXBUF	06Fh
	USCI Synchronous Receive Buffer	UCBRXBUF	06Eh
	USCI Synchronous Status	UCBSTAT	06Dh
	USCI I2C Interrupt Enable	UCBI2CIE	06Ch
	USCI Synchronous Bit Rate 1	UCBBR1	06Bh
	USCI Synchronous Bit Rate 0	UCBBR0	06Ah
	USCI Synchronous Control 1	UCBCTL1	069h
	USCI Synchronous Control 0	UCBCTL0	068h
	USCI Transmit Buffer	UCATXBUF	067h
	USCI Receive Buffer	UCARXBUF	066h
	USCI Status	UCASTAT	065h
	USCI Modulation Control	UCAMCTL	064h
	USCI Baud Rate 1	UCABR1	063h
	USCI Baud Rate 0	UCABR0	062h
	USCI Control 1	UCACTL1	061h
	USCI Control 0	UCACTL0	060h
	USCI IrDA Receive Control	UCAIRRCTL	05Fh
	USCI IrDA Transmit Control	UCAIRTCTL	05Eh
	USCI LIN Control	UCAABCTL	05Dh
Comparator_A	Comparator_A port disable	CAPD	05Bh
	Comparator_A control 2	CACTL2	05Ah
	Comparator_A control 1	CACTL1	059h
BrownOUT, SVS	SVS control register (Reset by brownout signal)	SVSCTL	056h
FLL+Clock	FLL+ Control 1	FLL_CTL1	054h
	FLL+ Control 0	FLL_CTL0	053h
	System clock frequency control	SCFQCTL	052h
	System clock frequency integrator	SCFI1	051h
	System clock frequency integrator	SCFI0	050h
RTC (Basic Timer 1)	Real Time Clock Year High Byte	RTCYEARH	04Fh
	Real Time Clock Year Low Byte	RTCYEARL	04Eh
	Real Time Clock Month	RTCMON	04Dh
	Real Time Clock Day of Month	RTCDAY	04Ch
	Basic Timer1 Counter 2	BTCNT2	047h
	Basic Timer1 Counter 1	BTCNT1	046h
	Real Time Counter 4	RTCNT4	045h
	(Real Time Clock Day of Week)	(RTCDOW)	
	Real Time Counter 3	RTCNT3	044h
	(Real Time Clock Hour)	(RTCHOUR)	
	Real Time Counter 2	RTCNT2	043h
	(Real Time Clock Minute)	(RTCMIN)	
	Real Time Counter 1	RTCNT1	042h
	(Real Time Clock Second)	(RTCSEC)	
	Real Time Clock Control	RTCCTL	041h
	Basic Timer1 Control	BTCTL	040h

peripheral file map (continued)

PERIPHERALS WITH BYTE ACCESS (CONTINUED)			
Port P10	Port P10 selection	P10SEL	00Fh
	Port P10 direction	P10DIR	00Dh
	Port P10 output	P10OUT	00Bh
	Port P10 input	P10IN	009h
Port P9	Port P9 selection	P9SEL	00Eh
	Port P9 direction	P9DIR	00Ch
	Port P9 output	P9OUT	00Ah
	Port P9 input	P9IN	008h
Port P8	Port P8 selection	P8SEL	03Fh
	Port P8 direction	P8DIR	03Dh
	Port P8 output	P8OUT	03Bh
	Port P8 input	P8IN	039h
Port P7	Port P7 selection	P7SEL	03Eh
	Port P7 direction	P7DIR	03Ch
	Port P7 output	P7OUT	03Ah
	Port P7 input	P7IN	038h
Port P6	Port P6 selection	P6SEL	037h
	Port P6 direction	P6DIR	036h
	Port P6 output	P6OUT	035h
	Port P6 input	P6IN	034h
Port P5	Port P5 selection	P5SEL	033h
	Port P5 direction	P5DIR	032h
	Port P5 output	P5OUT	031h
	Port P5 input	P5IN	030h
Port P4	Port P4 selection	P4SEL	01Fh
	Port P4 direction	P4DIR	01Eh
	Port P4 output	P4OUT	01Dh
	Port P4 input	P4IN	01Ch
Port P3	Port P3 selection	P3SEL	01Bh
	Port P3 direction	P3DIR	01Ah
	Port P3 output	P3OUT	019h
	Port P3 input	P3IN	018h
Port P2	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt-edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h
Port P1	Port P1 selection	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt-edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h

peripheral file map (continued)

PERIPHERALS WITH BYTE ACCESS (CONTINUED)			
Special functions	SFR module enable 2	ME2	005h
	SFR module enable 1	ME1	004h
	SFR interrupt flag 2	IFG2	003h
	SFR interrupt flag 1	IFG1	002h
	SFR interrupt enable 2	IE2	001h
	SFR interrupt enable 1	IE1	000h

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Voltage range applied at V_{CC} to V_{SS} . . . . . −0.3 V to 4.1 V
Voltage range applied to any pin (see Note) . . . . . −0.3 V to V_{CC} + 0.3 V
Diode current at any device terminal . . . . . ±2 mA
Storage temperature range, T_{stg}: Unprogrammed device . . . . . −55°C to 150°C
Programmed device . . . . . −40°C to 85°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: All voltages referenced to V_{SS}. The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TDI/TCLK pin when blowing the JTAG fuse.

recommended operating conditions

			MIN	NOM	MAX	UNITS
Supply voltage during program execution (see Note 1), V_{CC} (AV_{CC} = $DV_{CC1/2}$ = V_{CC})		MSP430xG461x	1.8		3.6	V
Supply voltage during flash memory programming (see Note 1), V_{CC} (AV_{CC} = $DV_{CC1/2}$ = V_{CC})		MSP430FG461x	2.7		3.6	V
Supply voltage during program execution, SVS enabled and PORON = 1 (see Note 1 and Note 2), V_{CC} (AV_{CC} = $DV_{CC1/2}$ = V_{CC})		MSP430xG461x	2		3.6	V
Supply voltage (see Note 1), V_{SS} (AV_{SS} = $DV_{SS1/2}$ = V_{SS})			0		0	V
Operating free-air temperature range, T_A		MSP430xG461x	−40		85	°C
LFXT1 crystal frequency, $f_{(LFXT1)}$ (see Note 2)	LF selected, XTS_FLL = 0	Watch crystal		32.768		kHz
	XT1 selected, XTS_FLL = 1	Ceramic resonator	450		8000	
	XT1 selected, XTS_FLL = 1	Crystal	1000		8000	
XT2 crystal frequency, $f_{(XT2)}$		Ceramic resonator	450		8000	kHz
		Crystal	1000		8000	
Processor frequency (signal MCLK), $f_{(System)}$		V_{CC} = 1.8 V	DC		3.0	MHz
		V_{CC} = 2.0 V	DC		4.6	
		V_{CC} = 3.6 V	DC		8.0	

NOTES: 1. It is recommended to power AV_{CC} and DV_{CC} from the same source. A maximum difference of 0.3 V between AV_{CC} and DV_{CC} can be tolerated during power up and operation.
2. The minimum operating supply voltage is defined according to the trip point where POR is going active by decreasing the supply voltage. POR is going inactive when the supply voltage is raised above the minimum supply voltage plus the hysteresis of the SVS circuitry.
3. In LF mode, the LFXT1 oscillator requires a watch crystal. In XT1 mode, LFXT1 accepts a ceramic resonator or a crystal.

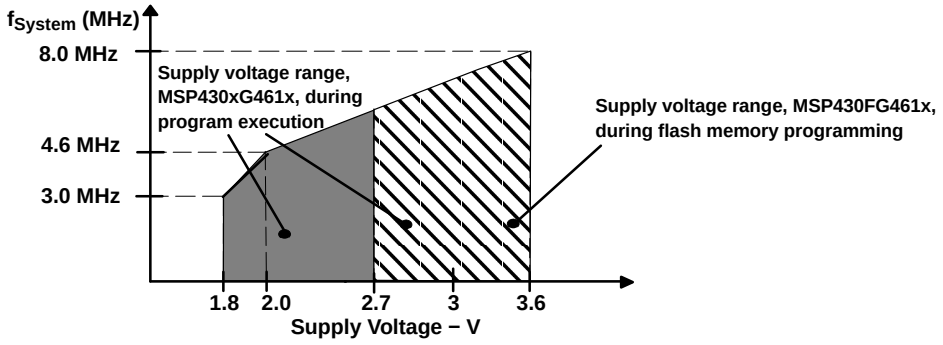


Figure 1. Frequency vs Supply Voltage, Typical Characteristic

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

supply current into AV_{CC} + DV_{CC} excluding external current

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{(AM)}$	Active mode (see Note 1 and Note 4) $f_{(MCLK)} = f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz XTS=0, SELM=(0,1) (FG461x: Program executes from flash)	CG461x	T_A = −40°C to 85°C	V_{CC} = 2.2 V		280	370	µA
				V_{CC} = 3 V		470	580	
		FG461x	T_A = −40°C to 85°C	V_{CC} = 2.2 V		400	480	µA
				V_{CC} = 3 V		600	740	
$I_{(LPM0)}$	Low-power mode (LPM0) (see Note 1 and Note 4)	xG461x	T_A = −40°C to 85°C	V_{CC} = 2.2 V		45	70	µA
				V_{CC} = 3 V		75	110	
$I_{(LPM2)}$	Low-power mode (LPM2), $f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32,768 Hz, SCG0 = 0 (see Note 2 and Note 4)		T_A = −40°C to 85°C	V_{CC} = 2.2 V		11	20	µA
				V_{CC} = 3 V		17	24	
$I_{(LPM3)}$	Low-power mode (LPM3) $f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32,768 Hz, SCG0 = 1 Basic Timer1 enabled, ACLK selected LCD_A enabled, LCDCPEN = 0; (static mode; $f_{LCD} = f_{(ACLK)}$ /32) (see Note 2 and Note 3 and Note 4)		T_A = −40°C	V_{CC} = 2.2 V		1.3	4.0	µA
			T_A = 25°C			1.3	4.0	
			T_A = 60°C			2.22	6.5	
			T_A = 85°C			6.5	15.0	
			T_A = −40°C	V_{CC} = 3 V		1.9	5.0	
			T_A = 25°C			1.9	5.0	
			T_A = 60°C			2.5	7.5	
			T_A = 85°C			7.5	18.0	
$I_{(LPM3)}$	Low-power mode (LPM3) $f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32,768 Hz, SCG0 = 1 Basic Timer1 enabled, ACLK selected LCD_A enabled, LCDCPEN = 0; (4−mux mode; $f_{LCD} = f_{(ACLK)}$ /32) (see Note 2 and Note 3 and Note 4)		T_A = −40°C	V_{CC} = 2.2 V		1.5	5.5	µA
			T_A = 25°C			1.5	5.5	
			T_A = 60°C			2.8	7.0	
			T_A = 85°C			7.2	17.0	
			T_A = −40°C	V_{CC} = 3 V		2.5	6.5	
			T_A = 25°C			2.5	6.5	
			T_A = 60°C			3.2	8.0	
			T_A = 85°C			8.5	20.0	
$I_{(LPM4)}$	Low-power mode (LPM4) $f_{(MCLK)}$ = 0 MHz, $f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 0 Hz, SCG0 = 1 (see Note 2 and Note 4)		T_A = −40°C	V_{CC} = 2.2 V		0.13	1.0	µA
			T_A = 25°C			0.22	1.0	
			T_A = 60°C			0.9	2.5	
			T_A = 85°C			4.3	12.5	
			T_A = −40°C	V_{CC} = 3 V		0.13	1.6	
			T_A = 25°C			0.3	1.6	
			T_A = 60°C			1.1	3.0	
			T_A = 85°C			5.0	15.0	

NOTES: 1. Timer_B is clocked by $f_{(DCOCLK)} = f_{(DCO)}$ = 1 MHz. All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
2. All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
3. The LPM3 currents are characterized with a Micro Crystal CC4V−T1A (9 pF) crystal and OSCCAPx = 1h.
4. Current for brownout included.

Current consumption of active mode versus system frequency, F version:

$$I_{(AM)} = I_{(AM)}\ [1\ MHz] \times f_{(System)}\ [MHz]$$

Current consumption of active mode versus supply voltage, F version:

$$I_{(AM)} = I_{(AM)\ [3\ V]} + 200\ \mu A/V \times (V_{CC} - 3\ V)$$

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

Schmitt-trigger inputs − Ports P1 to P10, $\overline{\text{RST}}$/NMI, JTAG (TCK, TMS, TDI/TCLK, TDO/TDI)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 2.2 V	1.1		1.55	V
		V_{CC} = 3 V	1.5		1.98	
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 2.2 V	0.4		0.9	V
		V_{CC} = 3 V	0.9		1.3	
V_{hys}	Input voltage hysteresis (V_{IT+} − V_{IT-})	V_{CC} = 2.2 V	0.3		1.1	V
		V_{CC} = 3 V	0.5		1	

inputs Px.x, TAx, TBx

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{(int)}$	External interrupt timing	Port P1, P2: P1.x to P2.x, external trigger signal for the interrupt flag, (see Note 1)	2.2 V	62			ns
			3 V	50			
$t_{(cap)}$	Timer_A, Timer_B capture timing	TA0, TA1, TA2 TB0, TB1, TB2, TB3, TB4, TB5, TB6	2.2 V	62			ns
			3 V	50			
$f_{(TAext)}$	Timer_A, Timer_B clock frequency externally applied to pin	TACLK, TBCLK, INCLK: $t_{(H)} = t_{(L)}$	2.2 V			8	MHz
$f_{(TBext)}$			3 V			10	
$f_{(TAint)}$	Timer_A, Timer_B clock frequency	SMCLK or ACLK signal selected	2.2 V			8	MHz
$f_{(TBint)}$			3 V			10	

NOTES: 1. The external signal sets the interrupt flag every time the minimum $t_{(int)}$ parameters are met. It may be set even with trigger signals shorter than $t_{(int)}$.

leakage current − Ports P1 to P10 (see Note 1)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{lkg(Px.y)}$	Leakage current	Port Px	$V_{(Px.y)}$ (see Note 2) $(1 \le x \le 10,\ 0 \le y \le 7)$	V_{CC} = 2.2 V/3 V			±50	nA

NOTES: 1. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
2. The port pin must be selected as input.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

outputs − Ports P1 to P10

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH(max)}$ = −1.5 mA,	V_{CC} = 2.2 V,	See Note 1	V_{CC}−0.25		V_{CC}	V
		$I_{OH(max)}$ = −6 mA,	V_{CC} = 2.2 V,	See Note 2	V_{CC}−0.6		V_{CC}	
		$I_{OH(max)}$ = −1.5 mA,	V_{CC} = 3 V,	See Note 1	V_{CC}−0.25		V_{CC}	
		$I_{OH(max)}$ = −6 mA,	V_{CC} = 3 V,	See Note 2	V_{CC}−0.6		V_{CC}	
V_{OL}	Low-level output voltage	$I_{OL(max)}$ = 1.5 mA,	V_{CC} = 2.2 V,	See Note 1	V_{SS}		V_{SS}+0.25	V
		$I_{OL(max)}$ = 6 mA,	V_{CC} = 2.2 V,	See Note 2	V_{SS}		V_{SS}+0.6	
		$I_{OL(max)}$ = 1.5 mA,	V_{CC} = 3 V,	See Note 1	V_{SS}		V_{SS}+0.25	
		$I_{OL(max)}$ = 6 mA,	V_{CC} = 3 V,	See Note 2	V_{SS}		V_{SS}+0.6	

NOTES: 1. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±12 mA to satisfy the maximum specified voltage drop.
2. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±48 mA to satisfy the maximum specified voltage drop.

output frequency

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{(Px.y)}$	(1 ≤ x ≤ 10, 0 ≤ y ≤ 7)	C_L = 20 pF, I_L = ±1.5 mA	V_{CC} = 2.2 V	DC		10	MHz
			V_{CC} = 3 V	DC		12	MHz
$f_{(MCLK)}$ $f_{(SMCLK)}$	P1.1/TA0/MCLK, P1.4/TBCLK/SMCLK,	C_L = 20 pF	V_{CC} = 2.2 V			10	MHz
$f_{(ACLK)}$	P1.5/TACLK/ACLK		V_{CC} = 3 V	DC		12	MHz
$t_{(Xdc)}$	Duty cycle of output frequency	P1.5/TACLK/ACLK, C_L = 20 pF V_{CC} = 2.2 V / 3 V	$f_{(ACLK)} = f_{(LFXT1)} = f_{(XT1)}$	40%		60%	
			$f_{(ACLK)} = f_{(LFXT1)} = f_{(LF)}$	30%		70%	
			$f_{(ACLK)} = f_{(LFXT1)}$		50%		
		P1.1/TA0/MCLK, C_L = 20 pF, V_{CC} = 2.2 V / 3 V	$f_{(MCLK)} = f_{(XT1)}$	40%		60%	
			$f_{(MCLK)} = f_{(DCOCLK)}$	50%− 15 ns	50%	50%+ 15 ns	
		P1.4/TBCLK/SMCLK, C_L = 20 pF, V_{CC} = 2.2 V / 3 V	$f_{(SMCLK)} = f_{(XT2)}$	40%		60%	
			$f_{(SMCLK)} = f_{(DCOCLK)}$	50%− 15 ns	50%	50%+ 15 ns	

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics − outputs

TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

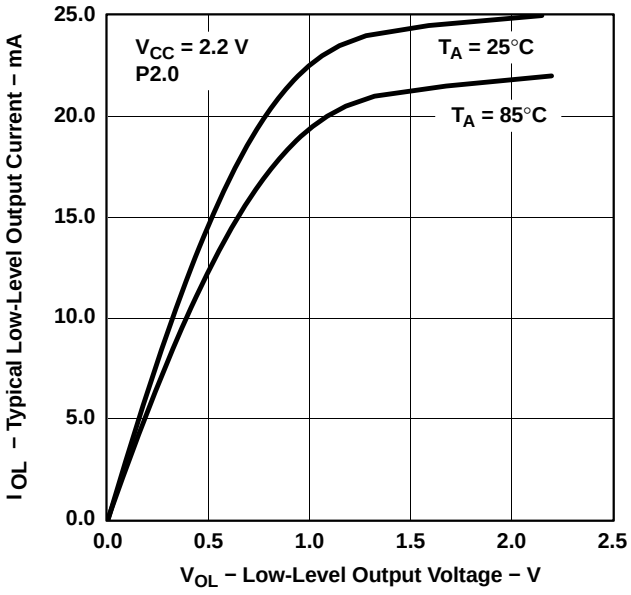


Figure 2

TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

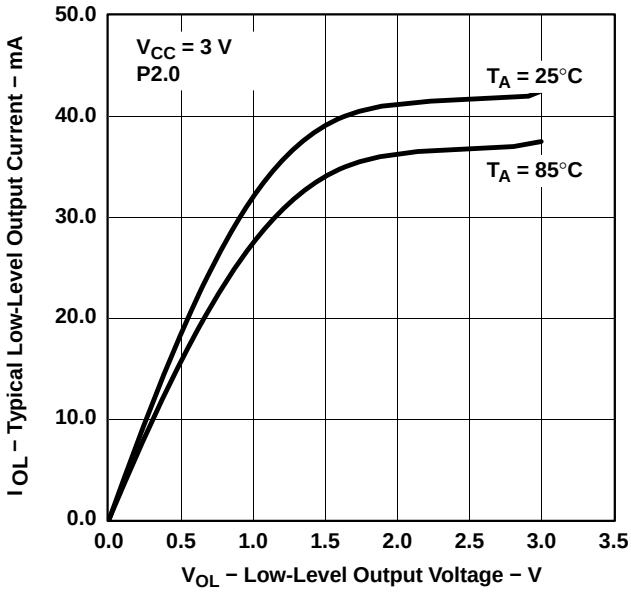


Figure 3

TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

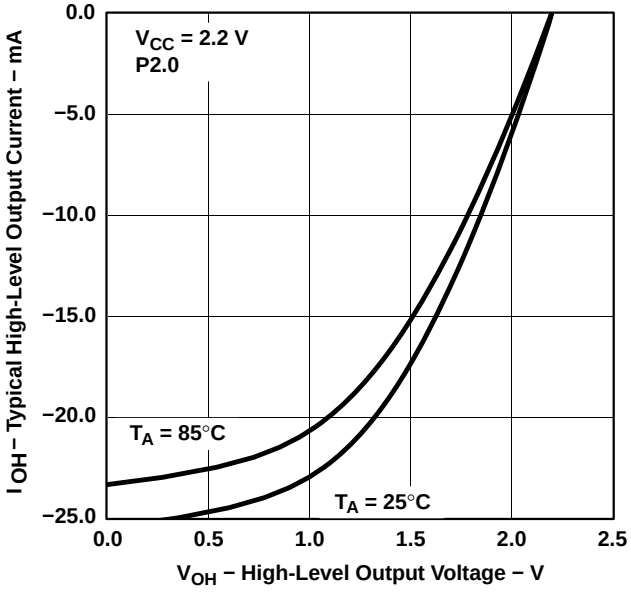


Figure 4

TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

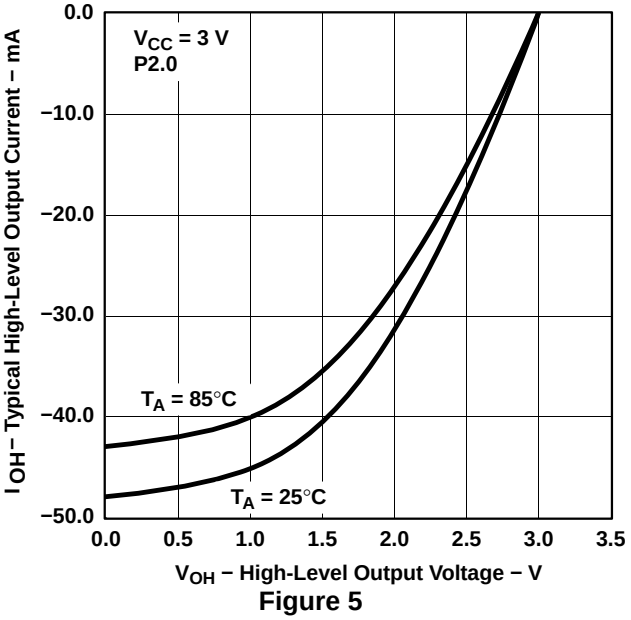


Figure 5

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

wake-up LPM3

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(LPM3)}$	Delay time	f = 1 MHz	V_{CC} = 2.2 V/3 V			6	µs
		f = 2 MHz				6	
		f = 3 MHz				6	

RAM

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VRAMh	CPU halted (see Note 1)	1.6			V

NOTE 1: This parameter defines the minimum supply voltage when the data in program memory RAM remain unchanged. No program execution should take place during this supply voltage condition.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

LCD_A

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(LCD)}$	Supply voltage (see Note 2)	Charge pump enabled (LCDCPEN = 1; VLCDx > 0000)		2.2		3.6	V
$I_{CC(LCD)}$	Supply current (see Note 2)	$V_{LCD(typ)}$=3 V; LCDCPEN = 1, VLCDx= 1000; all segments on, $f_{LCD} = f_{ACLK}/32$, no LCD connected (see Note 4) T_A = 25°C	2.2 V		3		µA
C_{LCD}	Capacitor on LCDCAP (see Note 1 and Note 3)	Charge pump enabled (LCDCPEN = 1; VLCDx > 0000)		4.7			µF
f_{LCD}	LCD frequency					1.1	kHz
V_{LCD}	LCD voltage (see Note 3)	VLCDx = 0000			V_{CC}		V
		VLCDx = 0001			2.60		
		VLCDx = 0010			2.66		
		VLCDx = 0011			2.72		
		VLCDx = 0100			2.78		
		VLCDx = 0101			2.84		
		VLCDx = 0110			2.90		
		VLCDx = 0111			2.96		
		VLCDx = 1000			3.02		
		VLCDx = 1001			3.08		
		VLCDx = 1010			3.14		
		VLCDx = 1011			3.20		
		VLCDx = 1100			3.26		
		VLCDx = 1101			3.32		
		VLCDx = 1110			3.38		
		VLCDx = 1111			3.44	3.60	
R_{LCD}	LCD driver output impedance	V_{LCD}=3 V; CPEN = 1; VLCDx = 1000, I_{LOAD} = ± 10 µA	2.2 V			10	kΩ

NOTES: 1. Enabling the internal charge pump with an external capacitor smaller than the minimum specified might damage the device.
2. Refer to the supply current specifications $I_{(LPM3)}$ for additional current specifications with the LCD_A module active.
3. Segments S0 through S3 are disabled when the LCD charge pump feature is enabled (LCDCPEN = 1) and cannot be used together with the LCD charge pump. In addition, when using segments S0 through S3 with an external LCD voltage supply, $V_{LCD} \leq AV_{CC}$.
4. Connecting an actual display will increase the current consumption depending on the size of the LCD.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

Comparator_A (see Note 1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{(CC)}$		CAON=1, CARSEL=0, CAREF=0	V_{CC} = 2.2 V		25	40	µA
			V_{CC} = 3 V		45	60	
$I_{(Refladder/RefDiode)}$		CAON=1, CARSEL=0, CAREF=1/2/3, No load at P1.6/CA0 and P1.7/CA1	V_{CC} = 2.2 V		30	50	µA
			V_{CC} = 3 V		45	71	
$V_{(Ref025)}$	$\frac{\text{Voltage @ 0.25 } V_{CC} \text{ node}}{V_{CC}}$	PCA0=1, CARSEL=1, CAREF=1, No load at P1.6/CA0 and P1.7/CA1	V_{CC} = 2.2 V / 3 V	0.23	0.24	0.25	
$V_{(Ref050)}$	$\frac{\text{Voltage @ 0.5 } V_{CC} \text{ node}}{V_{CC}}$	PCA0=1, CARSEL=1, CAREF=2, No load at P1.6/CA0 and P1.7/CA1	V_{CC} = 2.2V / 3 V	0.47	0.48	0.5	
$V_{(RefVT)}$		PCA0=1, CARSEL=1, CAREF=3, No load at P1.6/CA0 and P1.7/CA1; T_A = 85°C	V_{CC} = 2.2 V	390	480	540	mV
			V_{CC} = 3 V	400	490	550	
V_{IC}	Common-mode input voltage range	CAON=1	V_{CC} = 2.2 V / 3 V	0		V_{CC}−1	V
V_p−V_S	Offset voltage	See Note 2	VCC = 2.2 V / 3 V	−30		30	mV
V_{hys}	Input hysteresis	CAON = 1	V_{CC} = 2.2 V / 3 V	0	0.7	1.4	mV
$t_{(response\ LH)}$		T_A = 25°C, Overdrive 10 mV, without filter: CAF = 0	V_{CC} = 2.2 V	160	210	300	ns
			V_{CC} = 3 V	80	150	240	
		T_A = 25°C Overdrive 10 mV, with filter: CAF = 1	V_{CC} = 2.2 V	1.4	1.9	3.4	µs
			V_{CC} = 3 V	0.9	1.5	2.6	
$t_{(response\ HL)}$		T_A = 25°C Overdrive 10 mV, without filter: CAF = 0	V_{CC} = 2.2 V	130	210	300	ns
			V_{CC} = 3 V	80	150	240	
		T_A = 25°C, Overdrive 10 mV, with filter: CAF = 1	V_{CC} = 2.2 V	1.4	1.9	3.4	µs
			V_{CC} = 3 V	0.9	1.5	2.6	

NOTES: 1. The leakage current for the Comparator_A terminals is identical to $I_{lkg(Px.x)}$ specification.
2. The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A inputs on successive measurements. The two successive measurements are then summed together.

typical characteristics

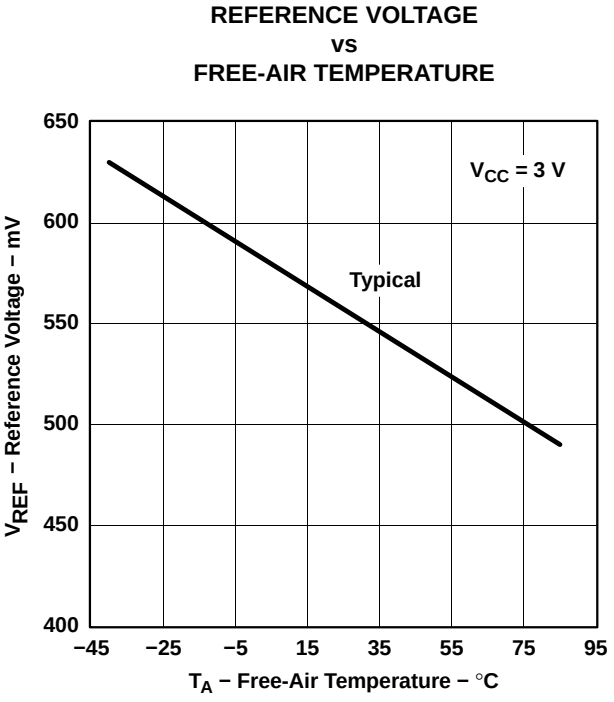


Figure 6. $V_{(RefVT)}$ vs Temperature

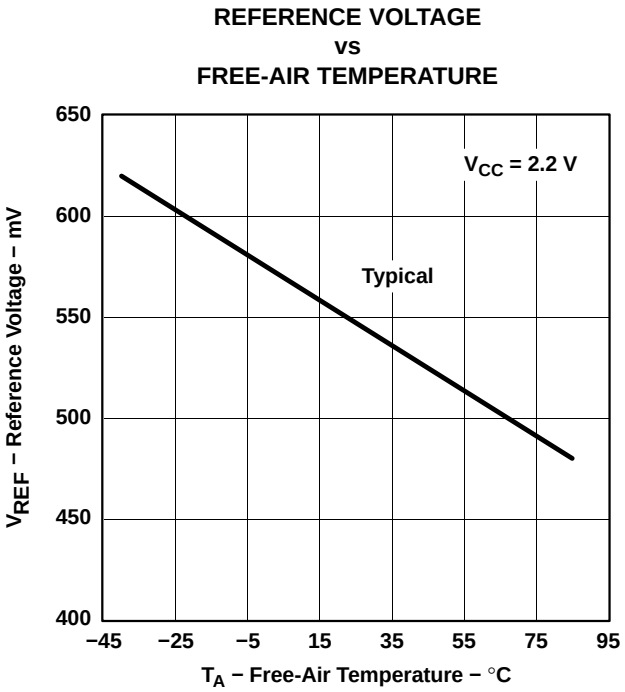


Figure 7. $V_{(RefVT)}$ vs Temperature

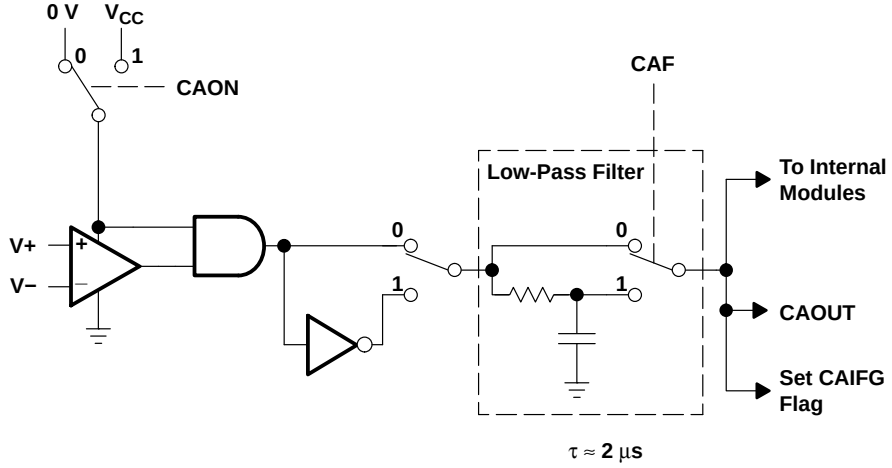


Figure 8. Block Diagram of Comparator_A Module

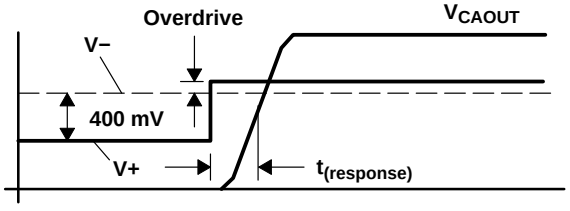


Figure 9. Overdrive Definition

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

POR/brownout reset (BOR) (see Note 1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(BOR)}$	Brownout (see Notes 2 and 3)				2000	µs
$V_{CC(start)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 10)		$0.7 \times V_{(B\_IT-)}$		V
$V_{(B\_IT-)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 10 through Figure 12)			1.79	V
$V_{hys(B\_IT-)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 10)	70	130	210	mV
$t_{(reset)}$		Pulse length needed at $\overline{RST}$/NMI pin to accepted reset internally, V_{CC} = 2.2 V/3 V	2			µs

NOTES: 1. The current consumption of the brownout module is already included in the I_{CC} current consumption data.
2. The voltage level $V_{(B\_IT-)} + V_{hys(B\_IT-)}$ is ≤ 1.89V.
3. During power up, the CPU begins code execution following a period of $t_{d(BOR)}$ after $V_{CC} = V_{(B\_IT-)} + V_{hys(B\_IT-)}$. The default FLL+ settings must not be changed until $V_{CC} \ge V_{CC(min)}$, where $V_{CC(min)}$ is the minimum supply voltage for the desired operating frequency. See the *MSP430x4xx Family User's Guide* for more information on the brownout/SVS circuit.

typical characteristics

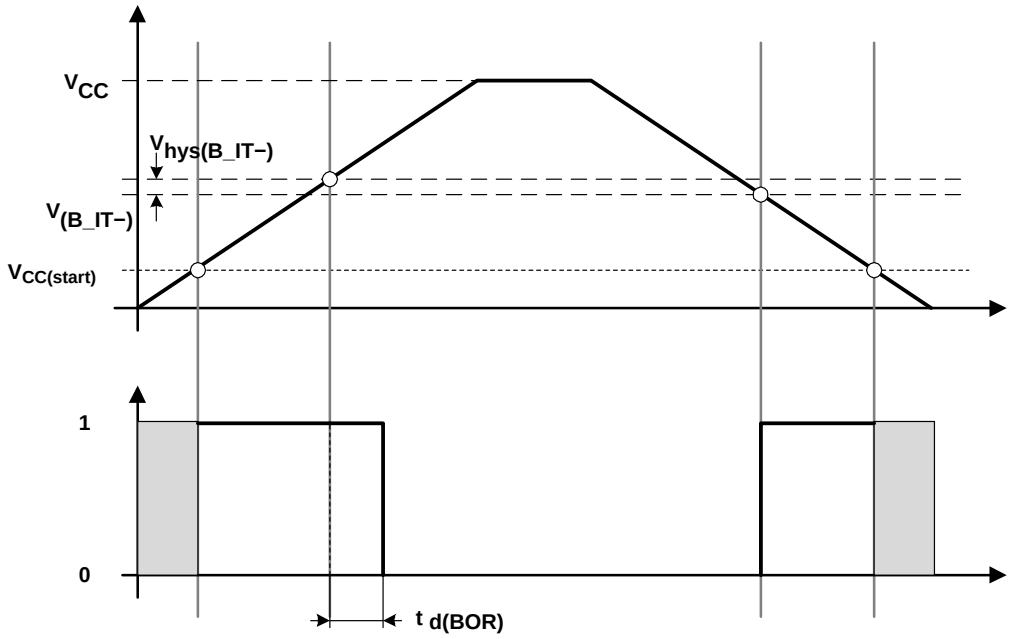


Figure 10. POR/Brownout Reset (BOR) vs Supply Voltage

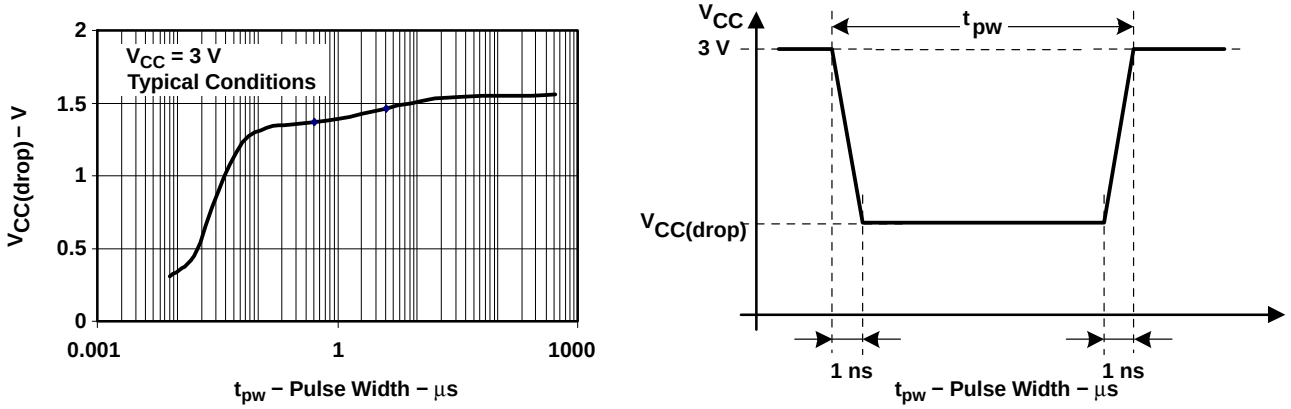


Figure 11. $V_{CC(drop)}$ Level With a Square Voltage Drop to Generate a POR/Brownout Signal

typical characteristics (continued)

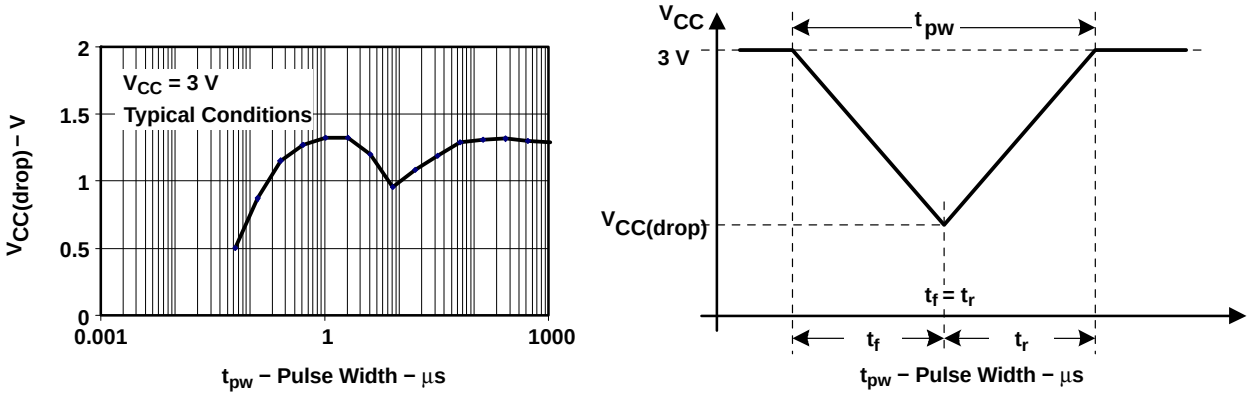


Figure 12. $V_{CC(drop)}$ Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

SVS (supply voltage supervisor/monitor) (see Note 1)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{(SVSR)}$	dV_{CC}/dt > 30 V/ms (see Figure 13)		5		150	µs
	$dV_{CC}/dt \le 30$ V/ms				2000	
$t_{d(SVSon)}$	SVS on, switch from VLD = 0 to VLD ≠ 0, V_{CC} = 3 V			150	300	µs
t_{settle}	VLD ≠ 0‡				12	µs
$V_{(SVSstart)}$	VLD ≠ 0, $V_{CC}/dt \le 3$ V/s (see Figure 13)			1.55	1.7	V
$V_{hys(SVS\_IT-)}$	$V_{CC}/dt \le 3$ V/s (see Figure 13)	VLD = 1	70	120	155	mV
		VLD = 2 .. 14	$V_{(SVS\_IT-)}$ x 0.001		$V_{(SVS\_IT-)}$ x 0.016	
	$V_{CC}/dt \le 3$ V/s (see Figure 13), external voltage applied on A7	VLD = 15	4.4		20	mV
$V_{(SVS\_IT-)}$	$V_{CC}/dt \le 3$ V/s (see Figure 13)	VLD = 1	1.8	1.9	2.05	V
		VLD = 2	1.94	2.1	2.23	
		VLD = 3	2.05	2.2	2.35	
		VLD = 4	2.14	2.3	2.46	
		VLD = 5	2.24	2.4	2.58	
		VLD = 6	2.33	2.5	2.69	
		VLD = 7	2.46	2.65	2.84	
		VLD = 8	2.58	2.8	2.97	
		VLD = 9	2.69	2.9	3.10	
		VLD = 10	2.83	3.05	3.26	
		VLD = 11	2.94	3.2	3.39	
		VLD = 12	3.11	3.35	3.58†	
		VLD = 13	3.24	3.5	3.73†	
		VLD = 14	3.43	3.7†	3.96†	
	$V_{CC}/dt \le 3$ V/s (see Figure 13), external voltage applied on A7	VLD = 15	1.1	1.2	1.3	
$I_{CC(SVS)}$ (see Note 1)	VLD ≠ 0, V_{CC} = 2.2 V/3 V			10	15	µA

† The recommended operating voltage range is limited to 3.6 V.

‡ t_{settle} is the settling time that the comparator o/p needs to have a stable level after VLD is switched VLD ≠ 0 to a different VLD value somewhere between 2 and 15. The overdrive is assumed to be > 50 mV.

NOTE 1: The current consumption of the SVS module is not included in the I_{CC} current consumption data.

typical characteristics

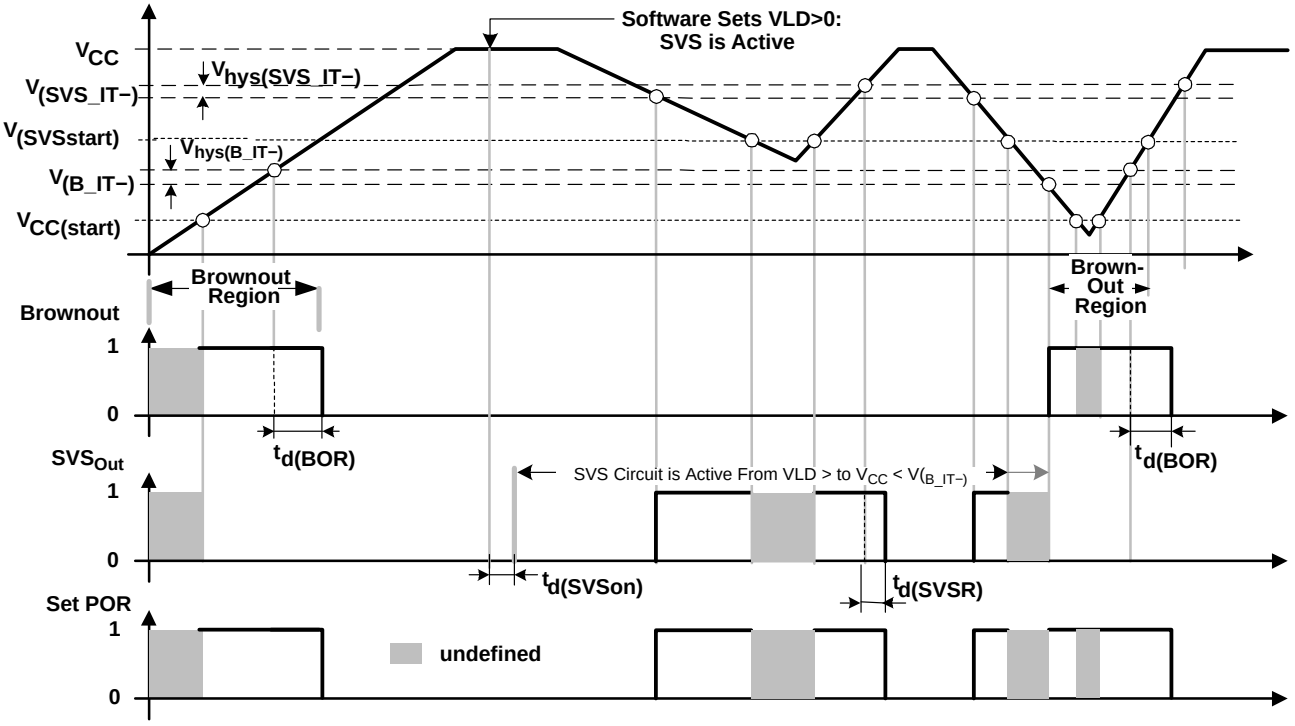


Figure 13. SVS Reset (SVSR) vs Supply Voltage

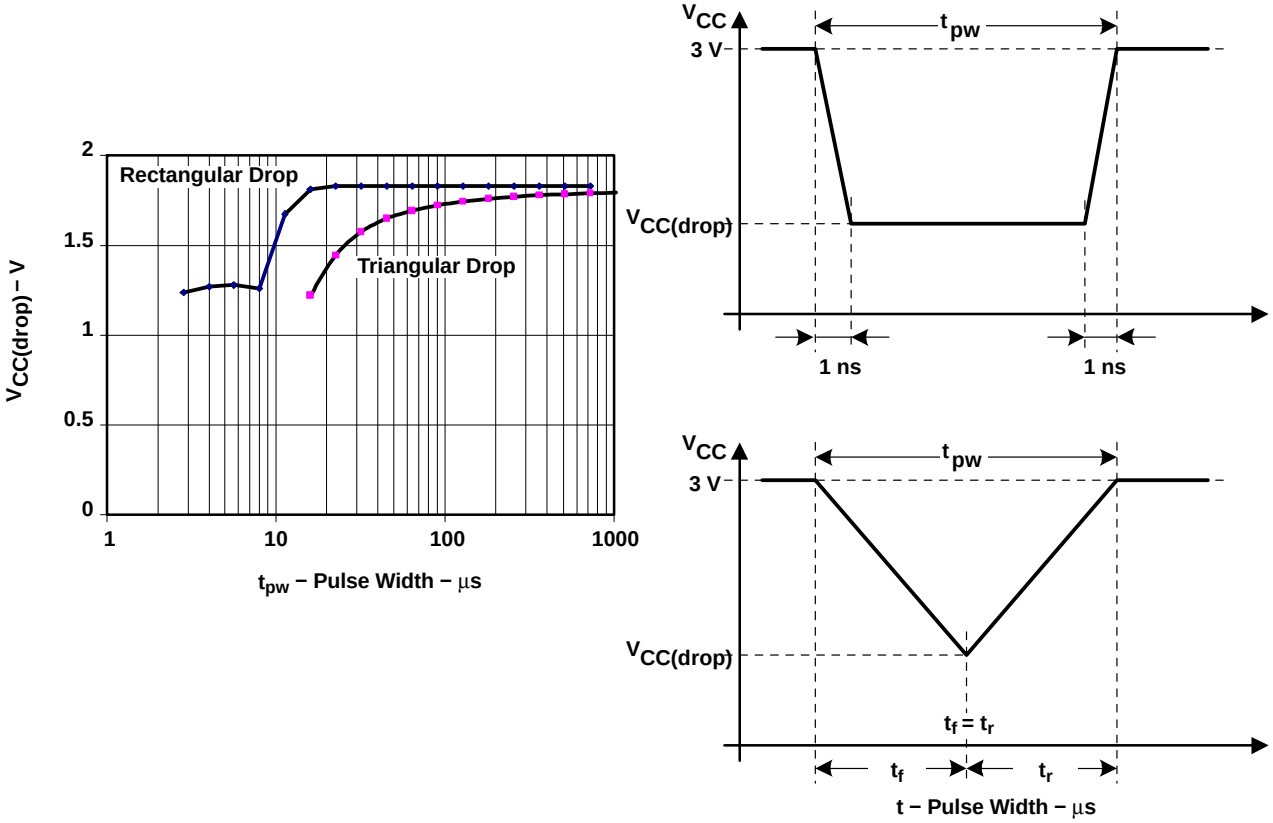


Figure 14. $V_{CC(drop)}$ With a Square Voltage Drop and a Triangle Voltage Drop to Generate an SVS Signal

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

DCO

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{(DCOCLK)}$	$N_{(DCO)}$=01Eh, FN_8=FN_4=FN_3=FN_2=0, D = 2; DCOPLUS= 0	2.2 V/3 V		1		MHz
$f_{(DCO=2)}$	FN_8=FN_4=FN_3=FN_2=0 ; DCOPLUS = 1	2.2 V	0.3	0.65	1.25	MHz
		3 V	0.3	0.7	1.3	
$f_{(DCO=27)}$	FN_8=FN_4=FN_3=FN_2=0; DCOPLUS = 1	2.2 V	2.5	5.6	10.5	MHz
		3 V	2.7	6.1	11.3	
$f_{(DCO=2)}$	FN_8=FN_4=FN_3=0, FN_2=1; DCOPLUS = 1	2.2 V	0.7	1.3	2.3	MHz
		3 V	0.8	1.5	2.5	
$f_{(DCO=27)}$	FN_8=FN_4=FN_3=0, FN_2=1; DCOPLUS = 1	2.2 V	5.7	10.8	18	MHz
		3 V	6.5	12.1	20	
$f_{(DCO=2)}$	FN_8=FN_4=0, FN_3= 1, FN_2=x; DCOPLUS = 1	2.2 V	1.2	2	3	MHz
		3 V	1.3	2.2	3.5	
$f_{(DCO=27)}$	FN_8=FN_4=0, FN_3= 1, FN_2=x; DCOPLUS = 1	2.2 V	9	15.5	25	MHz
		3 V	10.3	17.9	28.5	
$f_{(DCO=2)}$	FN_8=0, FN_4= 1, FN_3= FN_2=x; DCOPLUS = 1	2.2 V	1.8	2.8	4.2	MHz
		3 V	2.1	3.4	5.2	
$f_{(DCO=27)}$	FN_8=0, FN_4=1, FN_3= FN_2=x; DCOPLUS = 1	2.2 V	13.5	21.5	33	MHz
		3 V	16	26.6	41	
$f_{(DCO=2)}$	FN_8=1, FN_4=FN_3=FN_2=x; DCOPLUS = 1	2.2 V	2.8	4.2	6.2	MHz
		3 V	4.2	6.3	9.2	
$f_{(DCO=27)}$	FN_8=1,FN_4=FN_3=FN_2=x; DCOPLUS = 1	2.2 V	21	32	46	MHz
		3 V	30	46	70	
S_n	Step size between adjacent DCO taps: $S_n = f_{DCO(Tap\ n+1)} / f_{DCO(Tap\ n)}$ (see Figure 16 for taps 21 to 27)	1 < TAP ≤ 20	1.06		1.11	
		TAP = 27	1.07		1.17	
D_t	Temperature drift, $N_{(DCO)}$ = 01Eh, FN_8=FN_4=FN_3=FN_2=0 D = 2; DCOPLUS = 0	2.2 V	–0.2	–0.3	–0.4	%/°C
		3 V	–0.2	–0.3	–0.4	
D_V	Drift with V_{CC} variation, $N_{(DCO)}$ = 01Eh, FN_8=FN_4=FN_3=FN_2=0 D = 2; DCOPLUS = 0		0	5	15	%/V

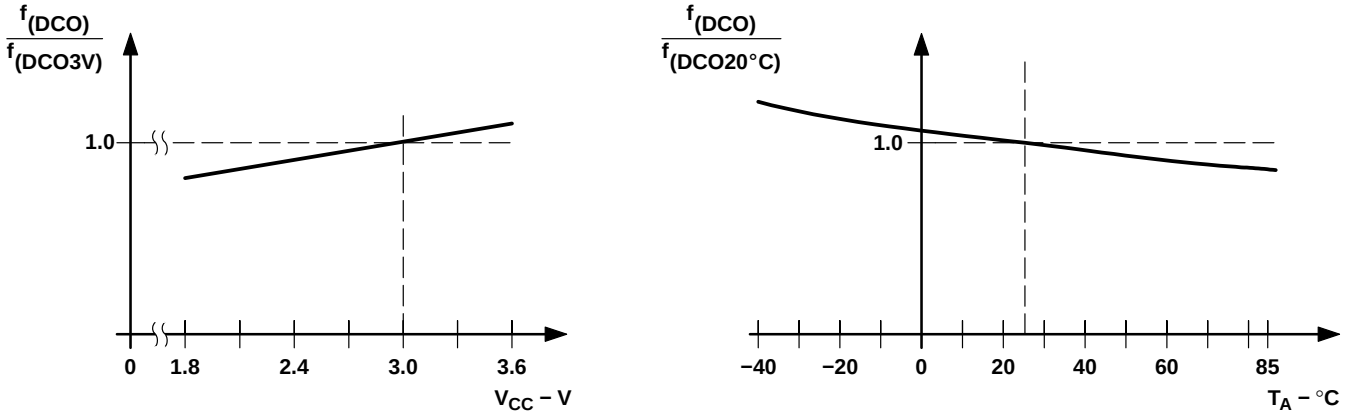


Figure 15. DCO Frequency vs Supply Voltage V_{CC} and vs Ambient Temperature

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

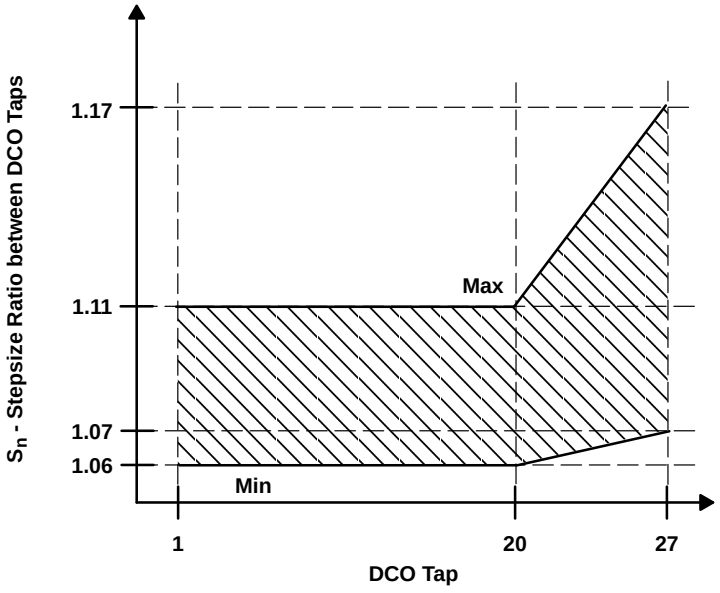


Figure 16. DCO Tap Step Size

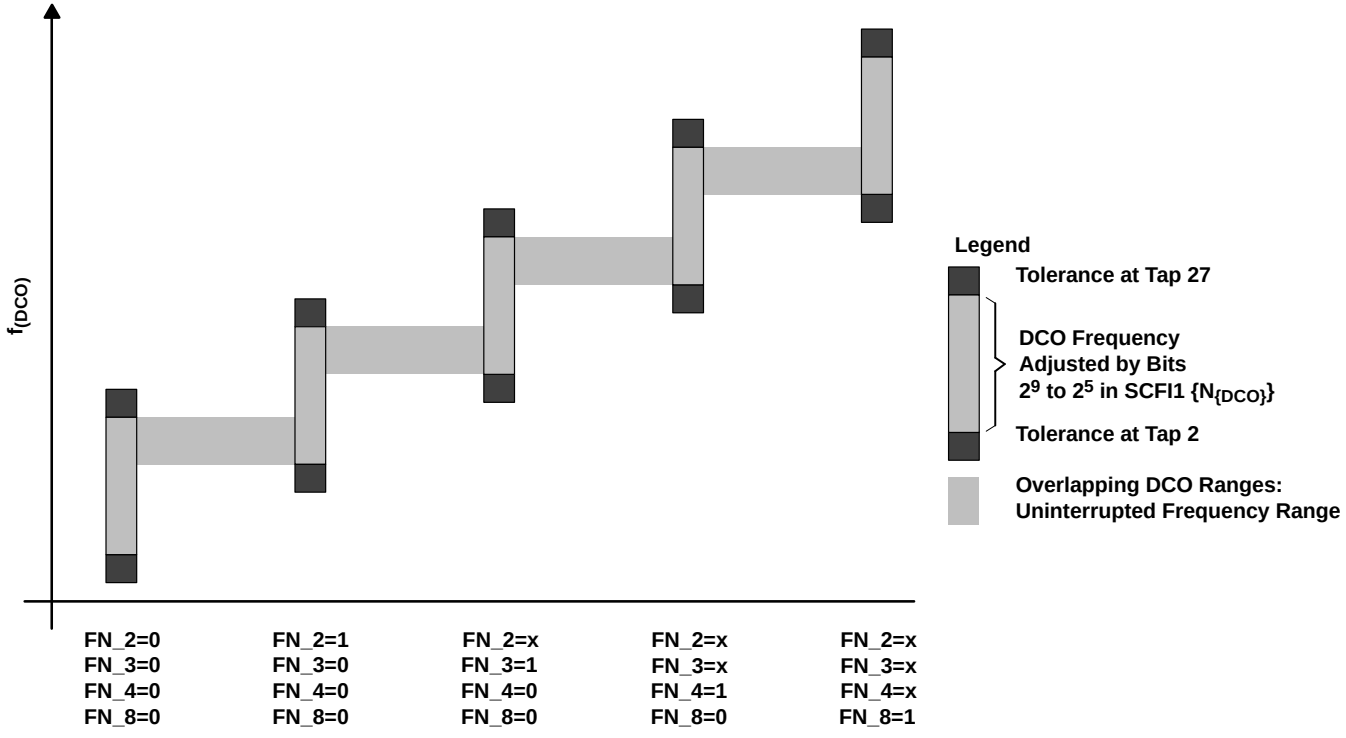


Figure 17. Five Overlapping DCO Ranges Controlled by FN_x Bits

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

crystal oscillator, LFXT1 oscillator (see Notes 1 and 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{XIN}	Integrated input capacitance (see Note 4)	OSCCAPx = 0h, V_{CC} = 2.2 V / 3 V		0		pF
		OSCCAPx = 1h, V_{CC} = 2.2 V / 3 V		10		
		OSCCAPx = 2h, V_{CC} = 2.2 V / 3 V		14		
		OSCCAPx = 3h, V_{CC} = 2.2 V / 3 V		18		
C_{XOUT}	Integrated output capacitance (see Note 4)	OSCCAPx = 0h, V_{CC} = 2.2 V / 3 V		0		pF
		OSCCAPx = 1h, V_{CC} = 2.2 V / 3 V		10		
		OSCCAPx = 2h, V_{CC} = 2.2 V / 3 V		14		
		OSCCAPx = 3h, V_{CC} = 2.2 V / 3 V		18		
V_{IL}	Input levels at XIN	V_{CC} = 2.2 V/3 V (see Note 3)	V_{SS}		$0.2 \times V_{CC}$	V
V_{IH}			$0.8 \times V_{CC}$		V_{CC}	

NOTES: 1. The parasitic capacitance from the package and board may be estimated to be 2 pF. The effective load capacitor for the crystal is (C_{XIN} x C_{XOUT}) / (C_{XIN} + C_{XOUT}). This is independent of XTS_FLL.

2. To improve EMI on the low-power LFXT1 oscillator, particularly in the LF mode (32 kHz), the following guidelines should be observed.
   - Keep the trace between the device and the crystal as short as possible.
   - Design a good ground plane around the oscillator pins.
   - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
   - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
   - Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
   - If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
   - Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.
3. Applies only when using an external logic-level clock source. XTS_FLL must be set. Not applicable when using a crystal or resonator.
4. External capacitance is recommended for precision real-time clock applications; OSCCAPx = 0h.

crystal oscillator, XT2 oscillator (see Note 1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
C_{XT2IN}	Integrated input capacitance	V_{CC} = 2.2 V/3 V		2		pF
C_{XT2OUT}	Integrated output capacitance	V_{CC} = 2.2 V/3 V		2		pF
V_{IL}	Input levels at XT2IN	V_{CC} = 2.2 V/3 V (see Note 2)	V_{SS}		$0.2 \times V_{CC}$	V
V_{IH}			$0.8 \times V_{CC}$		V_{CC}	V

NOTES: 1. The oscillator needs capacitors at both terminals, with values specified by the crystal manufacturer.

2. Applies only when using an external logic-level clock source. Not applicable when using a crystal or resonator.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

USCI (UART mode)

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty Cycle = 50% ± 10%				f_{SYSTEM}	MHz
f_{BITCLK}	BITCLK clock frequency (equals Baudrate in MBaud)		2.2V /3 V			1	MHz
t_τ	UART receive deglitch time (see Note 1)		2.2 V	50	150	600	ns
			3 V	50	100	600	

NOTE 1: Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized their width should exceed the maximum specification of the deglitch time.

USCI (SPI master mode) (see Figure 18 and Figure 19)

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	SMCLK, ACLK Duty Cycle = 50% ± 10%				f_{SYSTEM}	MHz
$t_{SU,MI}$	SOMI input data setup time		2.2 V	110			ns
			3 V	75			
$t_{HD,MI}$	SOMI input data hold time		2.2 V	0			ns
			3 V	0			
$t_{VALID,MO}$	SIMO output data valid time	UCLK edge to SIMO valid; C_L = 20 pF	2.2 V			30	ns
			3 V			20	

USCI (SPI slave mode) (see Figure 20 and Figure 21)

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
$t_{STE,LEAD}$	STE lead time STE low to clock		2.2 V/3 V		50		ns
$t_{STE,LAG}$	STE lag time Last clock to STE high		2.2 V/3 V	10			ns
$t_{STE,ACC}$	STE access time STE low to SOMI data out		2.2 V/3 V		50		ns
$t_{STE,DIS}$	STE disable time STE high to SOMI high impedance		2.2 V/3 V		50		ns
$t_{SU,SI}$	SIMO input data setup time		2.2 V	20			ns
			3 V	15			
$t_{HD,SI}$	SIMO input data hold time		2.2 V	10			ns
			3 V	10			
$t_{VALID,SO}$	SOMI output data valid time	UCLK edge to SOMI valid; C_L = 20 pF	2.2 V		75	110	ns
			3 V		50	75	

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

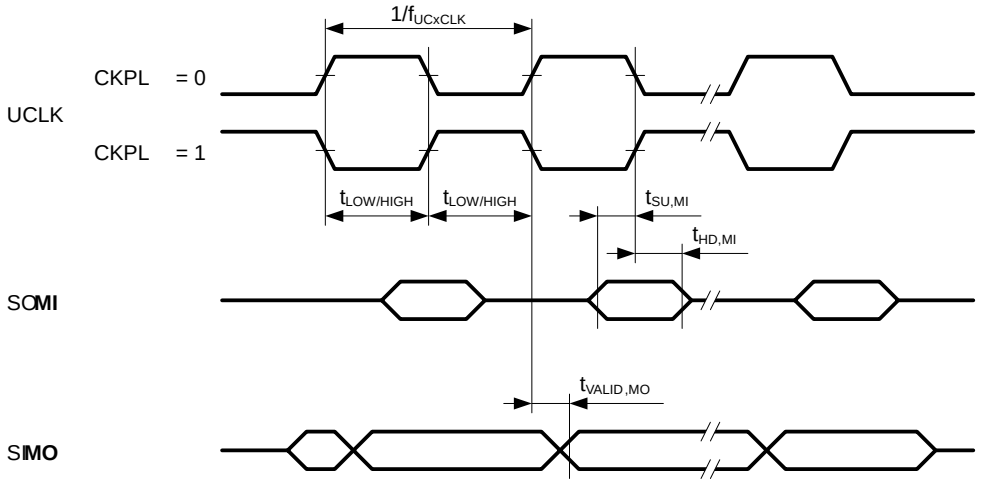


Figure 18. SPI Master Mode, CKPH = 0

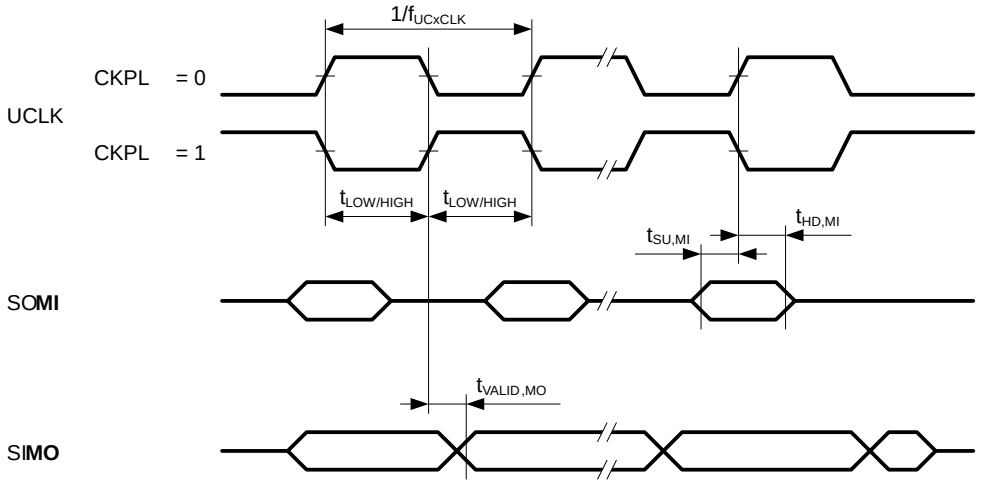


Figure 19. SPI Master Mode, CKPH = 1

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

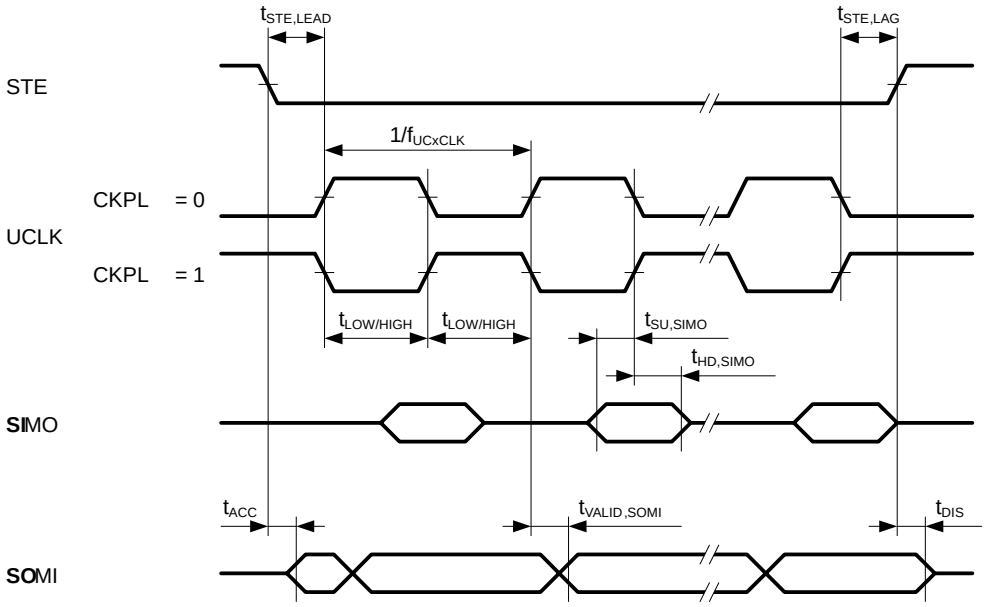


Figure 20. SPI Slave Mode, CKPH = 0

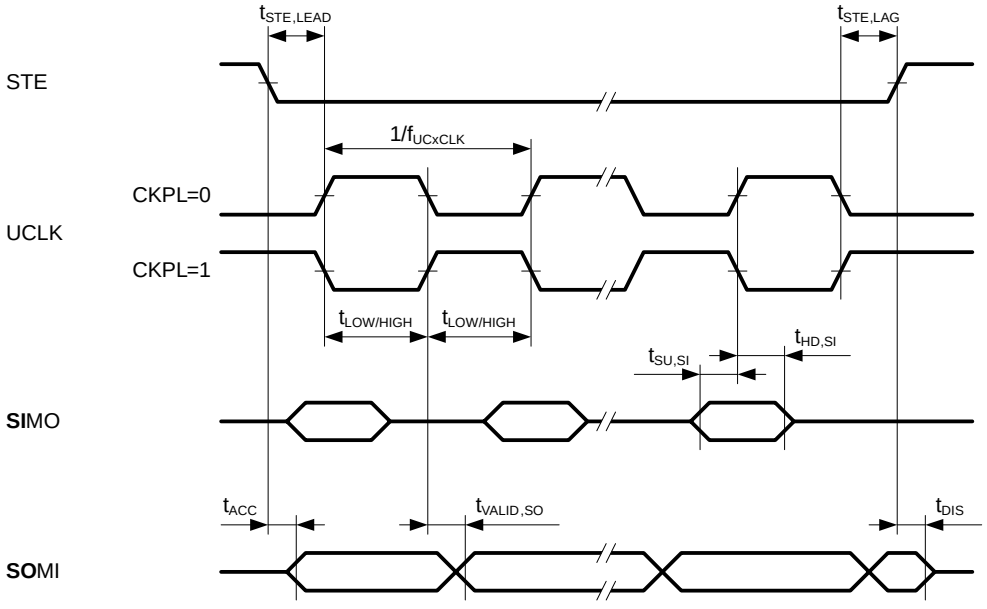


Figure 21. SPI Slave Mode, CKPH = 1

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

USCI (I2C mode) (see Figure 22)

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty Cycle = 50% ± 10%				f_{SYSTEM}	MHz
f_{SCL}	SCL clock frequency		2.2 V/3 V	0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	$f_{SCL} \le 100kHz$	2.2 V/3 V	4.0			µs
		$f_{SCL} > 100kHz$	2.2 V/3 V	0.6			
$t_{SU,STA}$	Set−up time for a repeated START	$f_{SCL} \le 100kHz$	2.2 V/3 V	4.7			µs
		$f_{SCL} > 100kHz$	2.2 V/3 V	0.6			
$t_{HD,DAT}$	Data hold time		2.2 V/3 V	0			ns
$t_{SU,DAT}$	Data set−up time		2.2 V/3 V	250			ns
$t_{SU,STO}$	Set−up time for STOP		2.2 V/3 V	4.0			µs
t_{SP}	Pulse width of spikes suppressed by input filter		2.2 V	50	150	600	ns
			3 V	50	100	600	

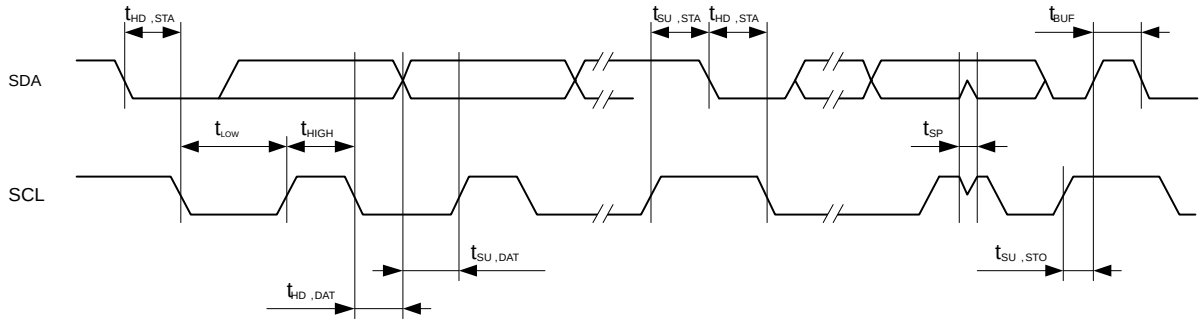


Figure 22. I2C Mode Timing

USART1 (see Note 1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(\tau)}$	USART1 deglitch time	V_{CC} = 2.2 V, SYNC = 0, UART mode	200	430	800	ns
		V_{CC} = 3 V, SYNC = 0, UART mode	150	280	500	

NOTE 1: The signal applied to the USART1 receive signal/terminal (URXD1) should meet the timing requirements of $t_{(\tau)}$ to ensure that the URXS flip-flop is set. The URXS flip-flop is set with negative pulses meeting the minimum-timing condition of $t_{(\tau)}$. The operating conditions to set the flag must be met independently from this timing constraint. The deglitch circuitry is active only on negative transitions on the URXD1 line.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC, power supply and input range conditions (see Note 1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	AV_{CC} and DV_{CC} are connected together, AV_{SS} and DV_{SS} are connected together, $V_{(AVSS)} = V_{(DVSS)} = 0$ V		2.2		3.6	V
$V_{(P6.x/Ax)}$	Analog input voltage range (see Note 2)	All external Ax terminals. Analog inputs selected in ADC12MCTLx register and P6Sel.x=1, $V_{(AVSS)} \le V_{Ax} \le V_{(AVCC)}$		0		V_{AVCC}	V
I_{ADC12}	Operating supply current into AV_{CC} terminal (see Note 3)	$f_{ADC12CLK}$ = 5.0 MHz, ADC12ON = 1, REFON = 0, SHT0=0, SHT1=0, ADC12DIV=0	V_{CC} = 2.2 V		0.65	1.3	mA
			V_{CC} = 3 V		0.8	1.6	
I_{REF+}	Operating supply current into AV_{CC} terminal (see Note 4)	$f_{ADC12CLK}$ = 5.0 MHz, ADC12ON = 0, REFON = 1, REF2_5V = 1	V_{CC} = 3 V		0.5	0.8	mA
		$f_{ADC12CLK}$ = 5.0 MHz, ADC12ON = 0, REFON = 1, REF2_5V = 0	V_{CC} = 2.2 V		0.5	0.8	mA
			V_{CC} = 3 V		0.5	0.8	
C_I	Input capacitance	Only one terminal can be selected at one time, Ax	V_{CC} = 2.2 V			40	pF
R_I	Input MUX ON resistance	$0V \le V_{Ax} \le V_{AVCC}$	V_{CC} = 3 V			2000	Ω

NOTES: 1. The leakage current is defined in the leakage current table with Ax parameter.
2. The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.
3. The internal reference supply current is not included in current consumption parameter I_{ADC12}.
4. The internal reference current is supplied via terminal AV_{CC}. Consumption is independent of the ADC12ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an A/D conversion.

12-bit ADC, external reference (see Note 1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{eREF+}	Positive external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$, (see Note 2)		1.4		V_{AVCC}	V
V_{REF-}/V_{eREF-}	Negative external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$, (see Note 3)		0		1.2	V
$(V_{eREF+} - V_{REF-}/V_{eREF-})$	Differential external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$, (see Note 4)		1.4		V_{AVCC}	V
I_{VeREF+}	Input leakage current	$0V \le V_{eREF+} \le V_{AVCC}$	V_{CC} = 2.2 V/3 V			±1	µA
$I_{VREF-/VeREF-}$	Input leakage current	$0V \le V_{eREF-} \le V_{AVCC}$	V_{CC} = 2.2 V/3 V			±1	µA

NOTES: 1. The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, C_I, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.
2. The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
3. The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
4. The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC, built-in reference

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
V_{REF+}	Positive built-in reference voltage output	REF2_5V = 1 for 2.5 V, $I_{VREF+}max \le I_{VREF+} \le I_{VREF+}min$	V_{CC} = 3 V	2.4	2.5	2.6	V
		REF2_5V = 0 for 1.5 V, $I_{VREF+}max \le I_{VREF+} \le I_{VREF+}min$	V_{CC} = 2.2 V/3 V	1.44	1.5	1.56	
$AV_{CC(min)}$	AV_{CC} minimum voltage, Positive built-in reference active	REF2_5V = 0, $I_{VREF+}max \le I_{VREF+} \le I_{VREF+}min$		2.2			V
		REF2_5V = 1, $I_{VREF+}min \ge I_{VREF+} \ge -0.5mA$		2.8			
		REF2_5V = 1, $I_{VREF+}min \ge I_{VREF+} \ge -1mA$		2.9			
I_{VREF+}	Load current out of V_{REF+} terminal		V_{CC} = 2.2 V	0.01		−0.5	mA
			V_{CC} = 3 V	0.01		−1	
$I_{L(VREF)+}$	Load-current regulation V_{REF+} terminal	I_{VREF+} = 500 µA +/− 100 µA, Analog input voltage ~0.75 V; REF2_5V = 0	V_{CC} = 2.2 V			±2	LSB
			V_{CC} = 3 V			±2	
		I_{VREF+} = 500 µA ± 100 µA, Analog input voltage ~1.25 V, REF2_5V = 1	V_{CC} = 3 V			±2	LSB
$I_{DL(VREF)+}$	Load current regulation V_{REF+} terminal	I_{VREF+} =100 µA → 900 µA, C_{VREF+}=5 µF, ax ~0.5 x V_{REF+}, Error of conversion result ≤ 1 LSB	V_{CC} = 3 V			20	ns
C_{VREF+}	Capacitance at pin V_{REF+} (see Note 1)	REFON =1, 0 mA ≤ I_{VREF+} ≤ I_{VREF+}max	V_{CC} = 2.2 V/3 V	5	10		µF
T_{REF+}	Temperature coefficient of built-in reference	I_{VREF+} is a constant in the range of 0 mA ≤ I_{VREF+} ≤ 1 mA	V_{CC} = 2.2 V/3 V			±100	ppm/°C
t_{REFON}	Settle time of internal reference voltage (see Figure 23 and Note 2)	I_{VREF+} = 0.5 mA, C_{VREF+} = 10 µF, V_{REF+} = 1.5 V, V_{AVCC} = 2.2 V				17	ms

NOTES: 1. The internal buffer operational amplifier and the accuracy specifications require an external capacitor. All INL and DNL tests uses two capacitors between pins V_{REF+} and AV_{SS} and V_{REF-}/V_{eREF-} and AV_{SS}: 10 µF tantalum and 100 nF ceramic.
2. The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB. The settling time depends on the external capacitive load.

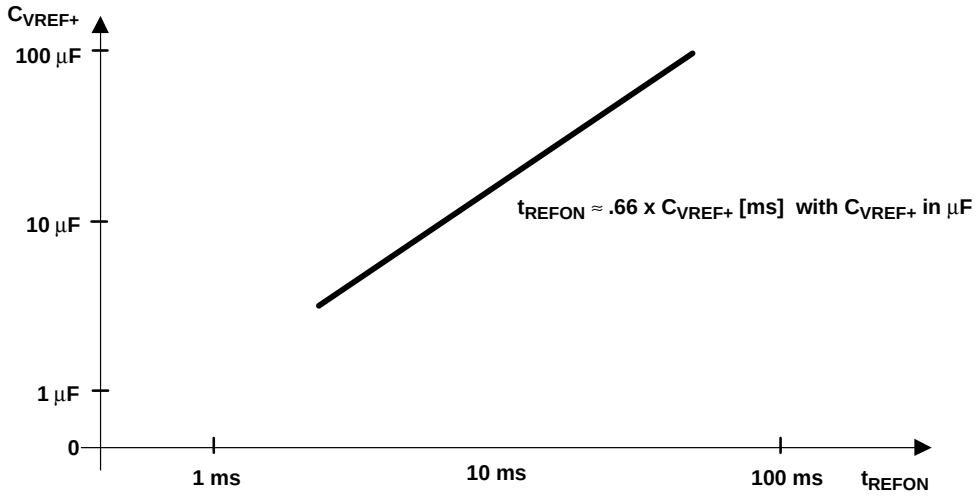


Figure 23. Typical Settling Time of Internal Reference t_{REFON} vs External Capacitor on V_{REF+}

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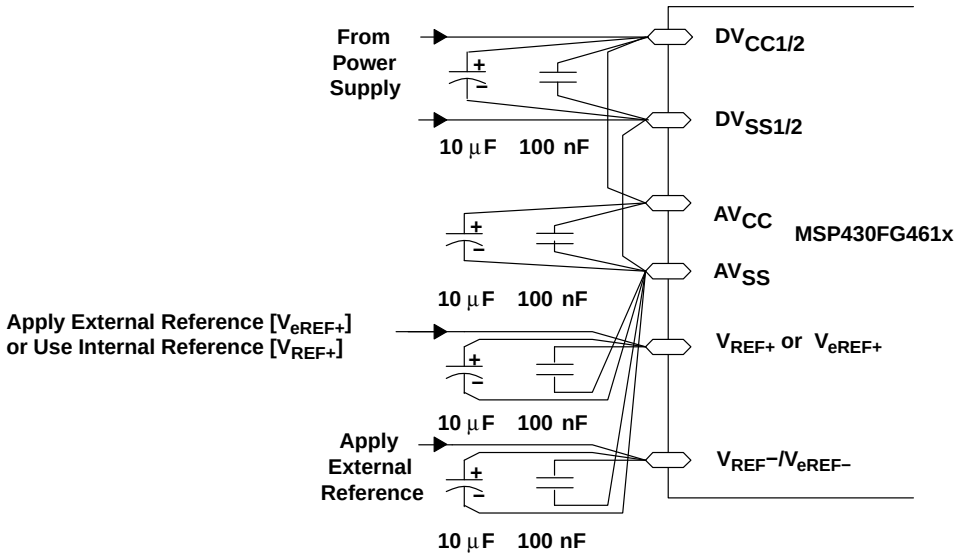


Figure 24. Supply Voltage and Reference Voltage Design V_{REF-}/V_{eREF-} External Supply

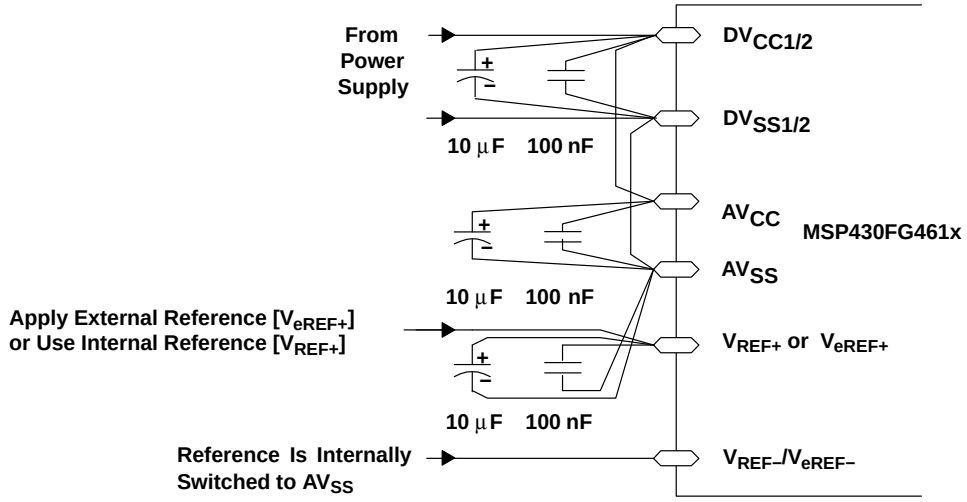


Figure 25. Supply Voltage and Reference Voltage Design V_{REF-}/V_{eREF-} = AV_{SS}, Internally Connected

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC, timing parameters

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$f_{ADC12CLK}$		For specified performance of ADC12 linearity parameters	V_{CC} = 2.2V/3 V	0.45	5	6.3	MHz
$f_{ADC12OSC}$	Internal ADC12 oscillator	ADC12DIV=0, $f_{ADC12CLK}=f_{ADC12OSC}$	V_{CC} = 2.2 V/ 3 V	3.7	5	6.3	MHz
$t_{CONVERT}$	Conversion time	$C_{VREF+} \geq 5$ µF, Internal oscillator, $f_{ADC12OSC}$ = 3.7 MHz to 6.3 MHz	V_{CC} = 2.2 V/ 3 V	2.06		3.51	µs
		External $f_{ADC12CLK}$ from ACLK, MCLK, or SMCLK, ADC12SSEL ≠ 0		13×ADC12DIV× $1/f_{ADC12CLK}$			µs
$t_{ADC12ON}$	Turn on settling time of the ADC	(see Note 1)				100	ns
t_{Sample}	Sampling time	R_S = 400 Ω, R_I = 1000 Ω, C_I = 30 pF, τ = [R_S + R_I] x C_I, (see Note 2)	V_{CC} = 3 V	1220			ns
			V_{CC} = 2.2 V	1400			

NOTES: 1. The condition is that the error in a conversion started after $t_{ADC12ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.

2. Approximately ten Tau (τ) are needed to get an error of less than ±0.5 LSB:
$t_{Sample} = \ln(2^{n+1}) \times (R_S + R_I) \times C_I + 800$ ns where n = ADC resolution = 12, R_S = external source resistance.

12-bit ADC, linearity parameters

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
E_I	Integral linearity error	1.4 V ≤ (V_{eREF+} − V_{REF-}/V_{eREF-}) min ≤ 1.6 V	V_{CC} = 2.2 V/3 V			±2	LSB
		1.6 V < (V_{eREF+} − V_{REF-}/V_{eREF-}) min ≤ [V_{AVCC}]				±1.7	
E_D	Differential linearity error	(V_{eREF+} − V_{REF-}/V_{eREF-})$_{min}$ ≤ (V_{eREF+} − V_{REF-}/V_{eREF-}), C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	V_{CC} = 2.2 V/3 V			±1	LSB
E_O	Offset error	(V_{eREF+} − V_{REF-}/V_{eREF-})$_{min}$ ≤ (V_{eREF+} − V_{REF-}/V_{eREF-}), Internal impedance of source R_S < 100 Ω, C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	V_{CC} = 2.2 V/3 V		±2	±4	LSB
E_G	Gain error	(V_{eREF+} − V_{REF-}/V_{eREF-})$_{min}$ ≤ (V_{eREF+} − V_{REF-}/V_{eREF-}), C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	V_{CC} = 2.2 V/3 V		±1.1	±2	LSB
E_T	Total unadjusted error	(V_{eREF+} − V_{REF-}/V_{eREF-})$_{min}$ ≤ (V_{eREF+} − V_{REF-}/V_{eREF-}), C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	V_{CC} = 2.2 V/3 V		±2	±5	LSB

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC, temperature sensor and built-in V_{MID}

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
I_{SENSOR}	Operating supply current into AV_{CC} terminal (see Note 1)	REFON = 0, INCH = 0Ah, ADC12ON=NA, T_A = 25°C	2.2 V		40	120	µA
			3 V		60	160	
V_{SENSOR}	(see Note 2)	ADC12ON = 1, INCH = 0Ah, T_A = 0°C	2.2 V/ 3 V		986		mV
TC_{SENSOR}		ADC12ON = 1, INCH = 0Ah	2.2 V/ 3 V		3.55±3%		mV/°C
$t_{SENSOR(sample)}$	Sample time required if channel 10 is selected (see Note 3)	ADC12ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB	2.2 V	30			µs
			3 V	30			
I_{VMID}	Current into divider at channel 11 (see Note 4)	ADC12ON = 1, INCH = 0Bh	2.2 V			NA	µA
			3 V			NA	
V_{MID}	AV_{CC} divider at channel 11	ADC12ON = 1, INCH = 0Bh, V_{MID} is ~0.5 x V_{AVCC}	2.2 V		1.1	1.1±0.04	V
			3 V		1.5	1.50±0.04	
$t_{VMID(sample)}$	Sample time required if channel 11 is selected (see Note 5)	ADC12ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB	2.2 V	1400			ns
			3 V	1220			

NOTES: 1. The sensor current I_{SENSOR} is consumed if (ADC12ON = 1 and REFON=1), or (ADC12ON=1 AND INCH=0Ah and sample signal is high). When REFON = 1, I_{SENSOR} is already included in I_{REF+}.
2. The temperature sensor offset can be as much as ±20°C. A single-point calibration is recommended in order to minimize the offset error of the built-in temperature sensor.
3. The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$
4. No additional current is needed. The V_{MID} is used during sampling.
5. The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.

12-bit DAC, supply specifications

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	AV_{CC} = DV_{CC}, AV_{SS} = DV_{SS} =0 V		2.20		3.60	V
I_{DD}	Supply current: Single DAC Channel (see Notes 1 and 2)	DAC12AMPx=2, DAC12IR=0, DAC12_xDAT=0800h	2.2 V/3 V		50	110	µA
		DAC12AMPx=2, DAC12IR=1, DAC12_xDAT=0800h , V_{eREF+}=V_{REF+}= AV_{CC}			50	110	
		DAC12AMPx=5, DAC12IR=1, DAC12_xDAT=0800h, V_{eREF+}=V_{REF+}= AV_{CC}			200	440	
		DAC12AMPx=7, DAC12IR=1, DAC12_xDAT=0800h, V_{eREF+}=V_{REF+}= AV_{CC}			700	1500	
PSRR	Power-supply rejection ratio (see Notes 3 and 4)	DAC12_xDAT = 800h, V_{REF} = 1.5 V, ΔAV_{CC} = 100mV	2.2 V		70		dB
		DAC12_xDAT = 800h, V_{REF} = 1.5 V or 2.5 V, ΔAV_{CC} = 100mV	3 V				

NOTES: 1. No load at the output pin, DAC12_0 or DAC12_1, assuming that the control bits for the shared pins are set properly.
2. Current into reference terminals not included. If DAC12IR = 1 current flows through the input divider; see Reference Input specifications.
3. PSRR = $20*\log\{\Delta AV_{CC}/\Delta V_{DAC12\_xOUT}\}$.
4. V_{REF} is applied externally. The internal reference is not used.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit DAC, linearity specifications (see Figure 26)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
Resolution		(12-bit Monotonic)		12			bits
INL	Integral nonlinearity (see Note 1)	V_{ref} = 1.5 V, DAC12AMPx = 7, DAC12IR = 1	2.2 V		±2.0	±8.0	LSB
		V_{ref} = 2.5 V, DAC12AMPx = 7, DAC12IR = 1	3 V				
DNL	Differential nonlinearity (see Note 1)	V_{ref} = 1.5 V, DAC12AMPx = 7, DAC12IR = 1	2.2 V		±0.4	±1.0	LSB
		V_{ref} = 2.5 V, DAC12AMPx = 7, DAC12IR = 1	3 V				
E_O	Offset voltage without calibration (see Notes 1, 2)	V_{ref} = 1.5 V, DAC12AMPx = 7, DAC12IR = 1	2.2 V			±21	mV
		V_{ref} = 2.5 V, DAC12AMPx = 7, DAC12IR = 1	3 V				
	Offset voltage with calibration (see Notes 1, 2)	V_{ref} = 1.5 V, DAC12AMPx = 7, DAC12IR = 1	2.2 V			±2.5	
		V_{ref} = 2.5 V, DAC12AMPx = 7, DAC12IR = 1	3 V				
$d_{E(O)}/d_T$	Offset error temperature coefficient (see Note 1)		2.2 V/3 V		±30		µV/°C
E_G	Gain error (see Note 1)	V_{REF} = 1.5 V	2.2 V			±3.50	% FSR
		V_{REF} = 2.5 V	3 V				
$d_{E(G)}/d_T$	Gain temperature coefficient (see Note 1)		2.2 V/3 V		10		ppm of FSR/°C
t_{Offset_Cal}	Time for offset calibration (see Note 3)	DAC12AMPx = 2	2.2 V/3 V			100	ms
		DAC12AMPx = 3,5				32	
		DAC12AMPx = 4,6,7				6	

NOTES: 1. Parameters calculated from the best-fit curve from 0x0A to 0xFFF. The best-fit curve method is used to deliver coefficients “a” and “b” of the first order equation: y = a + b*x. $V_{DAC12\_xOUT} = E_O + (1 + E_G) * (V_{eREF+}/4095) * DAC12\_xDAT$, DAC12IR = 1.
2. The offset calibration works on the output operational amplifier. Offset Calibration is triggered setting bit DAC12CALON
3. The offset calibration can be done if DAC12AMPx = {2, 3, 4, 5, 6, 7}. The output operational amplifier is switched off with DAC12AMPx = {0, 1}. It is recommended that the DAC12 module be configured prior to initiating calibration. Port activity during calibration may effect accuracy and is not recommended.

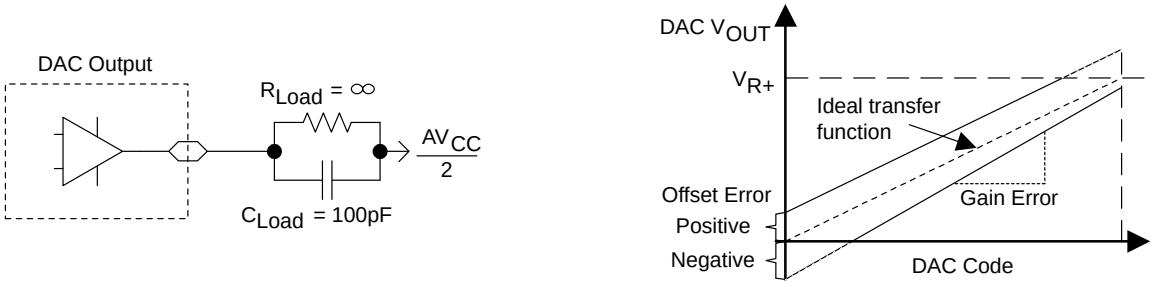
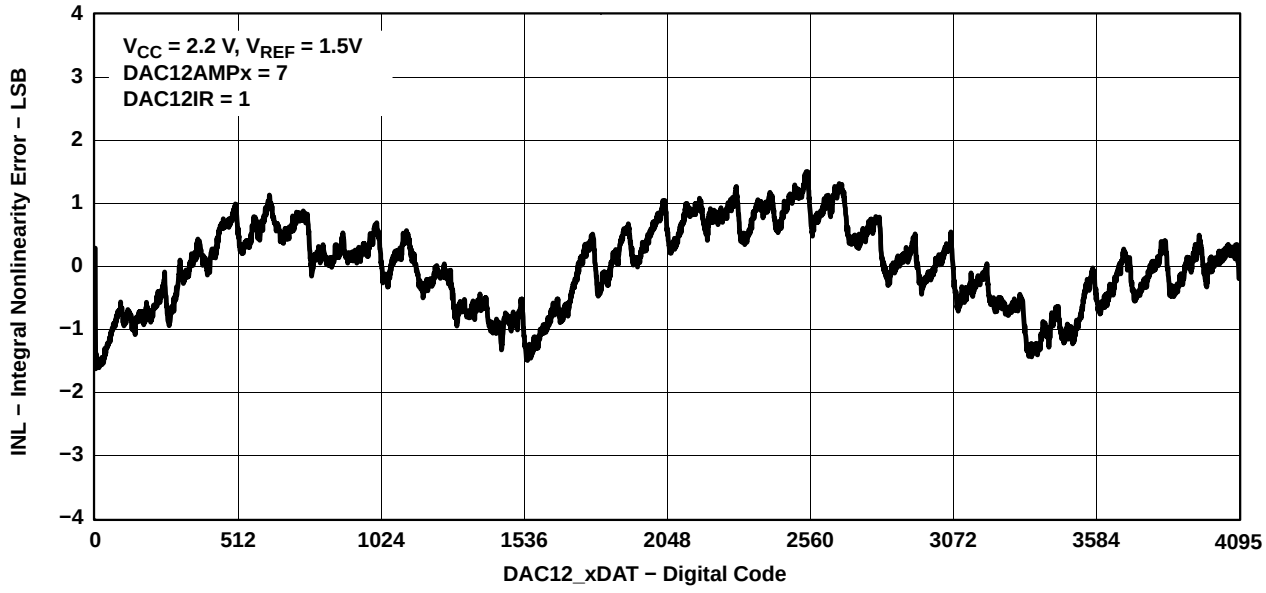


Figure 26. Linearity Test Load Conditions and Gain/Offset Definition

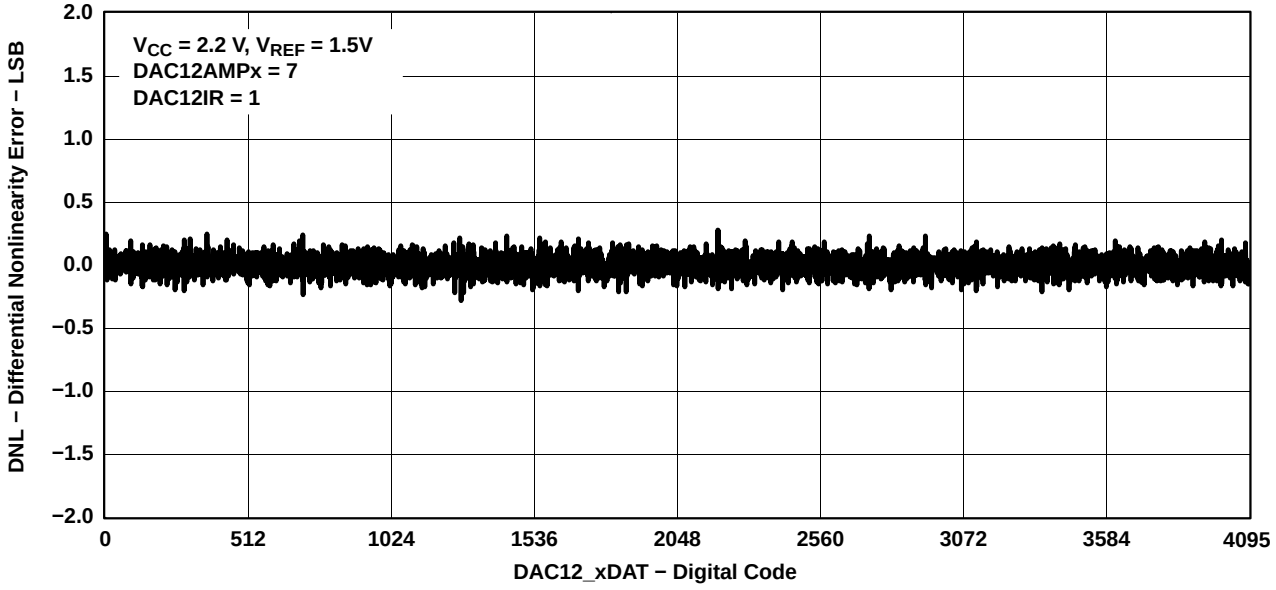
electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit DAC, linearity specifications (continued)

TYPICAL INL ERROR
vs
DIGITAL INPUT DATA



TYPICAL DNL ERROR
vs
DIGITAL INPUT DATA



electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit DAC, output specifications

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_O	Output voltage range (see Note 1, Figure 29)	No Load, $Ve_{REF+} = AV_{CC}$, DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7	2.2 V/3 V	0		0.005	V
		No Load, $Ve_{REF+} = AV_{CC}$, DAC12_xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = 7		AV_{CC}−0.05		AV_{CC}	
		R_{Load}= 3 kΩ, $Ve_{REF+} = AV_{CC}$, DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7		0		0.1	
		R_{Load}= 3 kΩ, $Ve_{REF+} = AV_{CC}$, DAC12_xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = 7		AV_{CC}−0.13		AV_{CC}	
$C_{L(DAC12)}$	Max DAC12 load capacitance		2.2V/3V			100	pF
$I_{L(DAC12)}$	Max DAC12 load current		2.2V	−0.5		+0.5	mA
			3V	−1.0		+1.0	
$R_{O/P(DAC12)}$	Output resistance (see Figure 29)	R_{Load}= 3 kΩ, $V_{O/P(DAC12)}$ < 0.3 V, DAC12AMPx = 2, DAC12_xDAT = 0h	2.2 V/3 V		150	250	Ω
		R_{Load}= 3 kΩ, $V_{O/P(DAC12)} > AV_{CC}$−0.3 V DAC12_xDAT = 0FFFh			150	250	
		R_{Load}= 3 kΩ, 0.3V ≤ $V_{O/P(DAC12)}$ ≤ AV_{CC} − 0.3V			1	4	

NOTE 1: Data is valid after the offset calibration of the output amplifier.

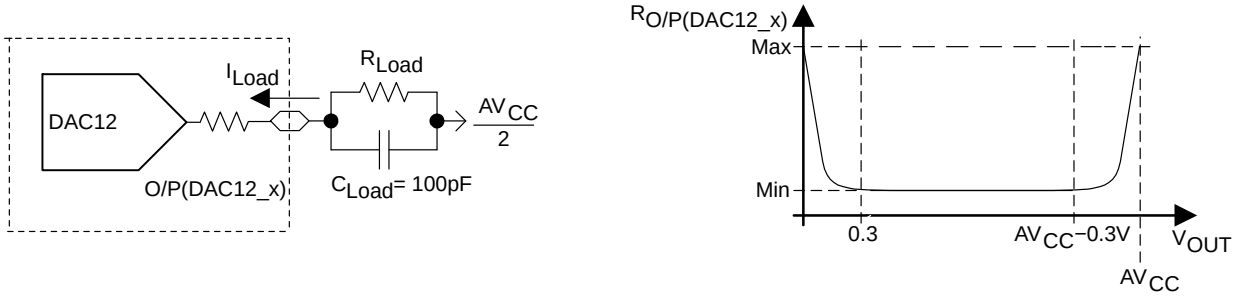


Figure 29. DAC12_x Output Resistance Tests

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

12-bit DAC, reference input specifications

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
Ve_{REF+}	Reference input voltage range	DAC12IR=0 (see Notes 1 and 2)	2.2 V/3 V		$AV_{CC}/3$	AV_{CC}+0.2	V
		DAC12IR=1 (see Notes 3 and 4)			AVcc	AVcc+0.2	
$Ri_{(VREF+)}$, $Ri_{(VeREF+)}$	Reference input resistance	DAC12_0 IR=DAC12_1 IR =0	2.2 V/3 V	20			MΩ
		DAC12_0 IR=1, DAC12_1 IR = 0		40	48	56	kΩ
		DAC12_0 IR=0, DAC12_1 IR = 1					
		DAC12_0 IR=DAC12_1 IR =1, DAC12_0 SREFx = DAC12_1 SREFx (see Note 5)		20	24	28	

NOTES: 1. For a full-scale output, the reference input voltage can be as high as 1/3 of the maximum output voltage swing (AV_{CC}).
2. The maximum voltage applied at reference input voltage terminal $Ve_{REF+} = [AV_{CC} − V_{E(O)}] / [3*(1 + E_G)]$.
3. For a full-scale output, the reference input voltage can be as high as the maximum output voltage swing (AV_{CC}).
4. The maximum voltage applied at reference input voltage terminal $Ve_{REF+} = [AV_{CC} − V_{E(O)}] / (1 + E_G)$.
5. When DAC12IR = 1 and DAC12SREFx = 0 or 1 for both channels, the reference input resistive dividers for each DAC are in parallel reducing the reference input resistance.

12-bit DAC, dynamic specifications; $V_{ref} = V_{CC}$, DAC12IR = 1 (see Figure 30 and Figure 31)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
t_{ON}	DAC12 on-time	DAC12_xDAT = 800h, $Error_{V(O)}$ < ±0.5 LSB (see Note 1,Figure 30)	DAC12AMPx = 0 → {2, 3, 4}	2.2 V/3 V		60	120	µs
			DAC12AMPx = 0 → {5, 6}			15	30	
			DAC12AMPx = 0 → 7			6	12	
$t_{S(FS)}$	Settling time, full-scale	DAC12_xDAT = 80h→ F7Fh→ 80h	DAC12AMPx = 2	2.2 V/3 V		100	200	µs
			DAC12AMPx = 3,5			40	80	
			DAC12AMPx = 4,6,7			15	30	
$t_{S(C-C)}$	Settling time, code to code	DAC12_xDAT = 3F8h→ 408h→ 3F8h BF8h→ C08h→ BF8h	DAC12AMPx = 2	2.2 V/3 V		5		µs
			DAC12AMPx = 3,5			2		
			DAC12AMPx = 4,6,7			1		
SR	Slew rate	DAC12_xDAT = 80h→ F7Fh→ 80h (see Note 2)	DAC12AMPx = 2	2.2 V/3 V	0.05	0.12		V/µs
			DAC12AMPx = 3,5		0.35	0.7		
			DAC12AMPx = 4,6,7		1.5	2.7		
Glitch energy, full-scale		DAC12_xDAT = 80h→ F7Fh→ 80h	DAC12AMPx = 2	2.2 V/3 V		600		nV-s
			DAC12AMPx = 3,5			150		
			DAC12AMPx = 4,6,7			30		

NOTES: 1. R_{Load} and C_{Load} connected to AV_{SS} (not $AV_{CC}/2$) in Figure 30.
2. Slew rate applies to output voltage steps >= 200mV.

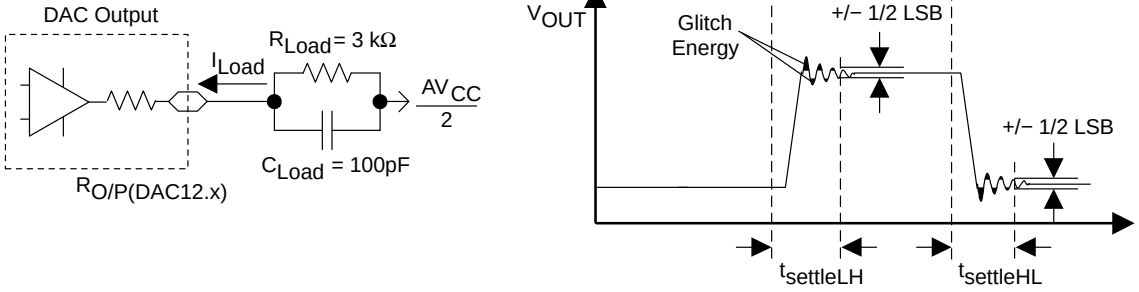


Figure 30. Settling Time and Glitch Energy Testing

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

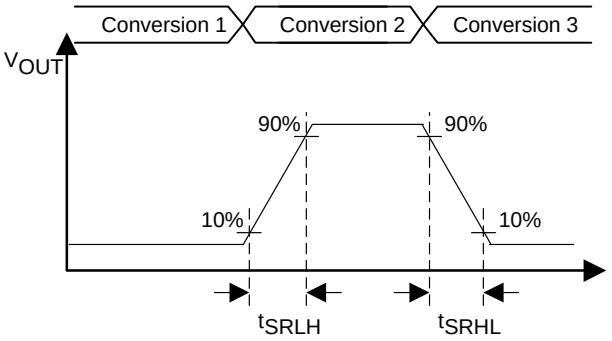


Figure 31. Slew Rate Testing

12-bit DAC, dynamic specifications continued (T_A = 25°C unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
BW_{-3dB} 3-dB bandwidth, V_{DC}=1.5V, V_{AC}=0.1V_{PP} (see Figure 32)	DAC12AMPx = {2, 3, 4}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h	2.2 V/3 V	40			kHz
	DAC12AMPx = {5, 6}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h		180			
	DAC12AMPx = 7, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h		550			
Channel-to-channel crosstalk (see Note 1 and Figure 33)	DAC12_0DAT = 800h, No Load, DAC12_1DAT = 80h<−>F7Fh, R_{Load} = 3kΩ f_{DAC12_1OUT} = 10kHz @ 50/50 duty cycle	2.2 V/3 V		−80		dB
	DAC12_0DAT = 80h<−>F7Fh, R_{Load} = 3kΩ, DAC12_1DAT = 800h, No Load, f_{DAC12_0OUT} = 10kHz @ 50/50 duty cycle			−80		

NOTE 1: R_{LOAD} = 3 kΩ, C_{LOAD} = 100 pF

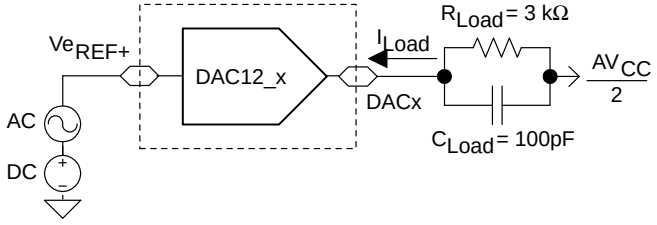


Figure 32. Test Conditions for 3-dB Bandwidth Specification

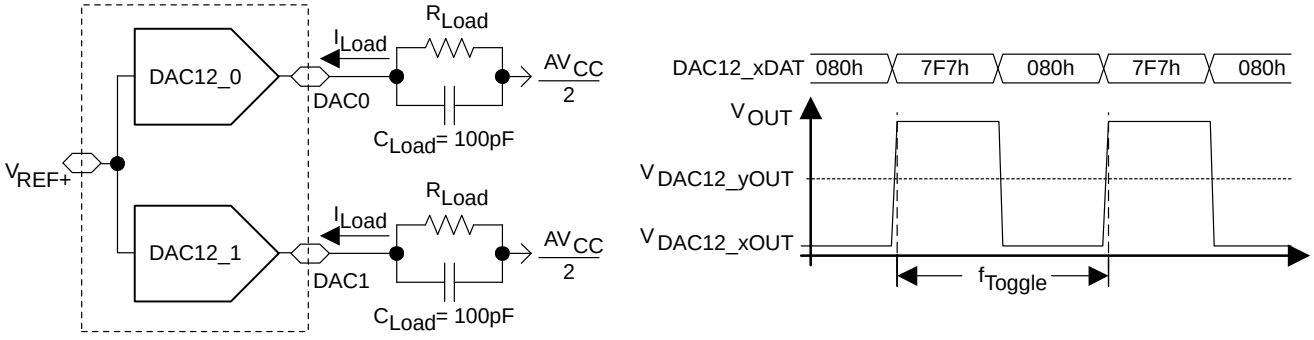


Figure 33. Crosstalk Test Conditions

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

operational amplifier OA, supply specifications

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		—	2.2		3.6	V
I_{CC}	Supply current (see Note 1)	Fast Mode, OARRIP = 1 (rail-to-rail mode off)	2.2 V/3 V		180	290	μA
		Medium Mode, OARRIP = 1 (rail-to-rail mode off)			110	190	
		Slow Mode, OARRIP = 1 (rail-to-rail mode off)			50	80	
		Fast Mode, OARRIP = 0 (rail-to-rail mode on)			300	490	
		Medium Mode, OARRIP = 0 (rail-to-rail mode on)			190	350	
		Slow Mode, OARRIP = 0 (rail-to-rail mode on)			90	190	
PSRR	Power supply rejection ratio	Non-inverting	2.2 V/3 V		70		dB

NOTE 1: P6SEL.x = 1 for each corresponding pin when used in OA input or OA output mode.

operational amplifier OA, input/output specifications

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
$V_{I/P}$	Voltage supply, I/P	OARRIP = 1 (rail-to-rail mode off)		—	−0.1		V_{CC}−1.2	V
		OARRIP = 0 (rail-to-rail mode on)			−0.1		V_{CC}+0.1	
I_{Ikg}	Input leakage current, I/P (see Notes 1 and 2)	T_A = −40 to +55°C		—	−5	±0.5	5	nA
		T_A = +55 to +85°C			−20	±5	20	
V_n	Voltage noise density, I/P	Fast Mode	$f_{V(I/P)}$ = 1 kHz	—		50		nV/√Hz
		Medium Mode				80		
		Slow Mode				140		
		Fast Mode	$f_{V(I/P)}$ = 10 kHz			30		
		Medium Mode				50		
		Slow Mode				65		
V_{IO}	Offset voltage, I/P			2.2 V/3 V			±10	mV
	Offset temperature drift, I/P	see Note 3		2.2 V/3 V		±10		µV/°C
	Offset voltage drift with supply, I/P	0.3V ≤ V_{IN} ≤ V_{CC}−0.3V ΔV_{CC}≤ ± 10%, T_A = 25°C		2.2 V/3 V			±1.5	mV/V
V_{OH}	High-level output voltage, O/P	Fast Mode, I_{SOURCE} ≤ −500µA		2.2 V	V_{CC}−0.2		V_{CC}	V
		Slow Mode,I_{SOURCE} ≤ −150µA		3 V	V_{CC}−0.1		V_{CC}	
V_{OL}	Low-level output voltage, O/P	Fast Mode, I_{SOURCE} ≤ +500µA		2.2 V	V_{SS}		0.2	V
		Slow Mode,I_{SOURCE} ≤ +150µA		3 V	V_{SS}		0.1	
$R_{O/P (OAx)}$	Output Resistance (see Figure 34 and Note 4)	R_{Load}= 3 kΩ, C_{Load} = 50pF, OARRIP = 0 (rail-to-rail mode on), $V_{O/P(OAx)}$ < 0.2 V		2.2 V/3 V		150	250	Ω
		R_{Load}= 3 kΩ, C_{Load} = 50pF, OARRIP = 0 (rail-to-rail mode on), $V_{O/P(OAx)}$ > AV_{CC} − 0.2 V				150	250	
		R_{Load}= 3 kΩ, C_{Load} = 50pF, OARRIP = 0 (rail-to-rail mode on), 0.2 V ≤ $V_{O/P(OAx)}$ ≤ AV_{CC} − 0.2 V				0.1	4	
CMRR	Common-mode rejection ratio	Non-inverting		2.2 V/3 V		70		dB

NOTES: 1. ESD damage can degrade input current leakage.
2. The input bias current is overridden by the input leakage current.
3. Calculated using the box method.
4. Specification valid for voltage-follower OAx configuration.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

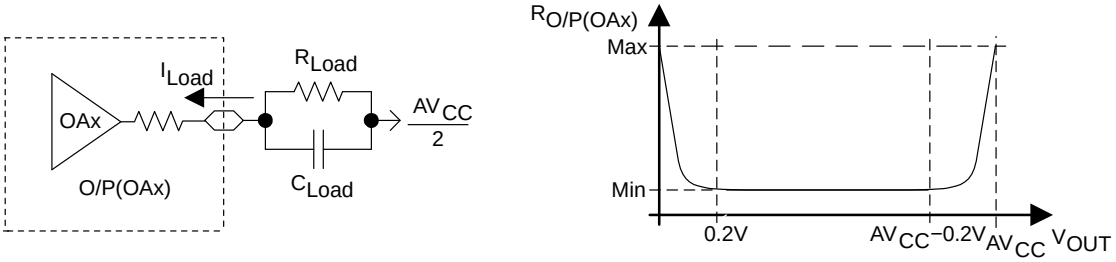


Figure 34. OAx Output Resistance Tests

operational amplifier OA, dynamic specifications

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
SR	Slew rate	Fast Mode	—		1.2		V/µs
		Medium Mode	—		0.8		
		Slow Mode	—		0.3		
	Open-loop voltage gain		—		100		dB
ϕ_m	Phase margin	C_L = 50 pF	—		60		deg
	Gain margin	C_L = 50 pF	—		20		dB
GBW	Gain-bandwidth product (see Figure 35 and Figure 36)	Non−inverting, Fast Mode, R_L = 47kΩ, C_L = 50pF	2.2 V/3 V		2.2		MHz
		Non−inverting, Medium Mode, R_L =300kΩ, C_L = 50pF			1.4		
		Non−inverting, Slow Mode, R_L =300kΩ, C_L = 50pF			0.5		
$t_{en(on)}$	Enable time on	t_{on}, non-inverting, Gain = 1	2.2 V/3 V		10	20	µs
$t_{en(off)}$	Enable time off		2.2 V/3 V			1	µs

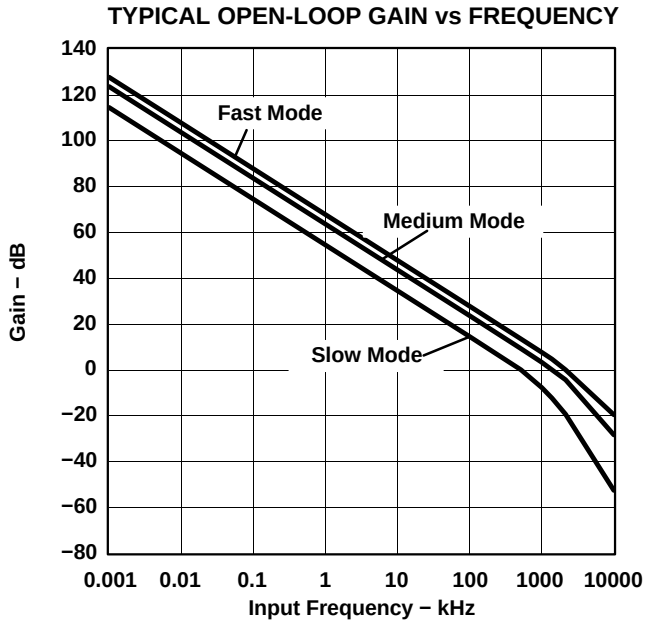


Figure 35

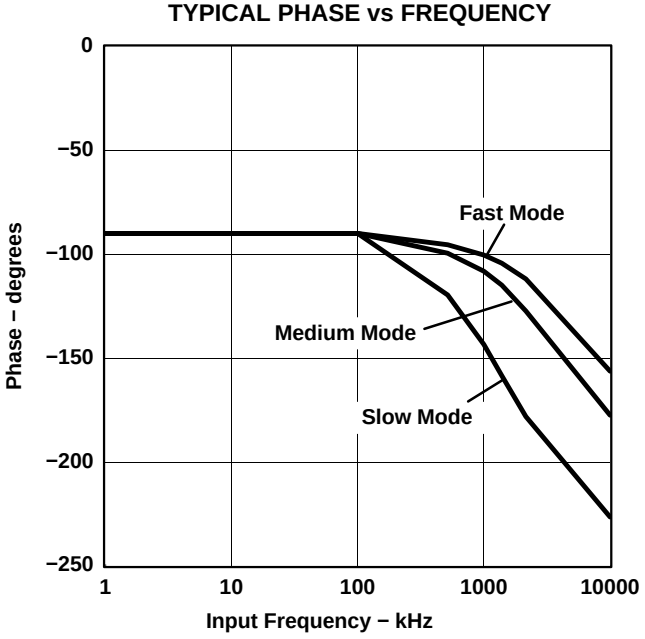


Figure 36

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

operational amplifier OA feedback network, noninverting amplifier mode (OAFCx = 4)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
G	Gain	OAFBRx = 0	2.2 V/ 3 V	0.996	1.00	1.002	
		OAFBRx = 1		1.329	1.334	1.340	
		OAFBRx = 2		1.987	2.001	2.016	
		OAFBRx = 3		2.64	2.667	2.70	
		OAFBRx = 4		3.93	4.00	4.06	
		OAFBRx = 5		5.22	5.33	5.43	
		OAFBRx = 6		7.76	7.97	8.18	
		OAFBRx = 7		15.0	15.8	16.6	
THD	Total harmonic distortion/ nonlinearity	All gains	2.2 V		−60		dB
			3 V		−70		
t_{Settle}	Settling time (see Note 1)	All power modes	2.2 V/3 V		7	12	µs

NOTES: 1. The settling time specifies the time until an ADC result is stable. This includes the minimum required sampling time of the ADC. The settling time of the amplifier itself might be faster.

operational amplifier OA feedback network, inverting amplifier mode (OAFCx = 6) (see Note 1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
G	Gain	OAFBRx = 1	2.2 V/ 3 V	−0.371	−0.335	−0.298	
		OAFBRx = 2		−1.031	−1.002	−0.972	
		OAFBRx = 3		−1.727	−1.668	−1.609	
		OAFBRx = 4		−3.142	−3.00	−2.856	
		OAFBRx = 5		−4.581	−4.33	−4.073	
		OAFBRx = 6		−7.529	−6.97	−6.379	
		OAFBRx = 7		−17.040	−14.8	−12.279	
THD	Total harmonic distortion/ nonlinearity	All gains	2.2 V		−60		dB
			3 V		−70		
t_{Settle}	Settling time (see Note 2)	All power modes	2.2 V/3 V		7	12	µs

NOTES: 1. This includes the 2 OA configuration “inverting amplifier with input buffer”. Both OA needs to be set to the same power mode OAPMx.
2. The settling time specifies the time until an ADC result is stable. This includes the minimum required sampling time of the ADC. The settling time of the amplifier itself might be faster.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

flash memory (MSP430FG461x devices only)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(PGM/ERASE)}$	Program and Erase supply voltage			2.7		3.6	V
f_{FTG}	Flash Timing Generator frequency			257		476	kHz
I_{PGM}	Supply current from DV_{CC} during program		2.7 V/ 3.6 V		3	5	mA
I_{ERASE}	Supply current from DV_{CC} during erase	See Note 3	2.7 V/ 3.6 V		3	7	mA
$I_{GMERASE}$	Supply current from DV_{CC} during global mass erase	See Note 4	2.7 V/ 3.6 V		6	14	mA
t_{CPT}	Cumulative program time	See Note 1	2.7 V/ 3.6 V			10	ms
$t_{CMErase}$	Cumulative mass erase time		2.7 V/ 3.6 V	20			ms
	Program/Erase endurance			10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C		100			years
t_{Word}	Word or byte program time	See Note 2			30		t_{FTG}
$t_{Block, 0}$	Block program time for 1st byte or word				25		
$t_{Block, 1-63}$	Block program time for each additional byte or word				18		
$t_{Block, End}$	Block program end-sequence wait time				6		
$t_{Mass Erase}$	Mass erase time				10593		
$t_{Global Mass Erase}$	Global mass erase time				10593		
$t_{Seg Erase}$	Segment erase time				4819		

NOTES: 1. The cumulative program time must not be exceeded during a block-write operation. This parameter is only relevant if the block write feature is used.
2. These values are hardwired into the Flash Controller's state machine ($t_{FTG} = 1/f_{FTG}$).
3. Lower 64-KB or upper 64-KB Flash memory erased.
4. All Flash memory erased.

JTAG interface

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TCK}	TCK input frequency	See Note 1	2.2 V	0		5	MHz
			3 V	0		10	MHz
$R_{Internal}$	Internal pull-up resistance on TMS, TCK, TDI/TCLK	See Note 2	2.2 V/ 3 V	25	60	90	kΩ

NOTES: 1. f_{TCK} may be restricted to meet the timing requirements of the module selected.
2. TMS, TDI/TCLK, and TCK pull-up resistors are implemented in all versions.

JTAG fuse (see Note 1)

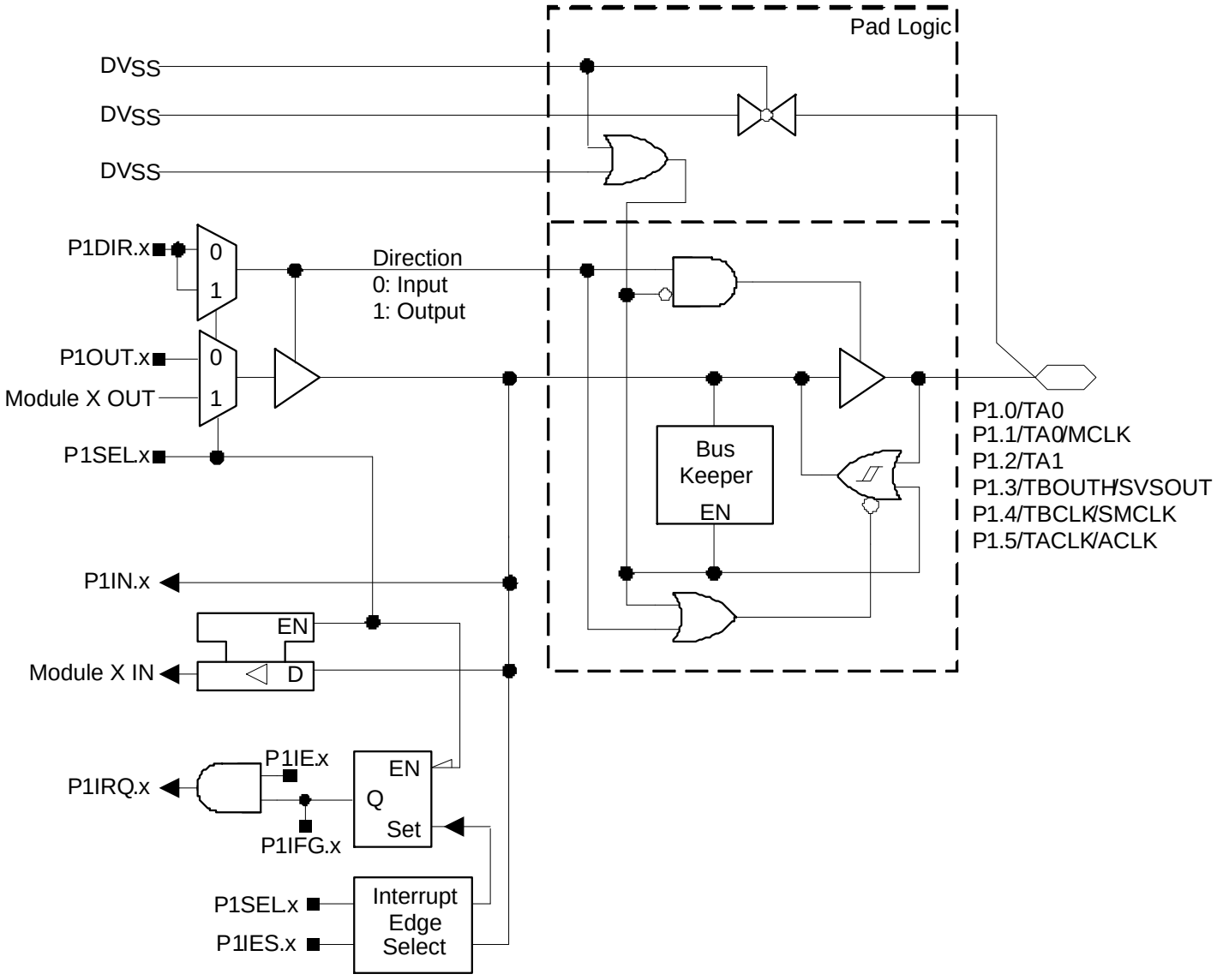
PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(FB)}$	Supply voltage during fuse-blow condition	T_A = 25°C		2.5			V
V_{FB}	Voltage level on TDI/TCLK for fuse-blow: F versions			6		7	V
I_{FB}	Supply current into TDI/TCLK during fuse blow					100	mA
t_{FB}	Time to blow fuse					1	ms

NOTE 1: Once the fuse is blown, no further access to the MSP430 JTAG/Test and emulation features is possible. The JTAG block is switched to bypass mode.

APPLICATION INFORMATION

input/output schematics

Port P1, P1.0 to P1.5, input/output with Schmitt trigger

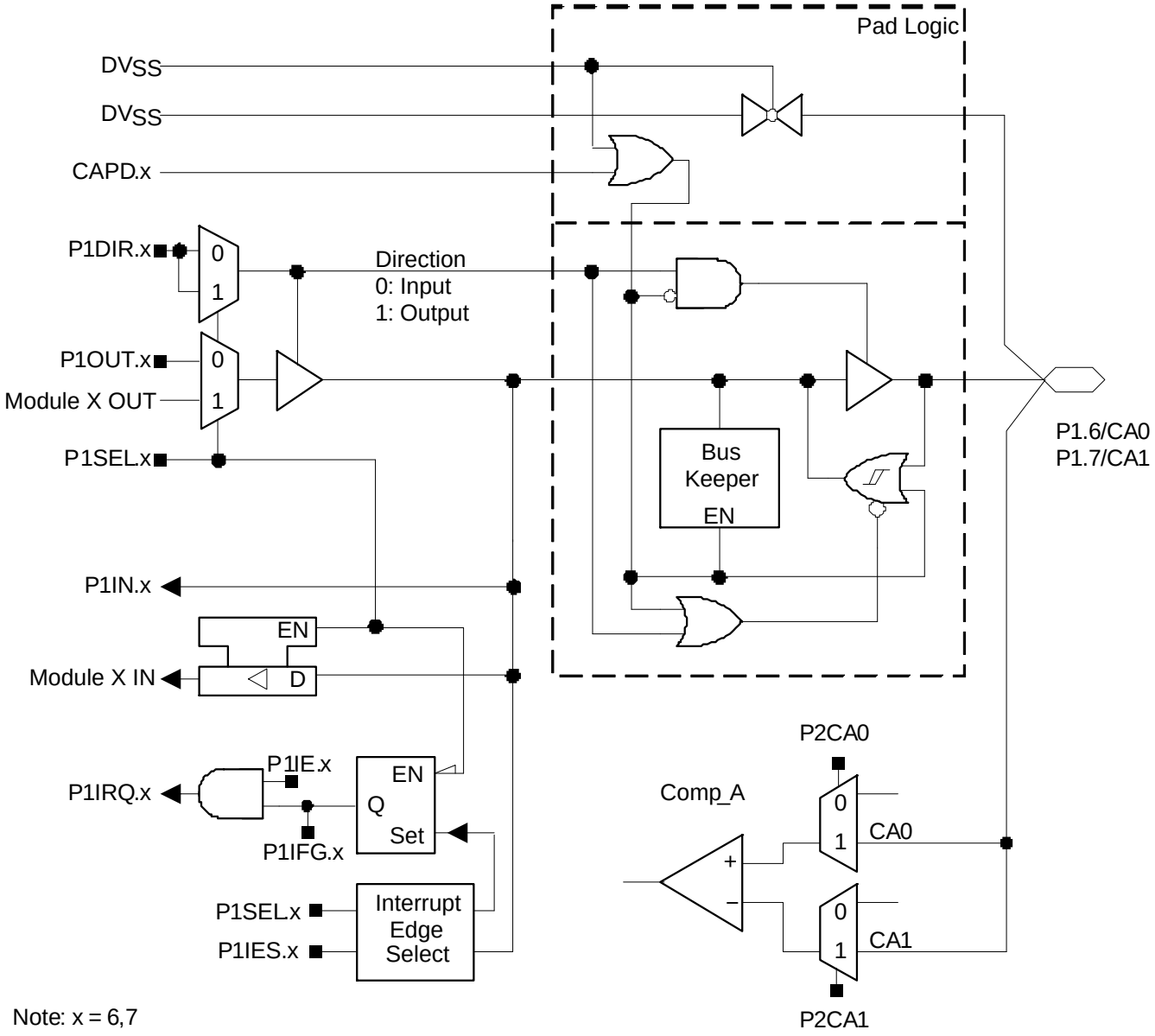


Note: x = 0,1,2,3,4,5

Port P1 (P1.0 to P1.5) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P1DIR.x	P1SEL.x
P1.0/TA0	0	P1.0 (I/O)	I: 0; O: 1	0
		Timer_A3.CCI0A	0	1
		Timer_A3.TA0	1	1
P1.1/TA0/MCLK	1	P1.1 (I/O)	I: 0; O: 1	0
		Timer_A3.CCI0B	0	1
		MCLK	1	1
P1.2/TA1	2	P1.2 (I/O)	I: 0; O: 1	0
		Timer_A3.CCI1A	0	1
		Timer_A3.TA1	1	1
P1.3/TBOUTH/SVSOUT	3	P1.3 (I/O)	I: 0; O: 1	0
		Timer_B7.TBOUTH	0	1
		SVSOUT	1	1
P1.4/TBCLK/SMCLK	4	P1.4 (I/O)	I: 0; O: 1	0
		Timer_B7.TBCLK	0	1
		SMCLK	1	1
P1.5/TACLK/ACLK	5	P1.5 (I/O)	I: 0; O: 1	0
		Timer_A3.TACLK	0	1
		ACLK	1	1

Port P1, P1.6, P1.7, input/output with Schmitt trigger



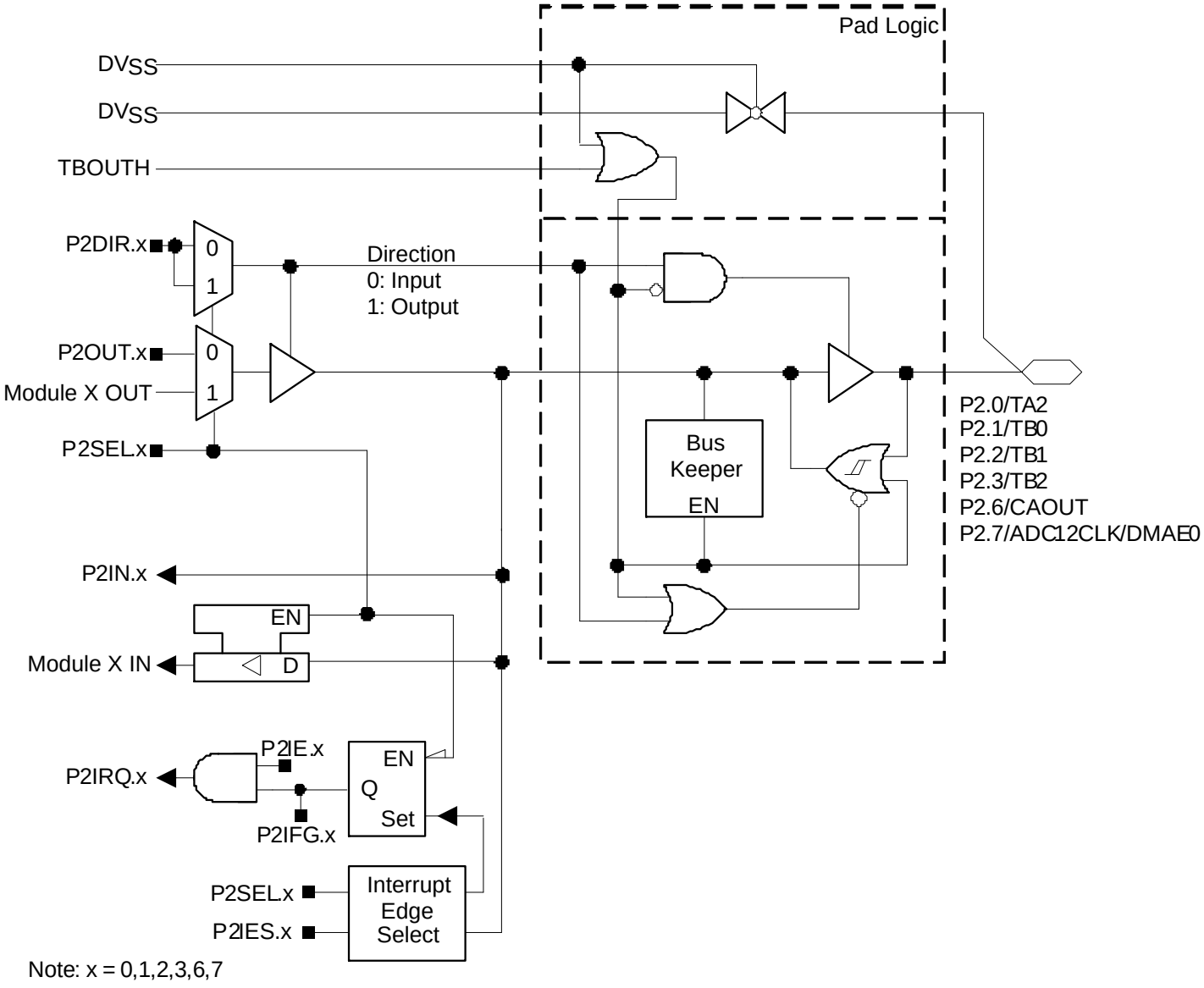
Note: x = 6,7

Port P1 (P1.6 and P1.7) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			CAPD.x	P1DIR.x	P1SEL.x
P1.6/CA0	6	P1.6 (I/O)	0	I: 0; O: 1	0
		CA0	1	X	X
P1.7/CA1	7	P1.7 (I/O)	0	I: 0; O: 1	0
		CA1	1	X	X

NOTE 1: X: Don't care

port P2, P2.0 to P2.3, P2.6 to P2.7, input/output with Schmitt trigger



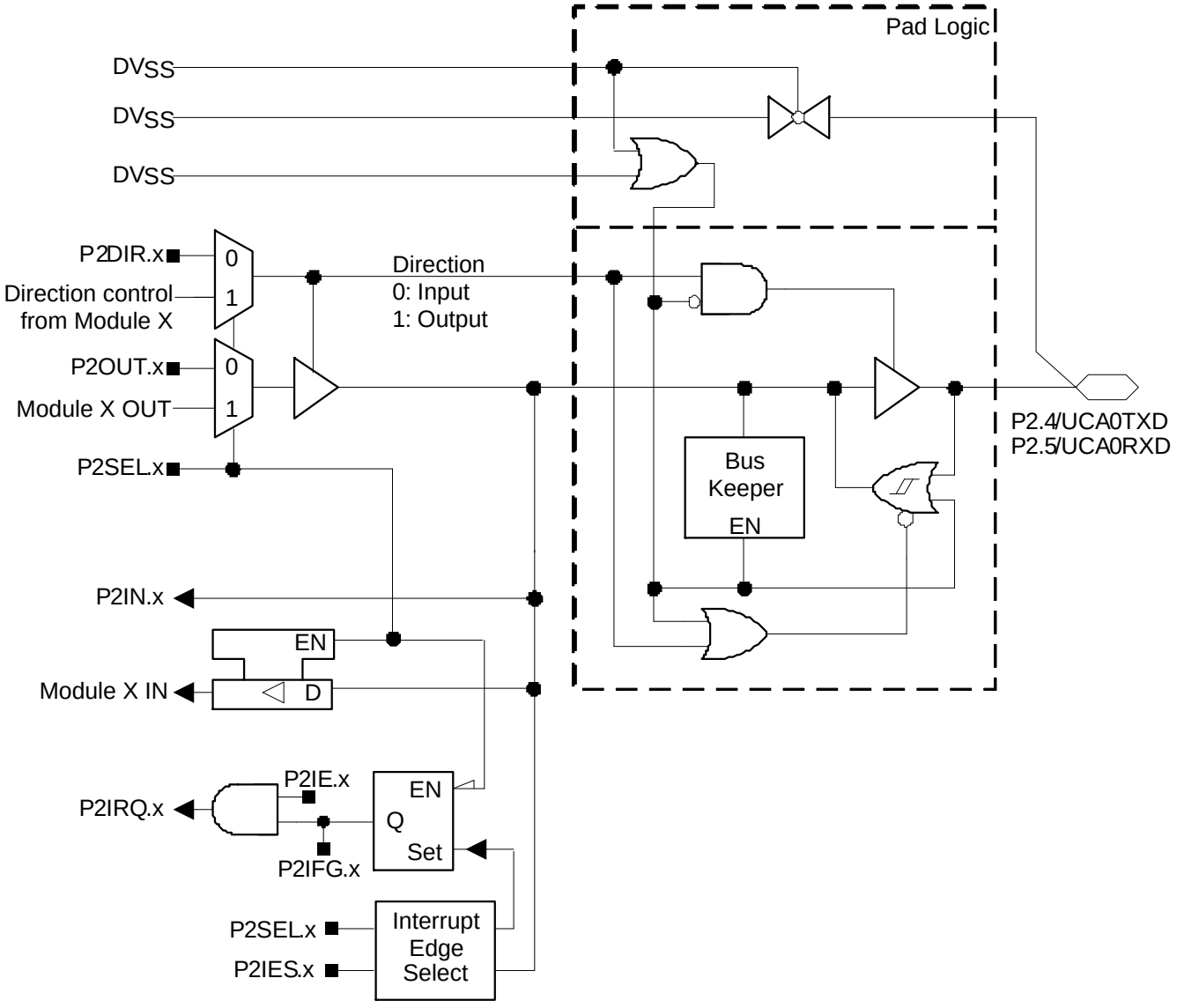
Note: x = 0,1,2,3,6,7

Port P2 (P2.0, P2.1, P2.2, P2.3, P2.6 and P2.7) pin functions

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P2DIR.x	P2SEL.x
P2.0/TA2	0	P2.0 (I/O)	I: 0; O: 1	0
		Timer_A3.CCI2A	0	1
		Timer_A3.TA2	1	1
P2.1/TB0	1	P2.1 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI0A and Timer_B7.CCI0B	0	1
		Timer_B7.TB0 (see Note 1)	1	1
P2.2/TB1	2	P2.2 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI1A and Timer_B7.CCI1B	0	1
		Timer_B7.TB1 (see Note 1)	1	1
P2.3/TB3	3	P2.3 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI2A and Timer_B7.CCI2B	0	1
		Timer_B7.TB3 (see Note 1)	1	1
P2.6/CAOUT	6	P2.6 (I/O)	I: 0; O: 1	0
		CAOUT	1	1
P2.7/ADC12CLK/DMAE0	7	P2.7 (I/O)	I: 0; O: 1	0
		ADC12CLK	1	1
		DMAE0	0	1

NOTE 1: Setting TBOUTH causes all Timer_B outputs to be set to high impedance.

port P2, P2.4 to P2.5, input/output with Schmitt trigger



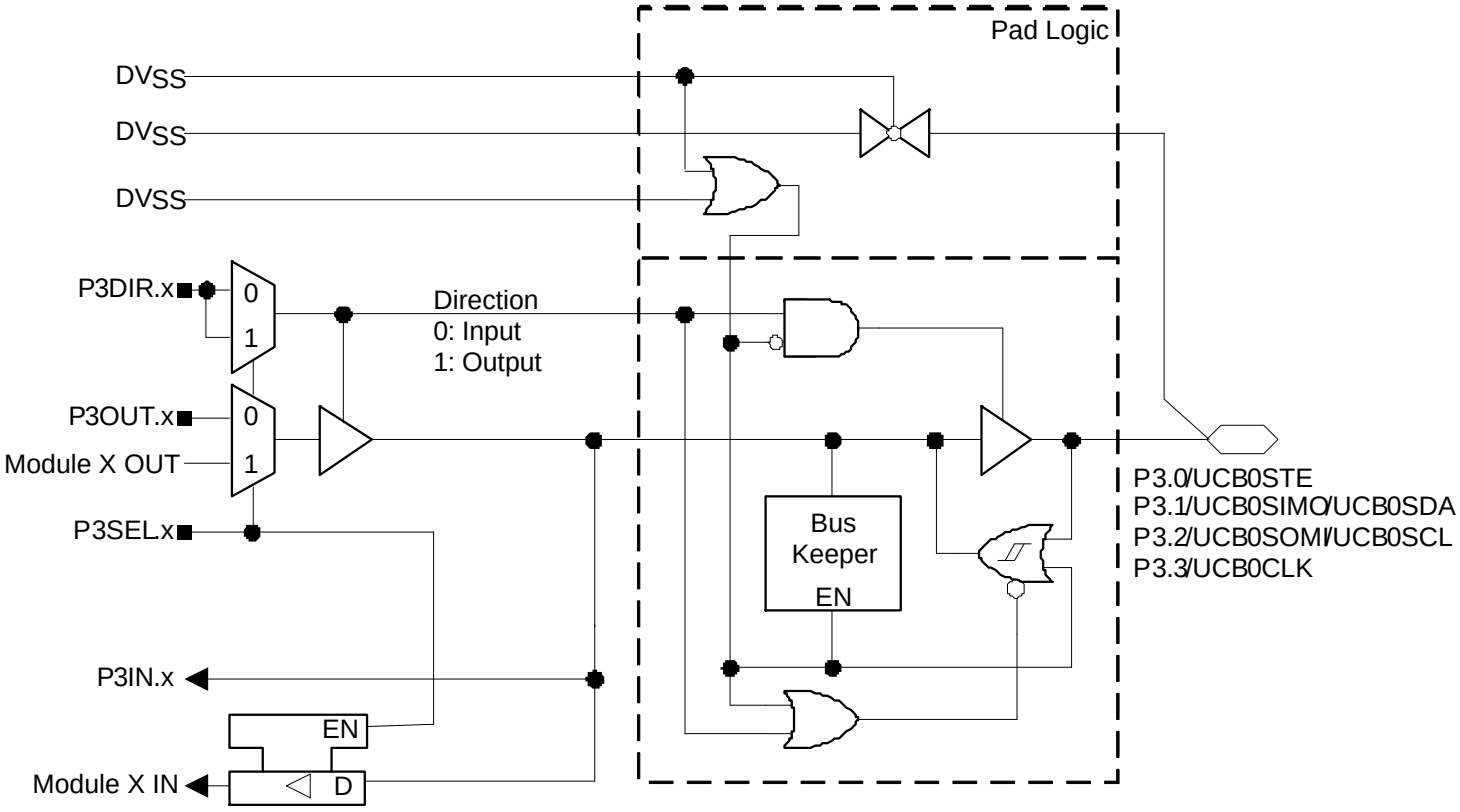
Note: x = 4,5

Port P2 (P2.4 and P2.5) pin functions

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P2DIR.x	P2SEL.x
P2.4/UCA0TXD	4	P2.4 (I/O)	I: 0; O: 1	0
		USCI_A0.UCA0TXD (see Note 1, 2)	X	1
P2.5/UCA0RXD	5	P2.5 (I/O)	I: 0; O: 1	0
		USCI_A0.UCA0RXD (see Note 1, 2)	X	1

NOTES: 1. X: Don't care
2. When in USCI mode, P2.4 is set to output, P2.5 is set to input.

port P3, P3.0 to P3.3, input/output with Schmitt trigger



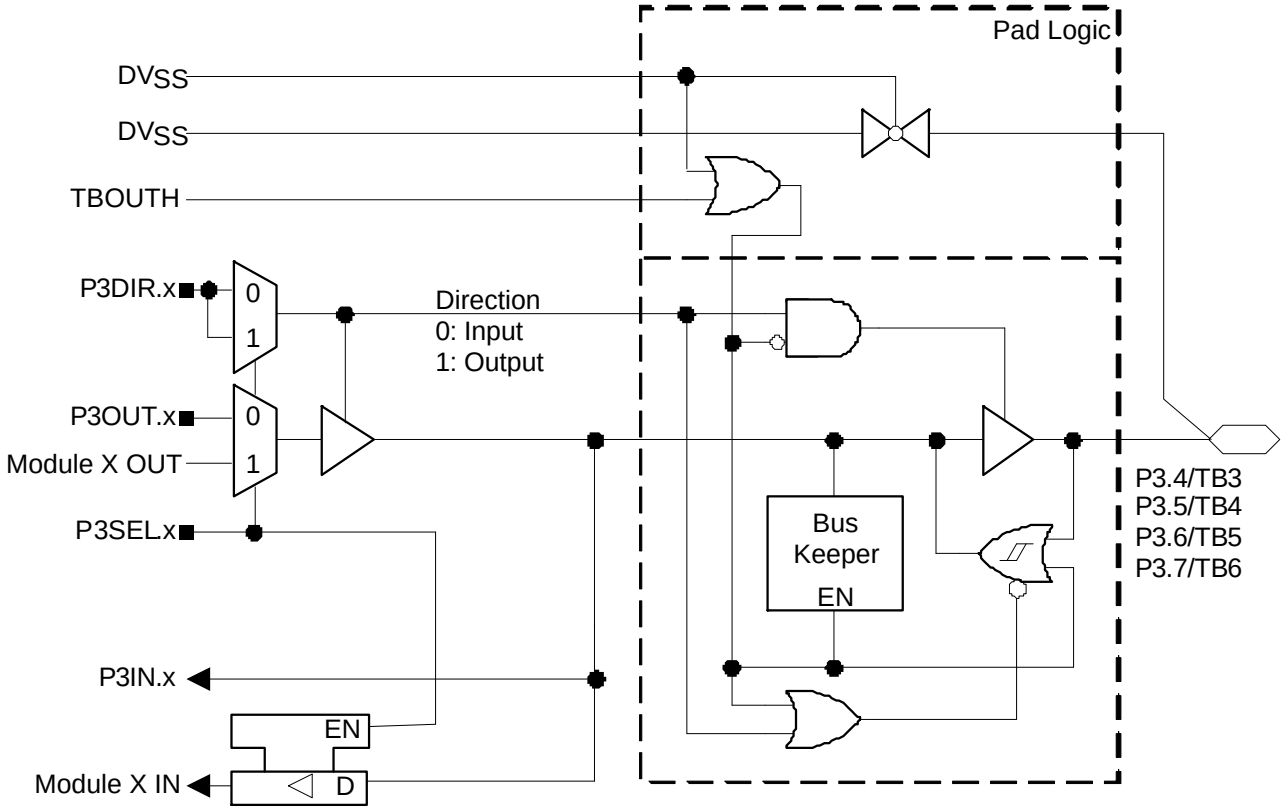
Note: x = 0,1,2,3

Port P3 (P3.0 to P3.3) pin functions

PIN NAME (P3.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P3DIR.x	P3SEL.x
P3.0/UCB0STE	0	P3.0 (I/O)	I: 0; O: 1	0
		UCB0STE (see Notes 1, 2)	X	1
P3.1/UCB0SIMO/ UCB0SDA	1	P3.1 (I/O)	I: 0; O: 1	0
		UCB0SIMO/UCB0SDA (see Notes 1, 2, 3)	X	1
P3.2/UCB0SOMI/ UCB0SCL	2	P3.2 (I/O)	I: 0; O: 1	0
		UCB0SOMI/UCB0SCL (see Notes 1, 2, 3)	X	1
P3.3/UCB0CLK	3	P3.3 (I/O)	I: 0; O: 1	0
		UCB0CLK (see Notes 1, 2)	X	1

NOTES: 1. X: Don't care
2. The pin direction is controlled by the USCI module.
3. In case the I2C functionality is selected the output drives only the logical 0 to V_{SS} level.

port P3, P3.4 to P3.7, input/output with Schmitt trigger



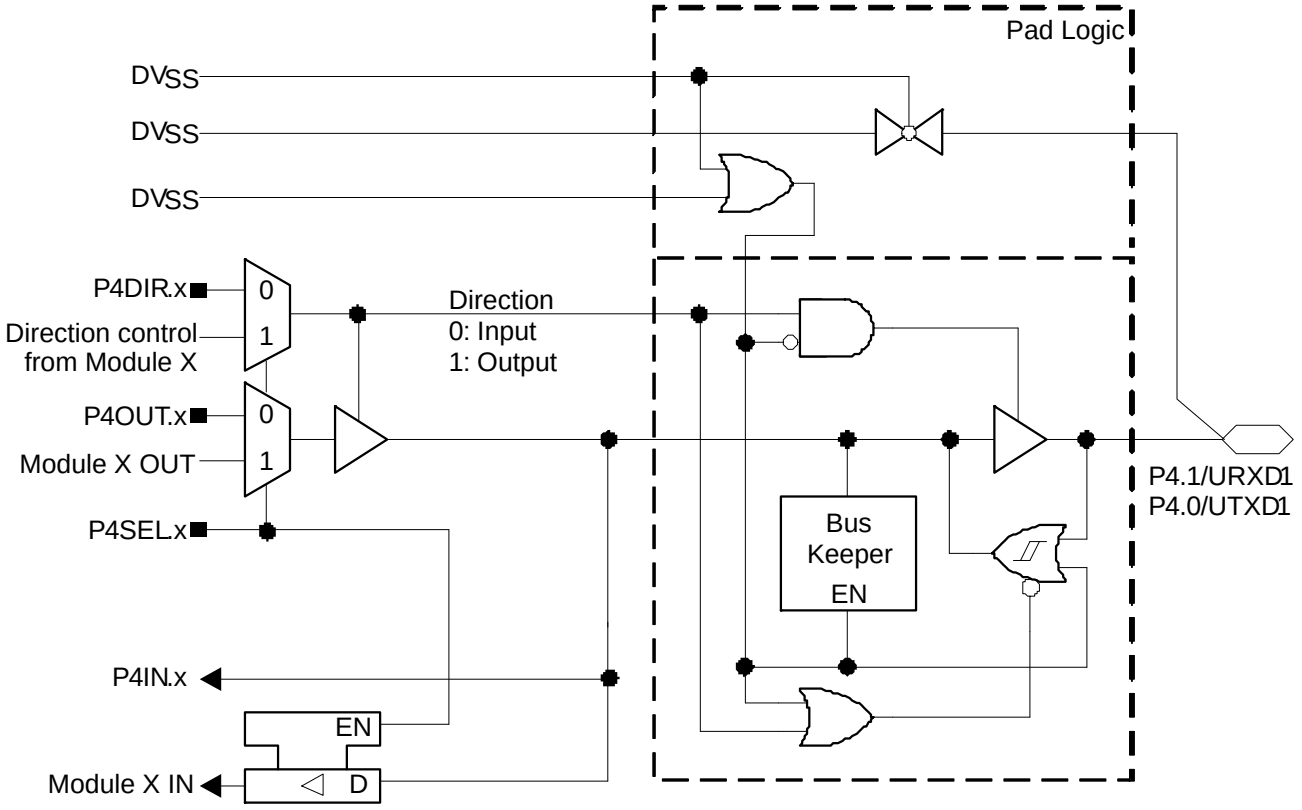
Note: x = 4,5,6,7

Port P3 (P3.4 to P3.7) pin functions

PIN NAME (P3.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P3DIR.x	P3SEL.x
P3.4/TB3	4	P3.4 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI3A and Timer_B7.CCI3B	0	1
		Timer_B7.TB3 (see Note 1)	1	1
P3.5/TB4	5	P3.5 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI4A and Timer_B7.CCI4B	0	1
		Timer_B7.TB4 (see Note 1)	1	1
P3.6/TB5	6	P3.6 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI5A and Timer_B7.CCI5B	0	1
		Timer_B7.TB5 (see Note 1)	1	1
P3.7/TB6	7	P3.7 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI6A and Timer_B7.CCI6B	0	1
		Timer_B7.TB6 (see Note 1)	1	1

NOTE 1: Setting TBOUTH causes all Timer_B outputs to be set to high impedance.

port P4, P4.0 to P4.1, input/output with Schmitt trigger



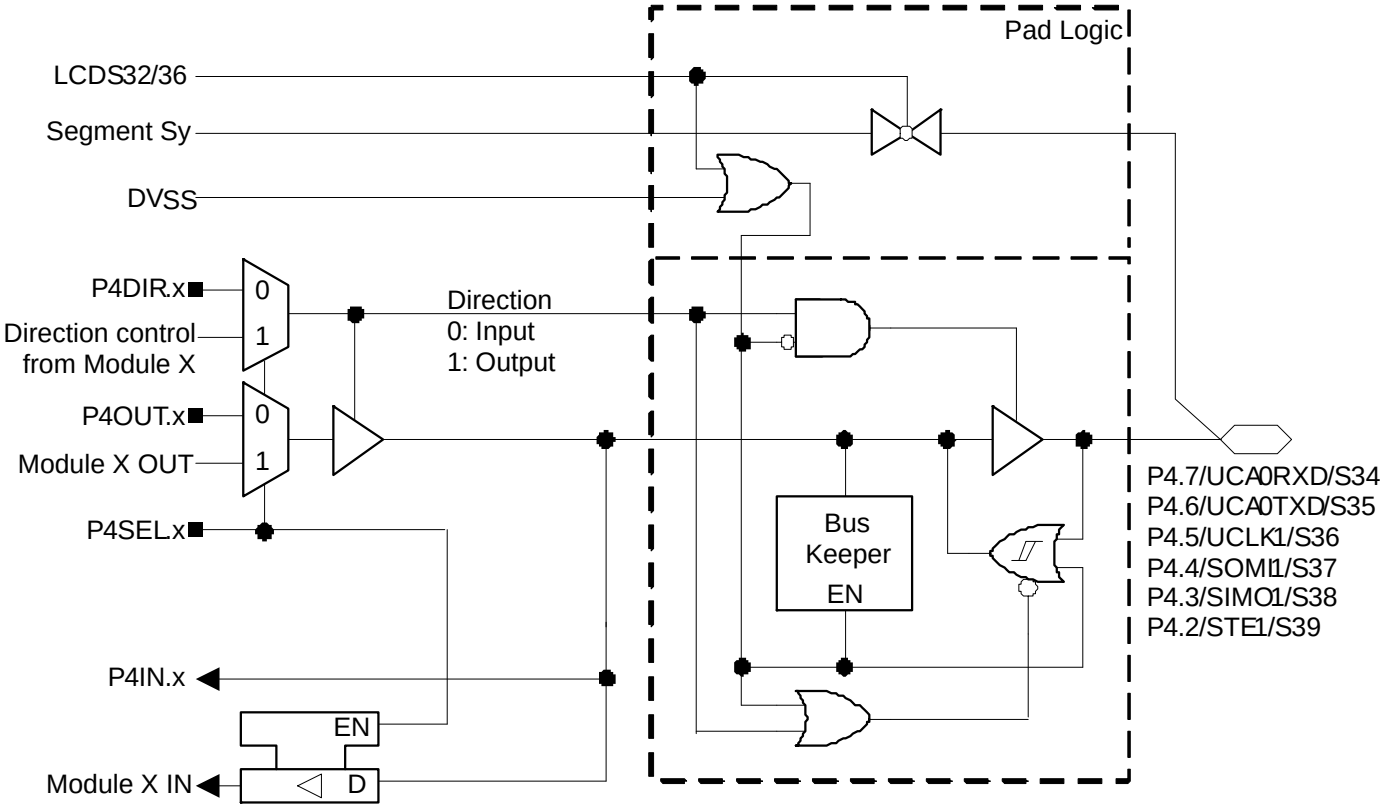
Note: x = 0,1

Port P4 (P4.0 to P4.1) pin functions

PIN NAME (P4.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P4DIR.x	P4SEL.x
P4.0/UTXD1	0	P4.0 (I/O)	I: 0; O: 1	0
		USART1.UTXD1 (see Notes 1, 2)	X	1
P4.1/URXD1	1	P4.1 (I/O)	I: 0; O: 1	0
		USART1.URXD1 (see Notes 1, 2)	X	1

NOTES: 1. X: Don't care
2. When in USART1 mode, P4.0 is set to output, P4.1 is set to input.

port P4, P4.2 to P4.7, input/output with Schmitt trigger



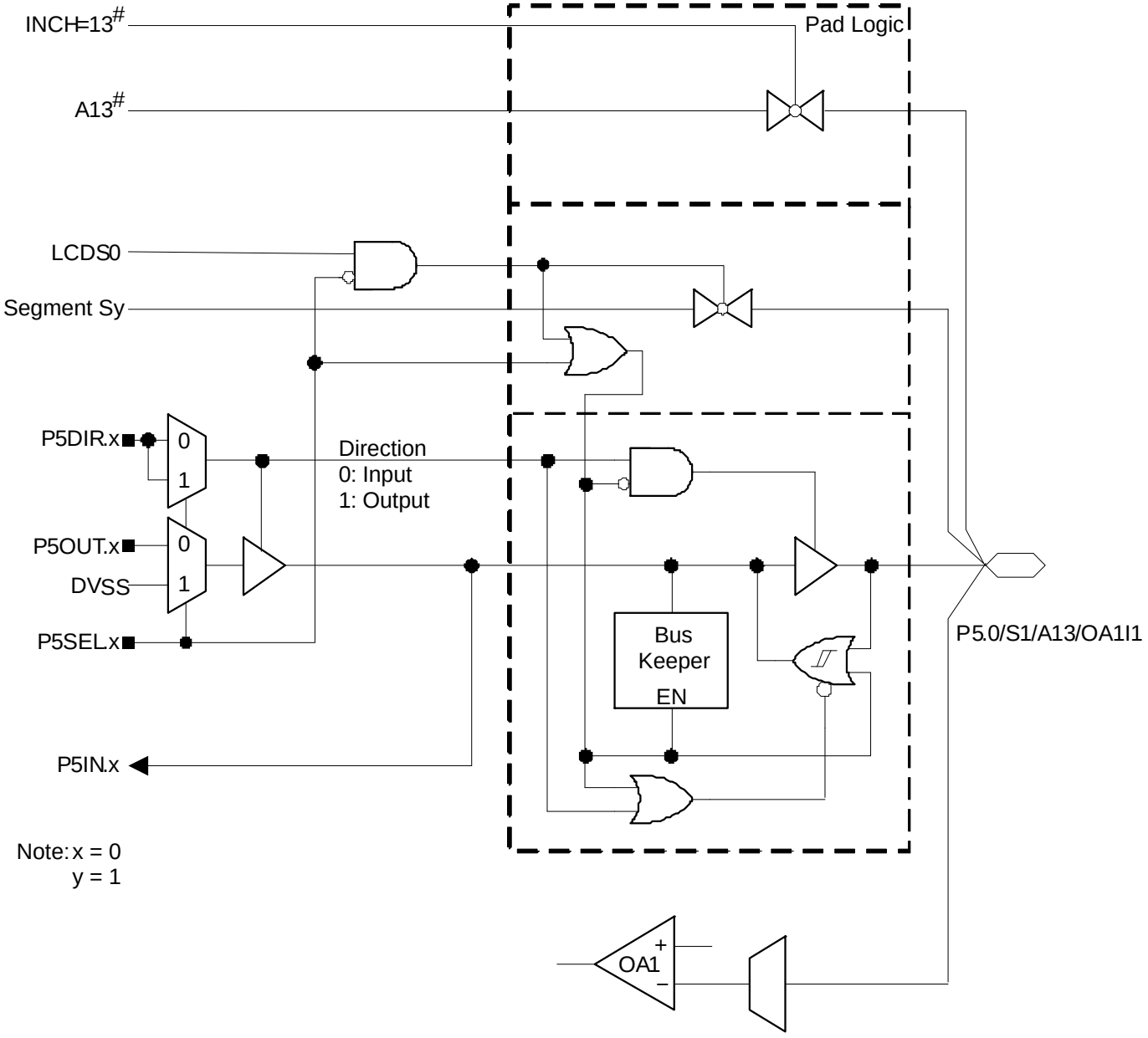
Note : x = 2,3,4,5,6,7
y = 34,35,36,37,38,39

Port P4 (P4.2 to P4.5) pin functions

PIN NAME (P4.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P4DIR.x	P4SEL.x	LCDS36
P4.2/STE1/S39	2	P4.2 (I/O)	I: 0; O: 1	0	0
		USART1.STE1	X	1	0
		S39 (see Note 1)	X	X	1
P4.3/SIMO/S38	3	P4.3 (I/O)	I: 0; O: 1	0	0
		USART1.SIMO1 (see Notes 1, 2)	X	1	0
		S38 (see Note 1)	X	X	1
P4.4/SOMI/S37	4	P4.4 (I/O)	I: 0; O: 1	0	0
		USART1.SOMI1 (see Notes 1, 2)	X	1	0
		S37 (see Note 1)	X	X	1
P4.5/SOMI/S36	5	P4.5 (I/O)	I: 0; O: 1	0	0
		USART1.UCLK1 (see Notes 1, 2)	X	1	0
		S36 (see Note 1)	X	X	1
P4.6/UCA0TXD/S35	6	P4.6 (I/O)	I: 0; O: 1	0	0
		USCI_A0.UCA0TXD (see Notes 1, 3)	X	1	0
		S35 (see Note 1)	X	X	1
P4.7/UCA0RXD/S34	7	P4.7 (I/O)	I: 0; O: 1	0	0
		USCI_A0.UCA0RXD (see Notes 1, 3)	X	1	0
		S34 (see Note 1)	X	X	1

NOTES: 1. X: Don't care
2. The pin direction is controlled by the USART1 module.
3. When in USCI mode, P4.6 is set to output, P4.7 is set to input.

port P5, P5.0, input/output with Schmitt trigger

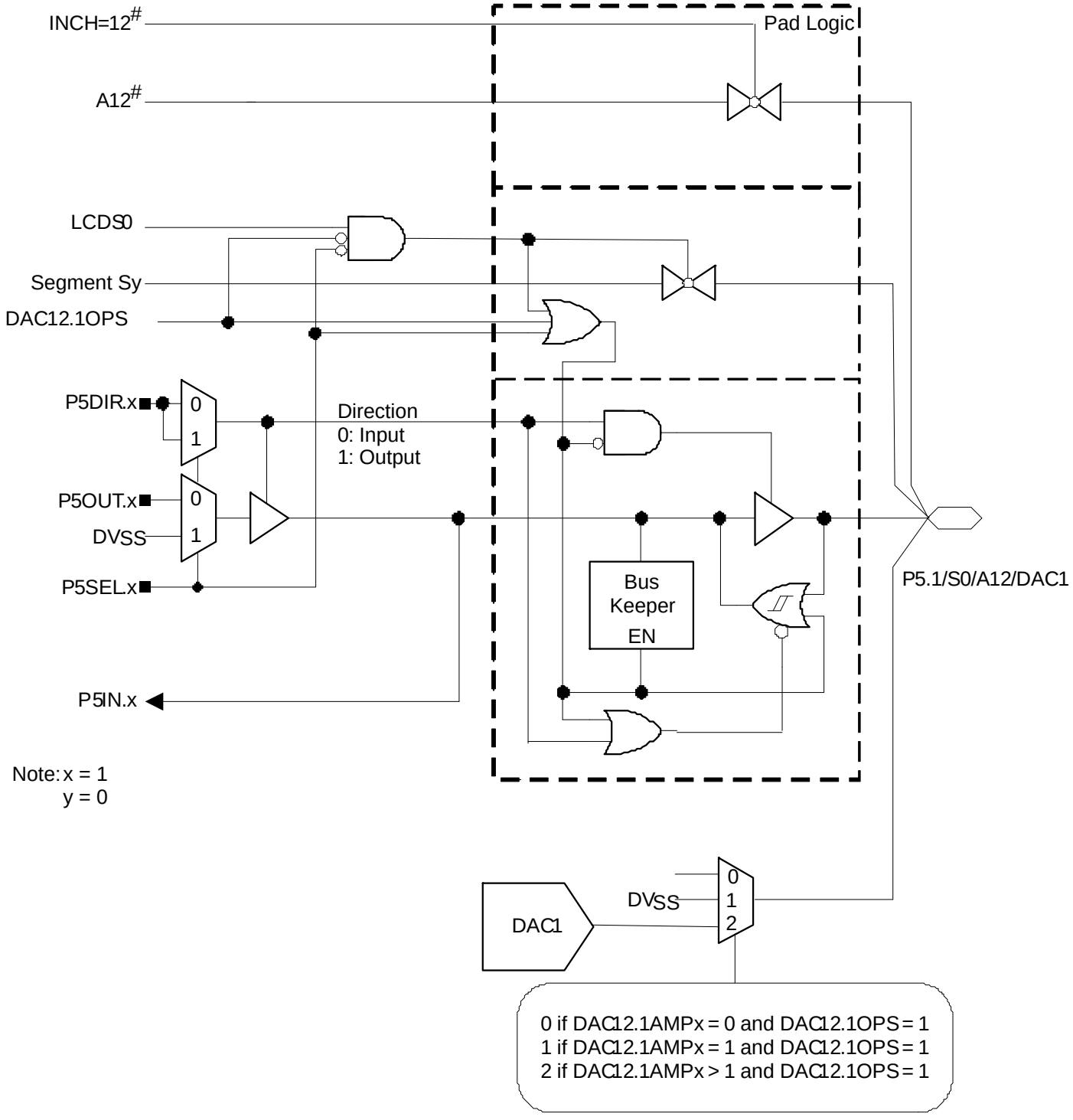


Port P5 (P5.0) pin functions

PIN NAME (P5.X)	X	FUNCTION	CONTROL BITS / SIGNALS				
			P5DIR.x	P5SEL.x	INCHx	OAPx(OA1) OANx(OA1)	LCDS0
P5.0/S1/A13/OA1I1	0	P5.0 (I/O) (see Note 1)	I: 0; O: 1	0	X	X	0
		OAI11 (see Note 1)	0	X	X	1	0
		A13 (see Notes 1, 3)	X	1	13	X	X
		S1 enabled (see Note 1)	X	0	X	X	1
		S1 disabled (see Note 1)	X	1	X	X	1

NOTES: 1. X: Don't care
2. N/A: Not available or not applicable.
3. Setting the P5SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

port P5, P5.1, input/output with Schmitt trigger

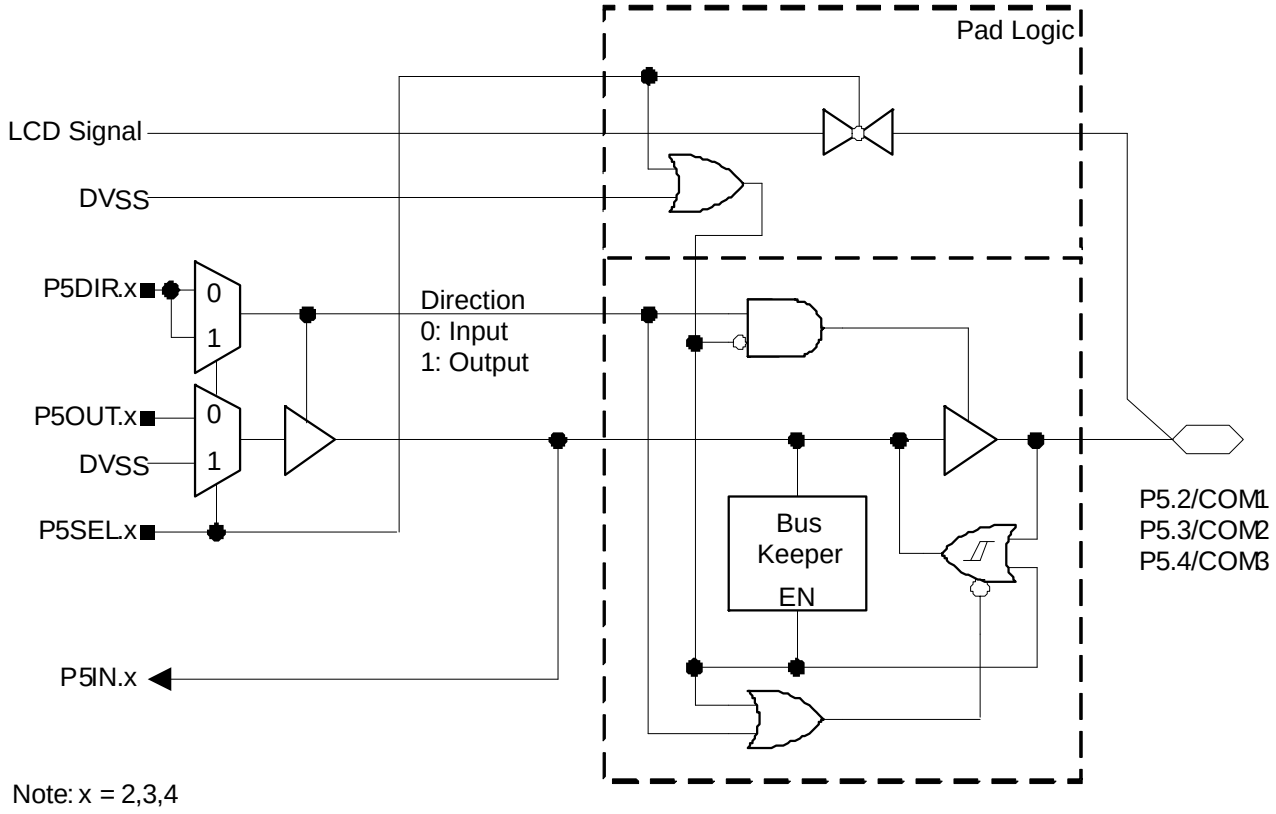


Port P5 (P5.1) pin functions

PIN NAME (P5.X)	X	FUNCTION	CONTROL BITS / SIGNALS					
			P5DIR.x	P5SEL.x	INCHx	DAC12.1OPS	DAC12.1AMPx	LCDS0
P5.1/S0/A12/DAC1	1	P5.1 (I/O) (see Note 1)	I: 0; O: 1	0	X	0	X	0
		DAC1 high impedance (see Note 1)	X	X	X	1	0	X
		DVSS (see Note 1)	X	X	X	1	1	X
		DAC1 output (see Note 1)	X	X	X	1	> 1	X
		A12 (see Notes 1, 2)	X	1	12	0	X	0
		S0 enabled (see Note 1)	X	0	X	0	X	1
		S0 disabled (see Note 1)	X	1	X	0	X	1

NOTES: 1. X: Don't care
2. Setting the P5SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

port P5, P5.2 to P5.4, input/output with Schmitt trigger

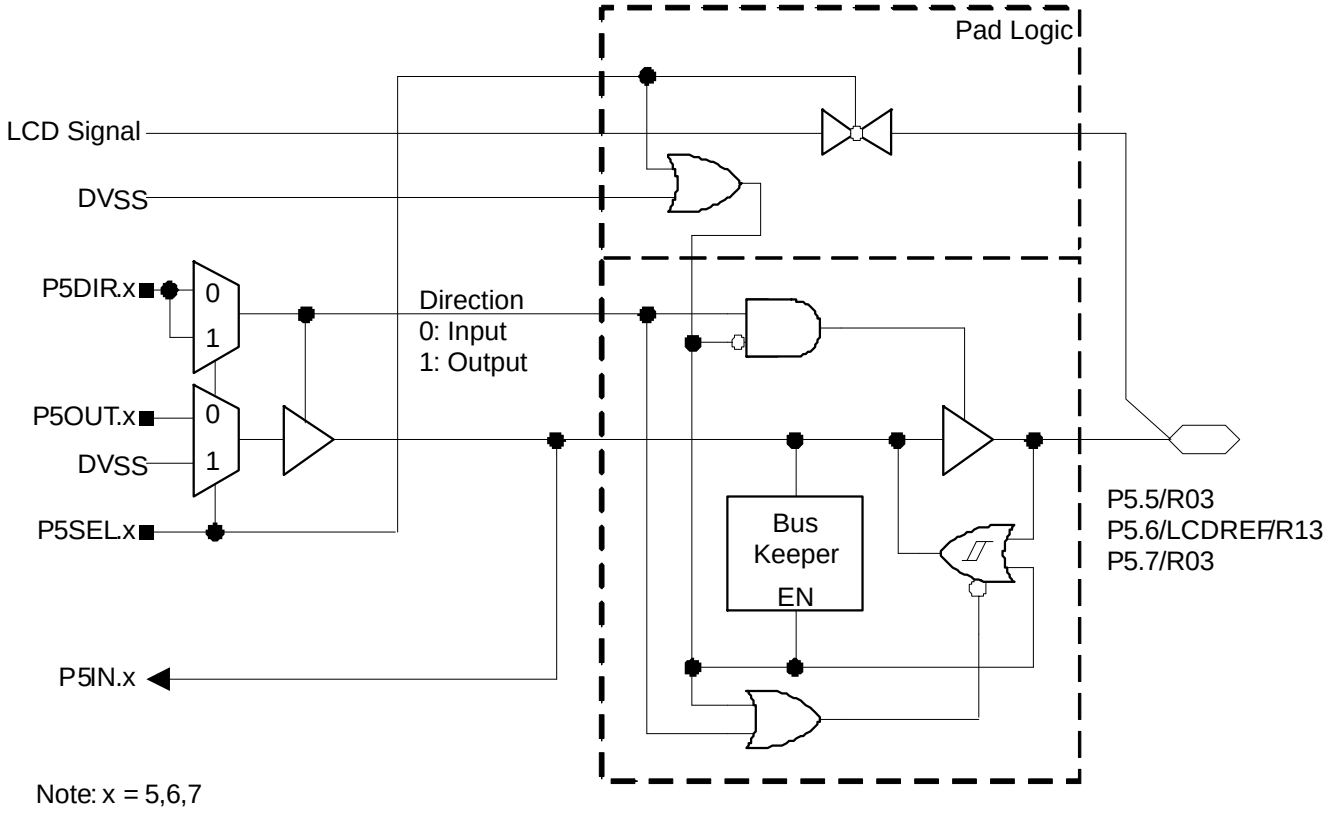


Port P5 (P5.2 to P5.4) pin functions

PIN NAME (P5.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P5DIR.x	P5SEL.x
P5.2/COM1	2	P5.2 (I/O)	I: 0; O: 1	0
		COM1 (see Note 1)	X	1
P5.3/COM2	3	P5.3 (I/O)	I: 0; O: 1	0
		COM2 (see Note 1)	X	1
P5.4/COM3	4	P5.4 (I/O)	I: 0; O: 1	0
		COM3 (see Note 1)	X	1

NOTE 1: X: Don't care

port P5, P5.5 to P5.7, input/output with Schmitt trigger

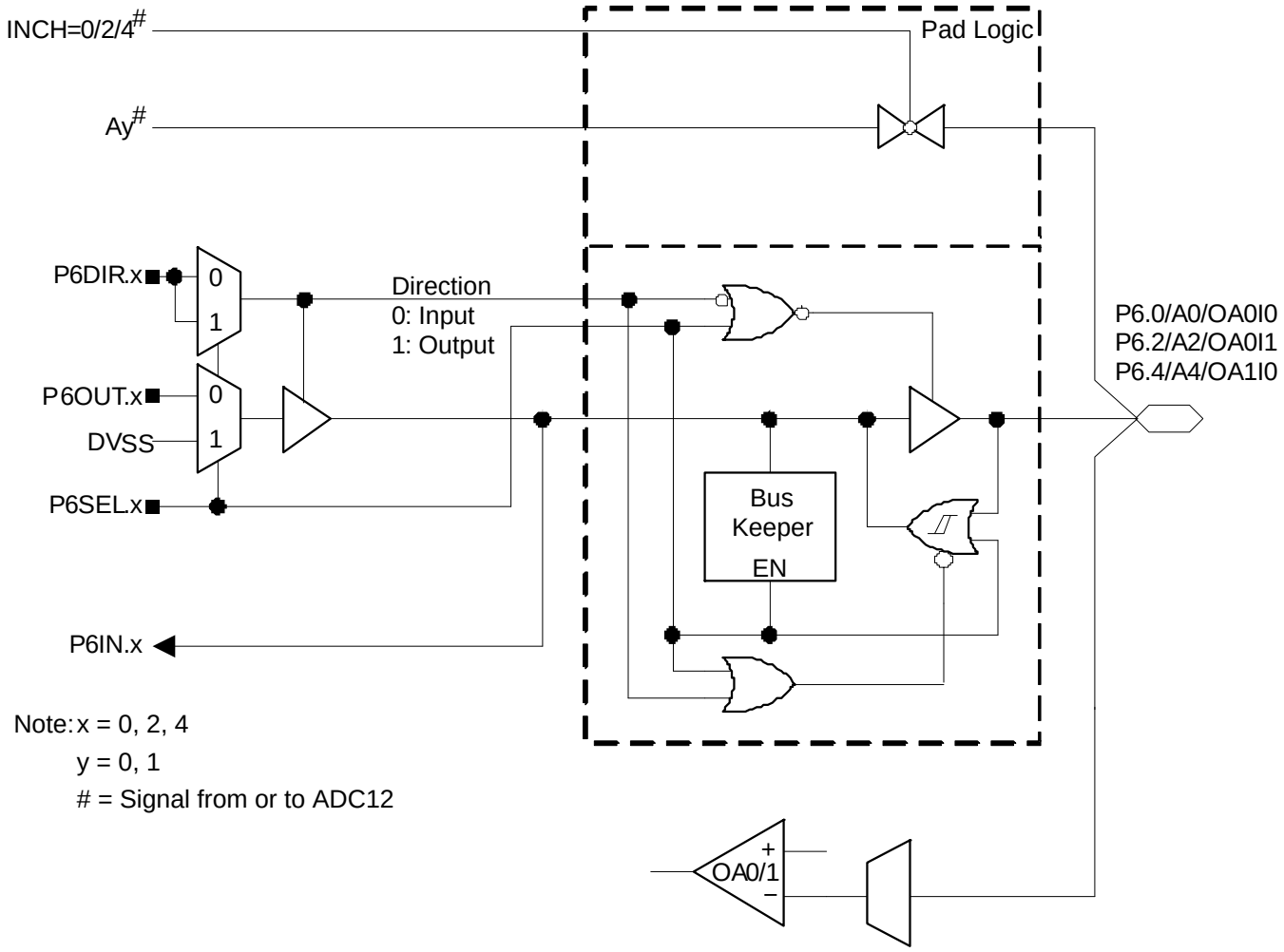


Port P5 (P5.5 to P5.7) pin functions

PIN NAME (P5.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P5DIR.x	P5SEL.x
P5.5/R03	5	P5.5 (I/O)	I: 0; O: 1	0
		R03 (see Note 1)	X	1
P5.6/LCDREF/R13	6	P5.6 (I/O)	I: 0; O: 1	0
		R13 or LCDREF (see Notes 1, 2)	X	1
P5.7/R03	7	P5.7 (I/O)	I: 0; O: 1	0
		R03 (see Note 1)	X	1

NOTES: 1. X: Don't care
2. External reference for the LCD_A charge pump is applied when VLCDREFx = 01. Otherwise R13 is selected.

port P6, P6.0, P6.2, and P6.4, input/output with Schmitt trigger

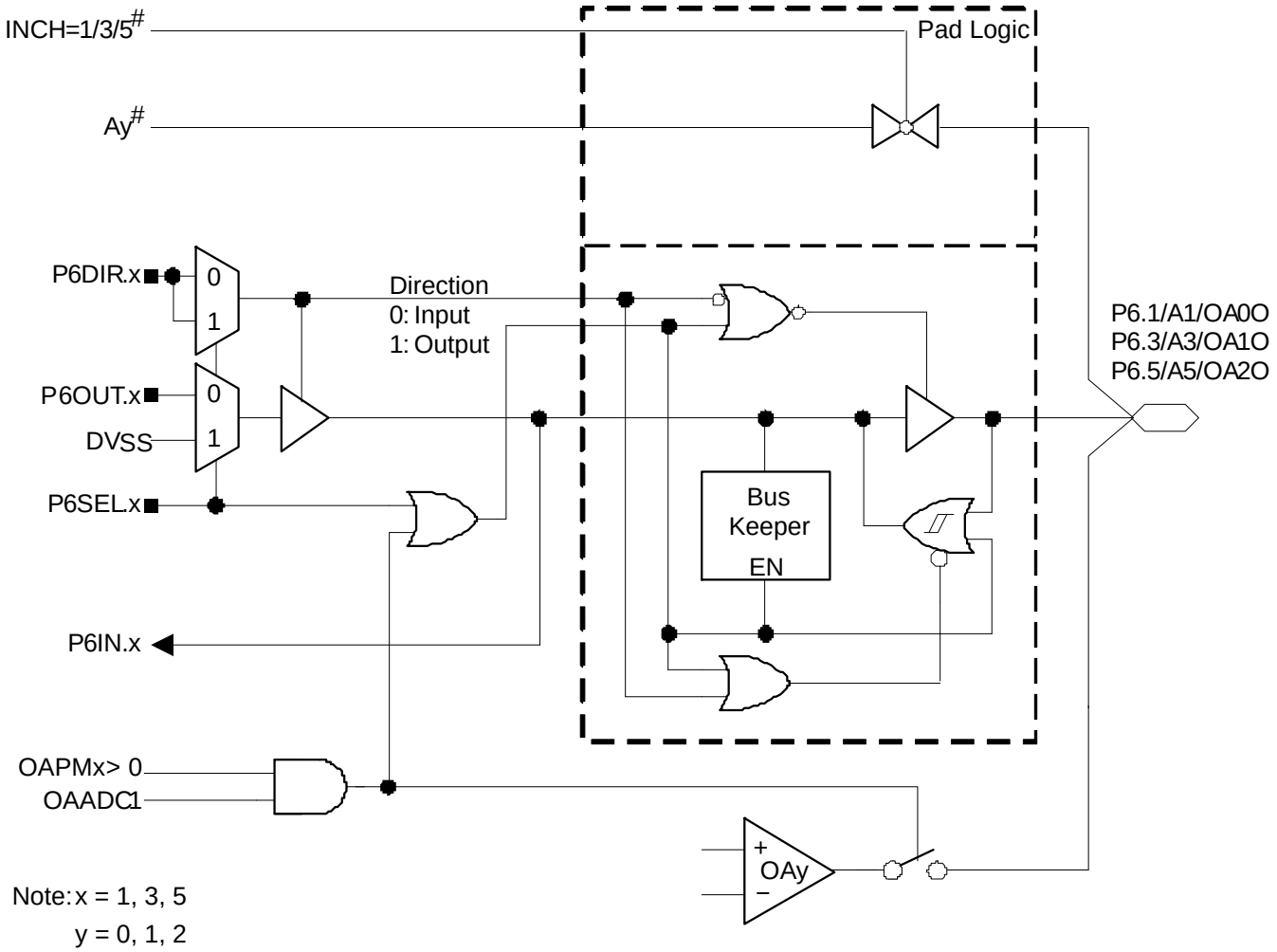


Port P6 (P6.0, P6.2, and P6.4) pin functions

PIN NAME (P6.X)	X	FUNCTION	CONTROL BITS / SIGNALS				
			P6DIR.x	P6SEL.x	OAPx (OA0) OANx (OA0)	OAPx (OA1) OANx(OA1)	INCHx
P6.0/A0/OA0I0	0	P6.0 (I/O) (see Note 1)	I: 0; O: 1	0	X	X	X
		OA0I0 (see Note 1)	0	X	0	X	X
		A0 (see Notes 1, 3)	X	1	X	X	0
P6.2/A2/OA0I1	2	P6.2 (I/O) (see Note 1)	I: 0; O: 1	0	X	X	X
		OA0I1 (see Note 1)	0	X	1	X	X
		A2 (see Notes 1, 3)	X	1	X	X	2
P6.4/A4/OA1I0	4	P6.4 (I/O) (see Note 1)	I: 0; O: 1	0	X	X	X
		OA1I0 (see Note 1)	0	X	X	0	X
		A4 (see Notes 1, 3)	X	1	X	X	4

NOTES: 1. X: Don't care
2. N/A: Not available or not applicable.
3. Setting the P6SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

port P6, P6.1, P6.3, and P6.5 input/output with Schmitt trigger



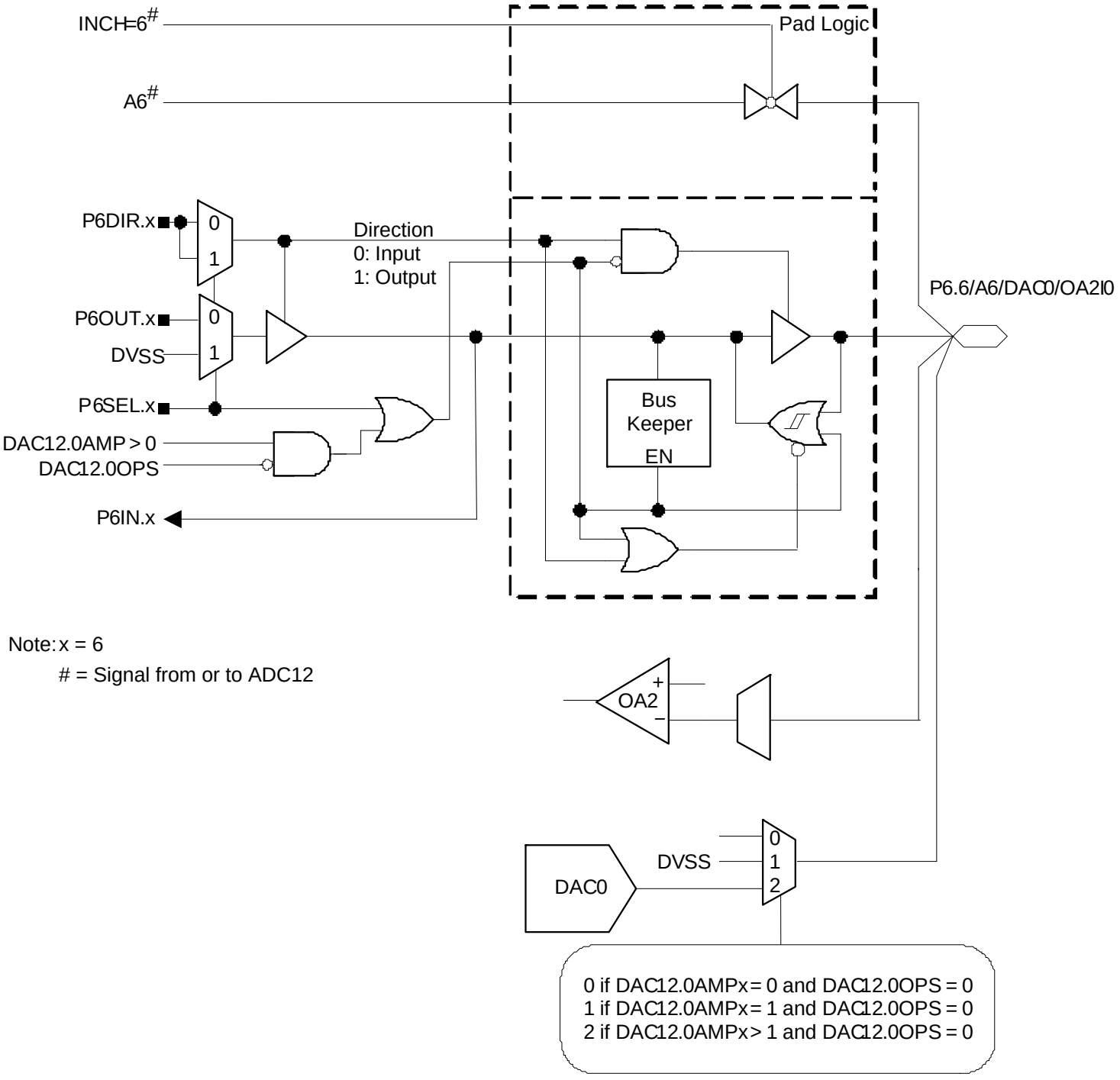
Note: x = 1, 3, 5
y = 0, 1, 2
# = Signal from or to ADC12

Port P6 (P6.1, P6.3, and P6.5) pin functions

PIN NAME (P6.X)	X	FUNCTION	CONTROL BITS / SIGNALS				
			P6DIR.x	P6SEL.x	OAADC1	OAPMx	INCHx
P6.1/A1/OA0O	1	P6.1 (I/O) (see Note 1)	I: 0; O: 1	0	X	0	X
		OA0O (see Notes 1, 4)	X	X	1	> 0	X
		A1 (see Notes 1, 3)	X	1	X	0	1
P6.3/A3/OA1O	3	P6.3 (I/O) (see Note 1)	I: 0; O: 1	0	X	0	X
		OA1O (see Notes 1, 4)	X	X	1	> 0	X
		A3 (see Notes 1, 3)	X	1	X	0	3
P6.5/A5/OA2O	5	P6.5 (I/O) (see Note 1)	I: 0; O: 1	0	X	0	X
		OA2O (see Notes 1, 4)	X	X	1	> 0	X
		A5 (see Notes 1, 3)	X	1	X	0	5

NOTES: 1. X: Don't care
2. N/A: Not available or not applicable.
3. Setting the P6SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
4. Setting the OAADC1 bit or setting OAFCx = 00 will cause the operational amplifier to be present at the pin as well as internally connected to the corresponding ADC12 input.

port P6, P6.6, input/output with Schmitt trigger



Note: x = 6

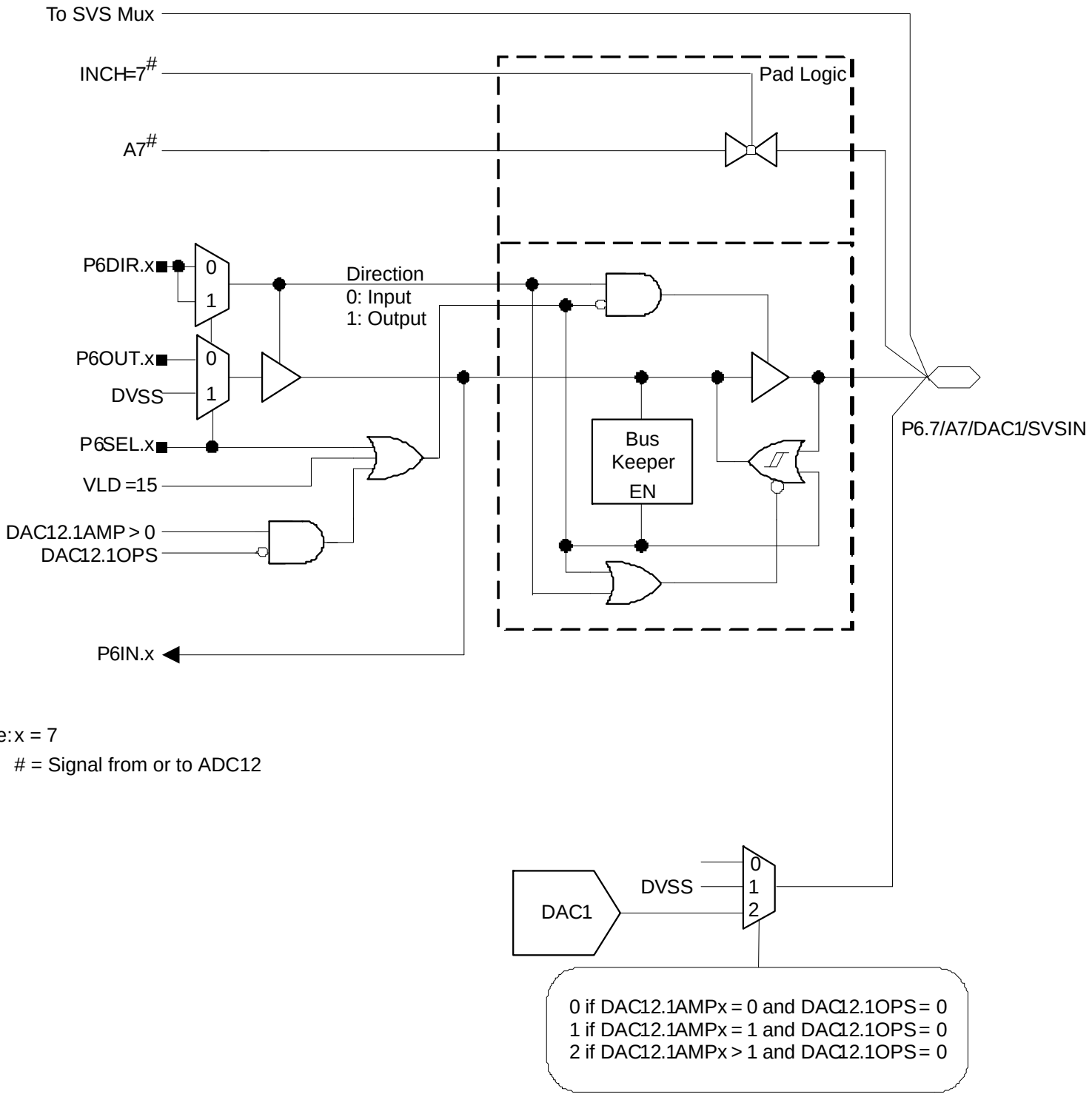
= Signal from or to ADC12

Port P6 (P6.6) pin functions

PIN NAME (P6.X)	X	FUNCTION	CONTROL BITS / SIGNALS					
			P6DIR.x	P6SEL.x	INCHx	DAC12.0OPS	DAC12.0AMPx	OAPx (OA2) OANx (OA2)
P6.6/A6/DAC0/OA2I0	6	P6.6 (I/O) (see Note 1)	I: 0; O: 1	0	X	1	X	X
		DAC0 high impedance (see Note 1)	X	X	X	0	0	X
		DVSS (see Note 1)	X	X	X	0	1	X
		DAC0 output (see Note 1)	X	X	X	0	>1	X
		A6 (see Notes 1, 2)	X	1	6	X	X	X
		OA2I0 (see Note 1)	0	X	0	X	X	0

NOTES: 1. X: Don't care
2. Setting the P6SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

port P6, P6.7, input/output with Schmitt trigger



Note: x = 7

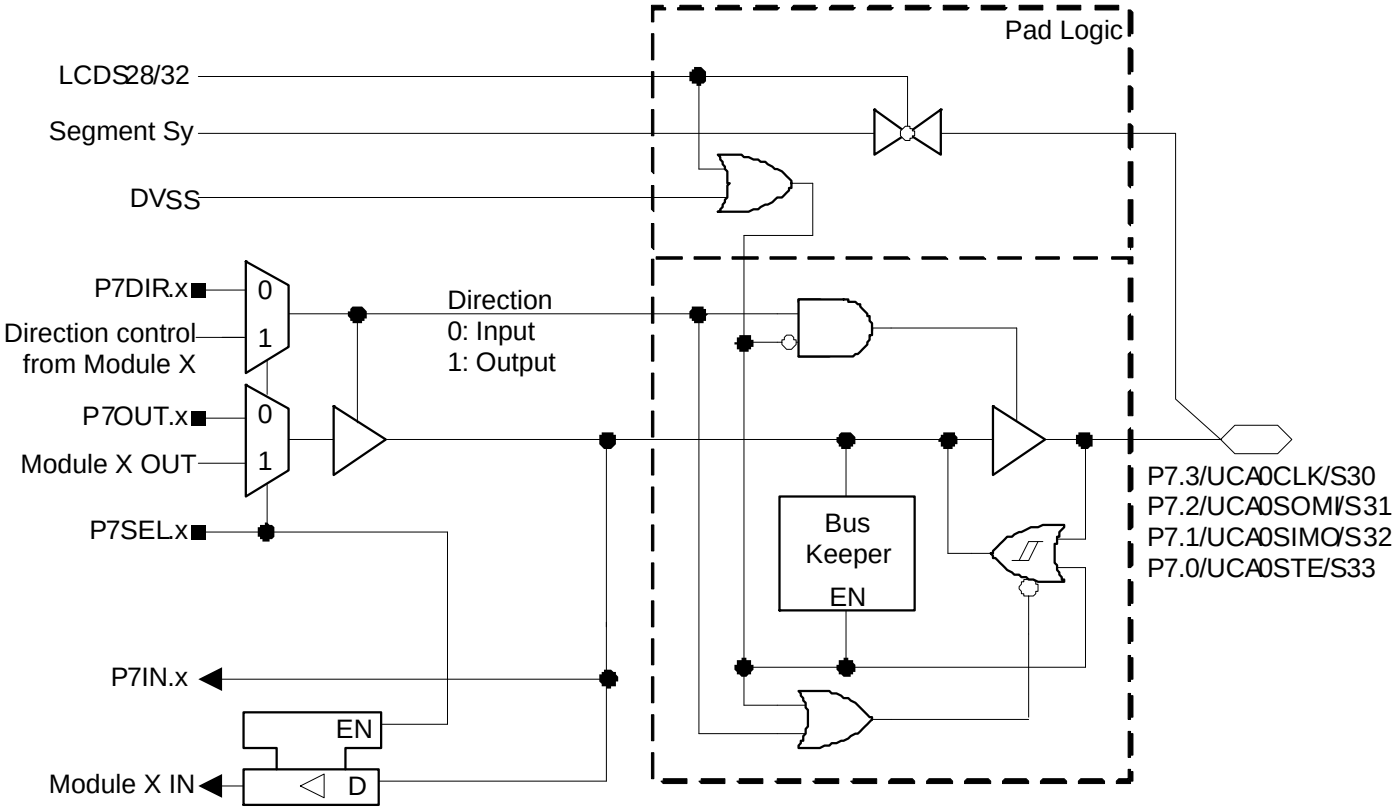
= Signal from or to ADC12

Port P6 (P6.7) pin functions

PIN NAME (P6.X)	X	FUNCTION	CONTROL BITS / SIGNALS				
			P6DIR.x	P6SEL.x	INCHx	DAC12.1OPS	DAC12.1AMPx
P6.7/A7/DAC1/SVSIN	7	P6.7 (I/O) (see Note 1)	I: 0; O: 1	0	X	1	X
		DAC1 high impedance (see Note 1)	X	X	X	0	0
		DVSS (see Note 1)	X	X	X	0	1
		DAC1 output (see Note 1)	X	X	X	0	> 1
		A7 (see Notes 1, 2)	X	1	7	X	X
		SVSIN (see Notes 1,3)	0	1	0	1	X

NOTES: 1. X: Don't care
2. Setting the P6SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
3. Setting VLDx = 15 will also cause the external SVSIN to be used. In this case, the P6SEL.x bit is a do not care.

port P7, P7.0 to P7.3, input/output with Schmitt trigger



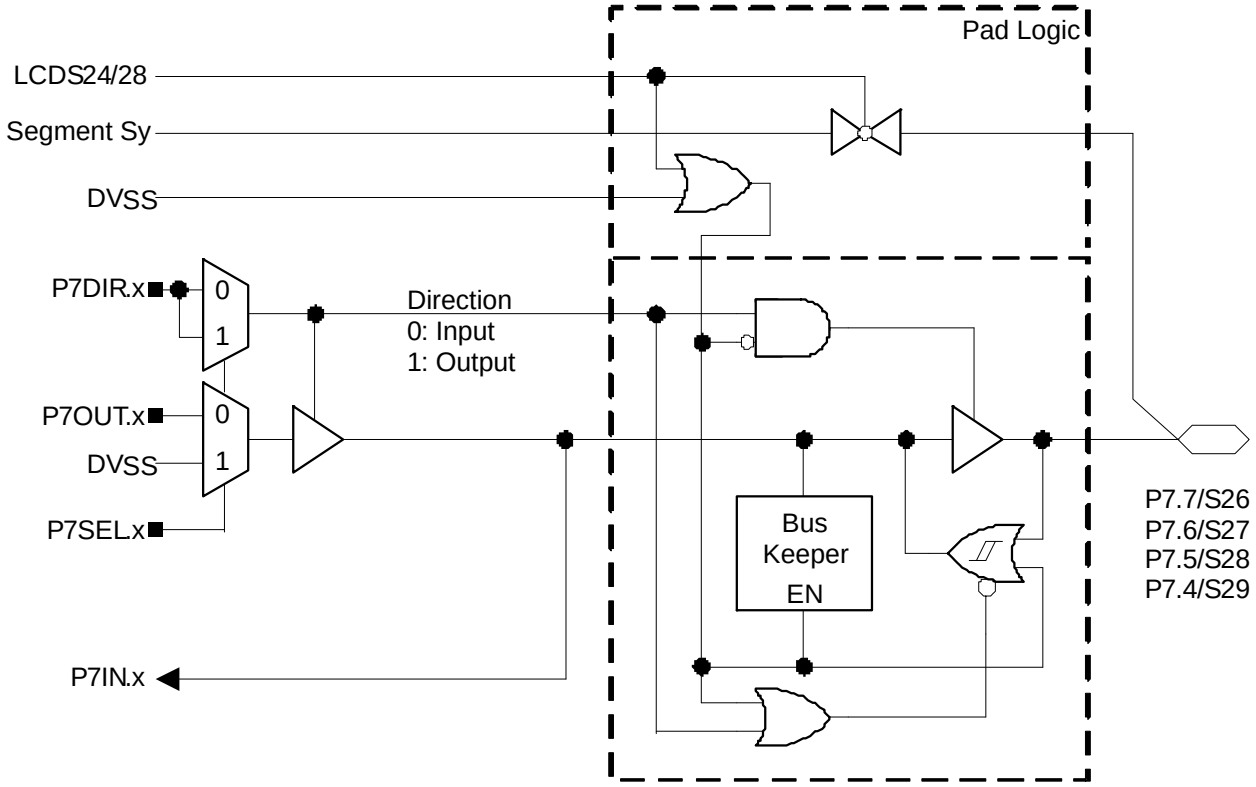
Note: x = 0, 1, 2, 3
y = 30, 31, 32, 33

Port P7 (P7.0 to P7.1) pin functions

PIN NAME (P7.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P7DIR.x	P7SEL.x	LCDS32
P7.0/UCA0STE/S33	0	P7.0 (I/O)	I: 0; O: 1	0	0
		USCI_A0.UCA0STE (see Notes 1, 2)	X	1	0
		S33 (see Note 1)	X	X	1
P7.1/UCA0SIMO/S32	1	P7.1 (I/O)	I: 0; O: 1	0	0
		USCI_A0.UCA0SIMO (see Notes 1, 2)	X	1	0
		S32 (see Note 1)	X	X	1
P7.2/UCA0SOMI/S31	2	P7.2 (I/O)	I: 0; O: 1	0	0
		USCI_A0.UCA0SOMI (see Notes 1, 3)	X	1	0
		S31 (see Note 1)	X	X	1
P7.3/UCA0CLK/S30	3	P7.3 (I/O)	I: 0; O: 1	0	0
		USCI_A0.UCA0CLK (see Notes 1, 3)	X	1	0
		S30 (see Note 1)	X	X	1

NOTES: 1. X: Don't care
2. The pin direction is controlled by the USCI module.
3. The pin direction is controlled by the USCI module.

port P7, P7.4 to P7.7, input/output with Schmitt trigger



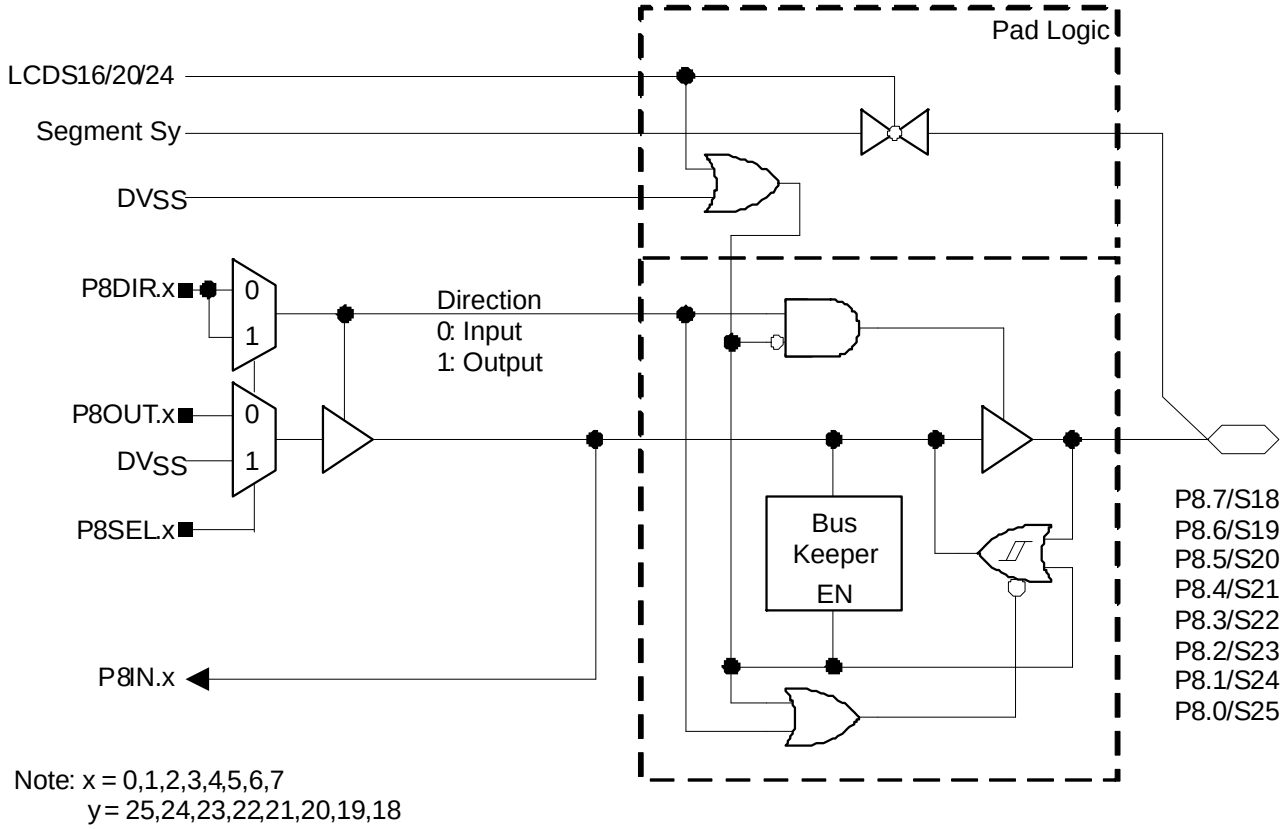
Note: x = 4, 5, 6, 7
y = 26, 27, 28, 29

Port P7 (P7.4 to P7.5) pin functions

PIN NAME (P7.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P7DIR.x	P7SEL.x	LCDS28
P7.4/S29	4	P7.4 (I/O)	I: 0; O: 1	0	0
		S29 (see Note 1)	X	X	1
P7.5/S28	5	P7.5 (I/O)	I: 0; O: 1	0	0
		S28 (see Note 1)	X	X	1
P7.6/S27	6	P7.6 (I/O)	I: 0; O: 1	0	0
		S27 (see Note 1)	X	X	1
P7.7/S26	7	P7.7 (I/O)	I: 0; O: 1	0	0
		S26 (see Note 1)	X	X	1

NOTE 1: X: Don't care

port P8, P8.0 to P8.7, input/output with Schmitt trigger



Note: x = 0,1,2,3,4,5,6,7
y = 25,24,23,22,21,20,19,18

Port P8 (P8.0 to P8.1) pin functions

PIN NAME (P8.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P8DIR.x	P8SEL.x	LCDS16
P8.0/S18	0	P8.0 (I/O)	I: 0; O: 1	0	0
		S18 (see Note 1)	X	X	1
P8.1/S19	0	P8.0 (I/O)	I: 0; O: 1	0	0
		S19 (see Note 1)	X	X	1
P8.2/S20	2	P8.2 (I/O)	I: 0; O: 1	0	0
		S20 (see Note 1)	X	X	1
P8.3/S21	3	P8.3 (I/O)	I: 0; O: 1	0	0
		S21 (see Note 1)	X	X	1
P8.4/S22	4	P8.4 (I/O)	I: 0; O: 1	0	0
		S22 (see Note 1)	X	X	1
P8.5/S23	5	P8.5 (I/O)	I: 0; O: 1	0	0
		S23 (see Note 1)	X	X	1

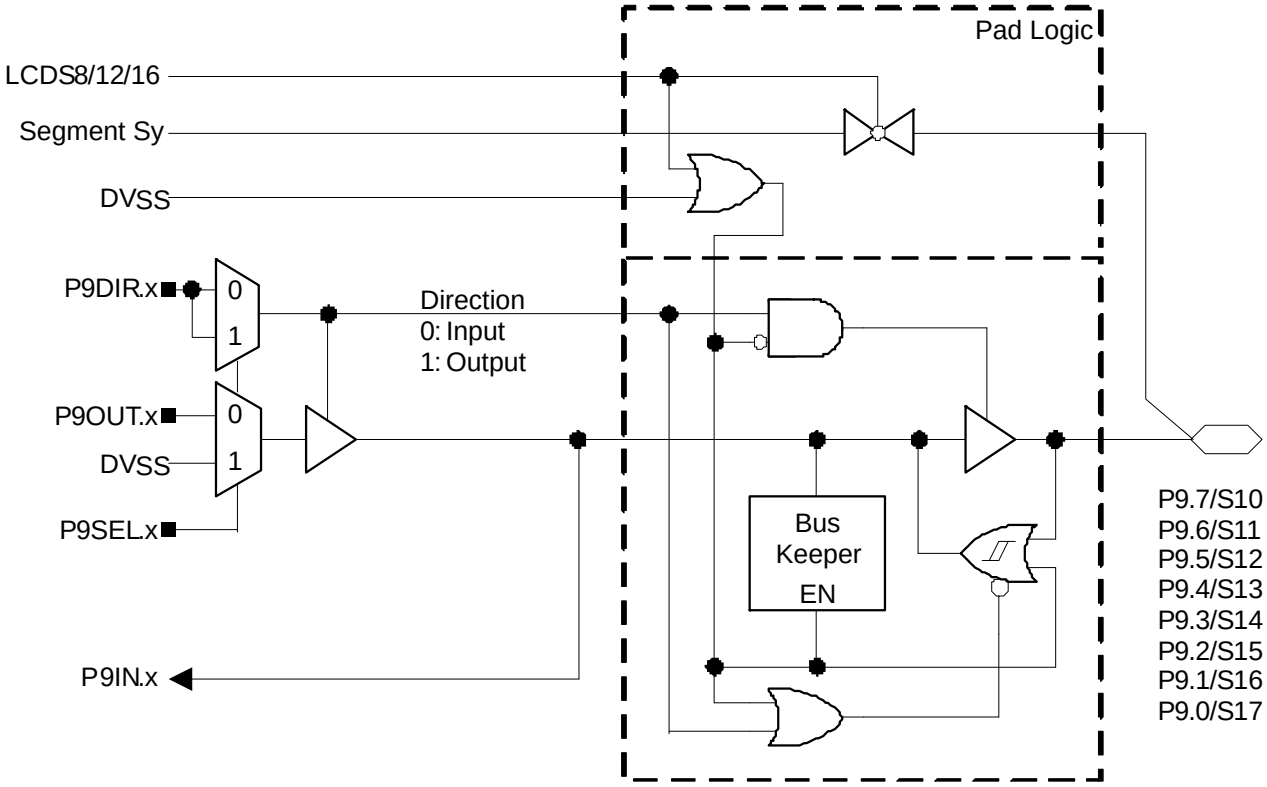
NOTE 1: X: Don’t care

Port P8 (P8.6 to P8.7) pin functions

PIN NAME (P8.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P8DIR.x	P8SEL.x	LCDS24
P8.6/S24	6	P8.6 (I/O)	I: 0; O: 1	0	0
		S24 (see Note 1)	X	X	1
P8.7/S25	7	P8.7 (I/O)	I: 0; O: 1	0	0
		S25 (see Note 1)	X	X	1

NOTE 1: X: Don’t care

port P9, P9.0 to P9.7, input/output with Schmitt trigger



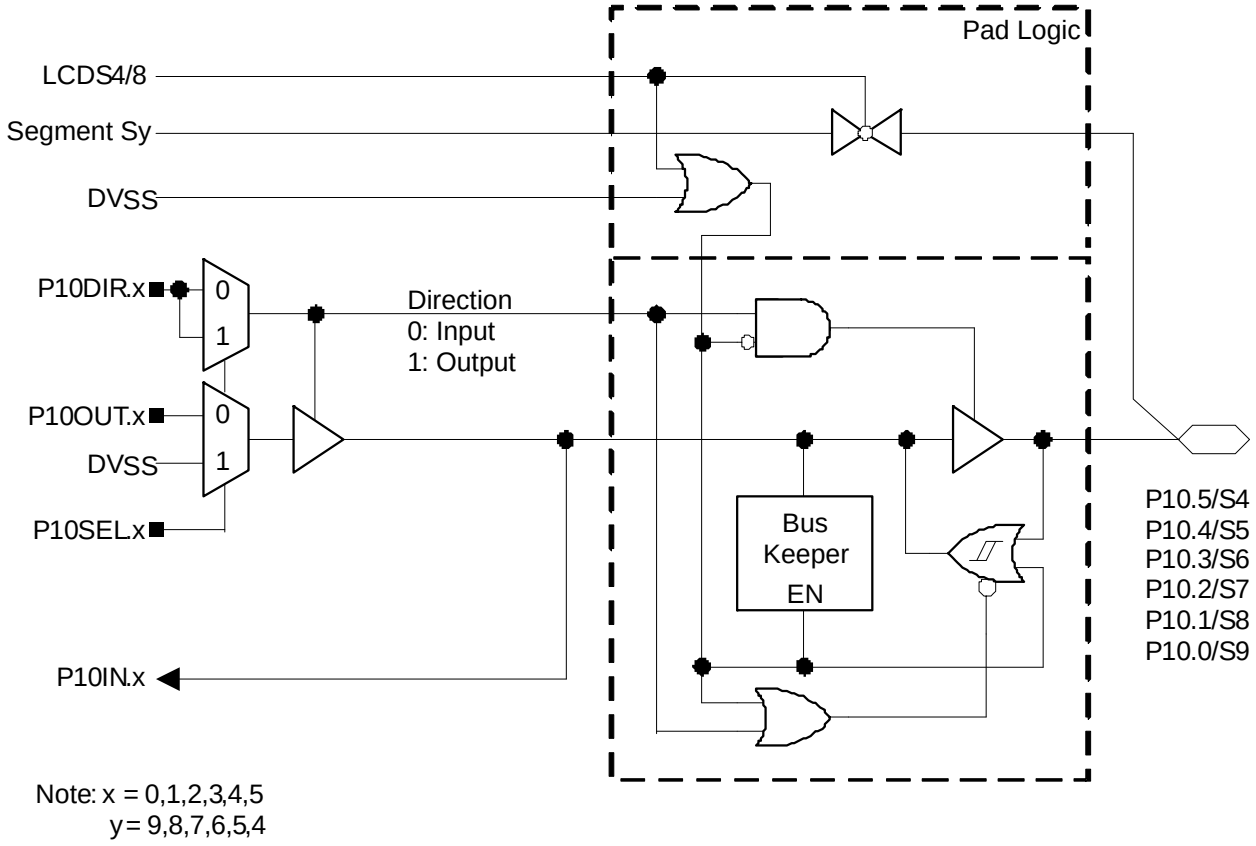
Note: x = 0,1,2,3,4,5,6,7
y = 17,16,15,14,13,12,11,10

Port P9 (P9.0 to P9.1) pin functions

PIN NAME (P9.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P9DIR.x	P9SEL.x	LCDS16
P9.0/S17	0	P9.0 (I/O)	I: 0; O: 1	0	0
		S17 (see Note 1)	X	X	1
P9.1/S16	1	P9.1 (I/O)	I: 0; O: 1	0	0
		S16 (see Note 1)	X	X	1
P9.2/S20	2	P9.2 (I/O)	I: 0; O: 1	0	0
		S15 (see Note 1)	X	X	1
P9.3/S21	3	P9.3 (I/O)	I: 0; O: 1	0	0
		S14 (see Note 1)	X	X	1
P9.4/S22	4	P9.4 (I/O)	I: 0; O: 1	0	0
		S13 (see Note 1)	X	X	1
P9.5/S23	5	P9.5 (I/O)	I: 0; O: 1	0	0
		S12 (see Note 1)	X	X	1
P9.6/S24	6	P9.6 (I/O)	I: 0; O: 1	0	0
		S11 (see Note 1)	X	X	1
P9.7/S25	7	P9.7 (I/O)	I: 0; O: 1	0	0
		S10 (see Note 1)	X	X	1

NOTE 1: X: Don’t care

port P10, P10.0 to P10.5, input/output with Schmitt trigger

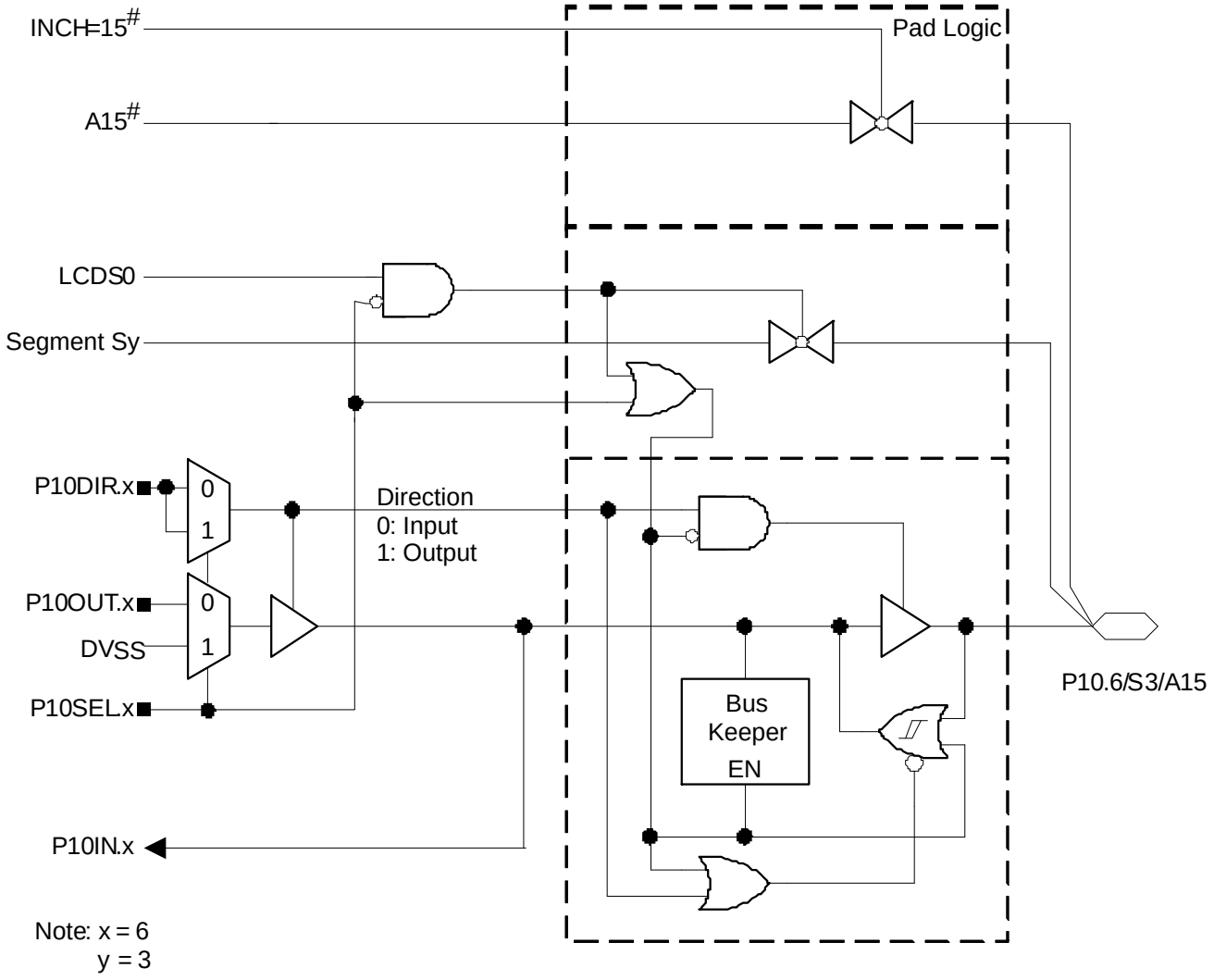


Port P10 (P10.0 to P10.1) pin functions

PIN NAME (P10.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P10DIR.x	P10SEL.x	LCDS8
P10.0/S8	0	P10.0 (I/O)	I: 0; O: 1	0	0
		S8 (see Note 1)	X	X	1
P10.1/S7	1	P10.1 (I/O)	I: 0; O: 1	0	0
		S7 (see Note 1)	X	X	1
P10.2/S7	2	P10.2 (I/O)	I: 0; O: 1	0	0
		S7 (see Note 1)	X	X	1
P10.3/S6	3	P10.3 (I/O)	I: 0; O: 1	0	0
		S6 (see Note 1)	X	X	1
P10.4/S5	4	P10.4 (I/O)	I: 0; O: 1	0	0
		S5 (see Note 1)	X	X	1
P10.5/S4	5	P10.5 (I/O)	I: 0; O: 1	0	0
		S4 (see Note 1)	X	X	1

NOTE 1: X: Don't care

port P10, P10.6, input/output with Schmitt trigger

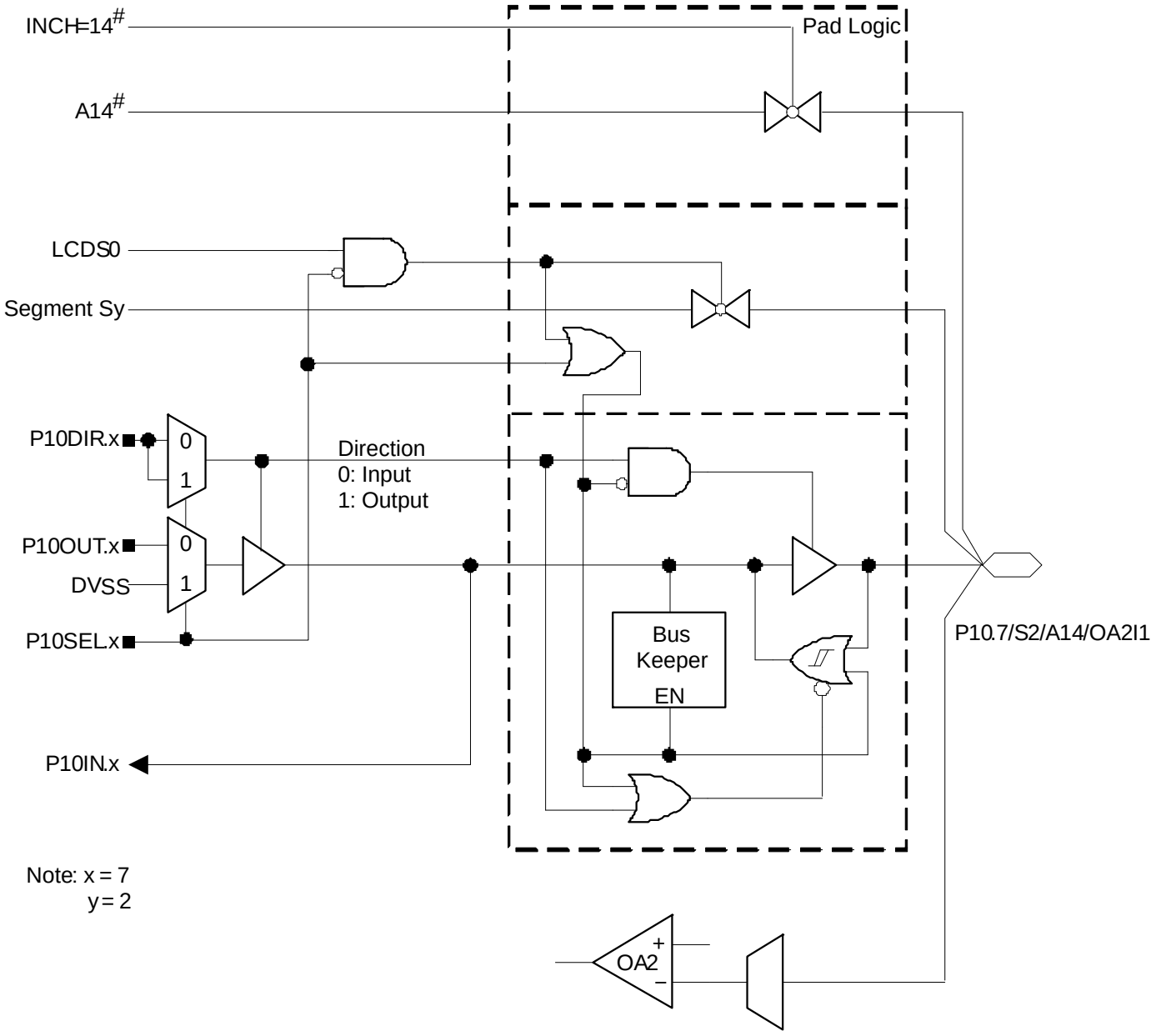


Port P10 (P10.6) pin functions

PIN NAME (P10.X)	X	FUNCTION	CONTROL BITS / SIGNALS			
			P10DIR.x	P10SEL.x	INCHx	LCDS0
P10.6/S3/A15	6	P5.0 (I/O) (see Note 1)	I: 0; O: 1	0	X	0
		A15 (see Notes 1, 3)	X	1	15	0
		S3 enabled (see Note 1)	X	0	X	1
		S3 disabled (see Note 1)	X	1	X	1

NOTES: 1. X: Don't care
2. N/A: Not available or not applicable.
3. Setting the P10SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

port P10, P10.7, input/output with Schmitt trigger

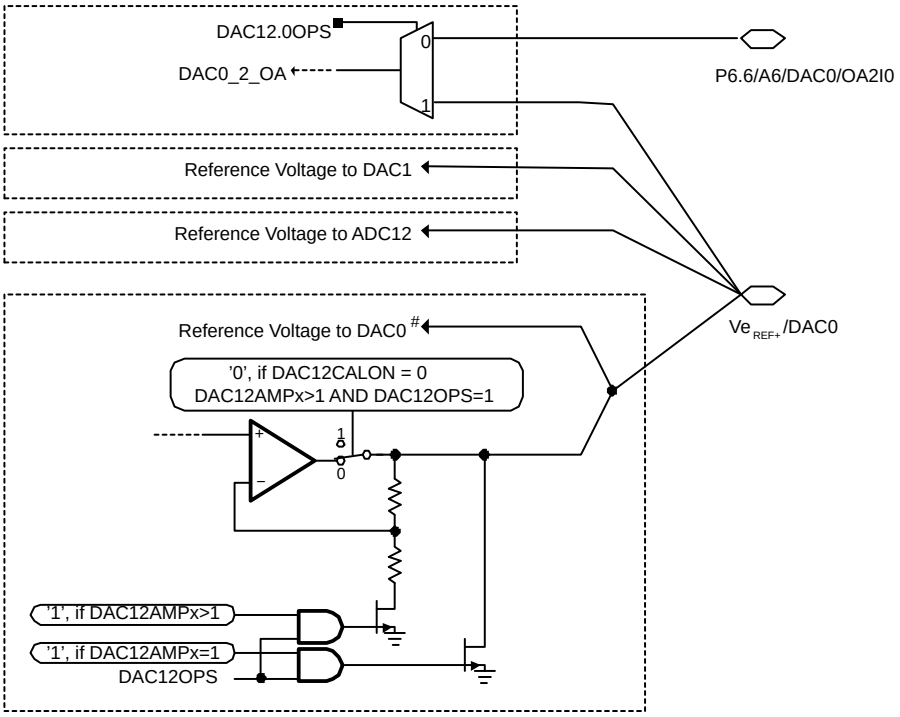


Port P10 (P10.7) pin functions

PIN NAME (P10.X)	X	FUNCTION	CONTROL BITS / SIGNALS				
			P10DIR.x	P10SEL.x	INCHx	OAPx (OA1) OANx (OA1)	LCDS0
P10.7/S2/A14/OA2I1	7	P10.7 (I/O) (see Note 1)	I: 0; O: 1	0	X	X	0
		A14 (see Notes 1, 3)	X	1	14	X	0
		OA2I1 (see Notes 1, 3)	0	X	X	1	0
		S2 enabled (see Note 1)	X	0	X	X	1
		S2 disabled (see Note 1)	X	1	X	X	1

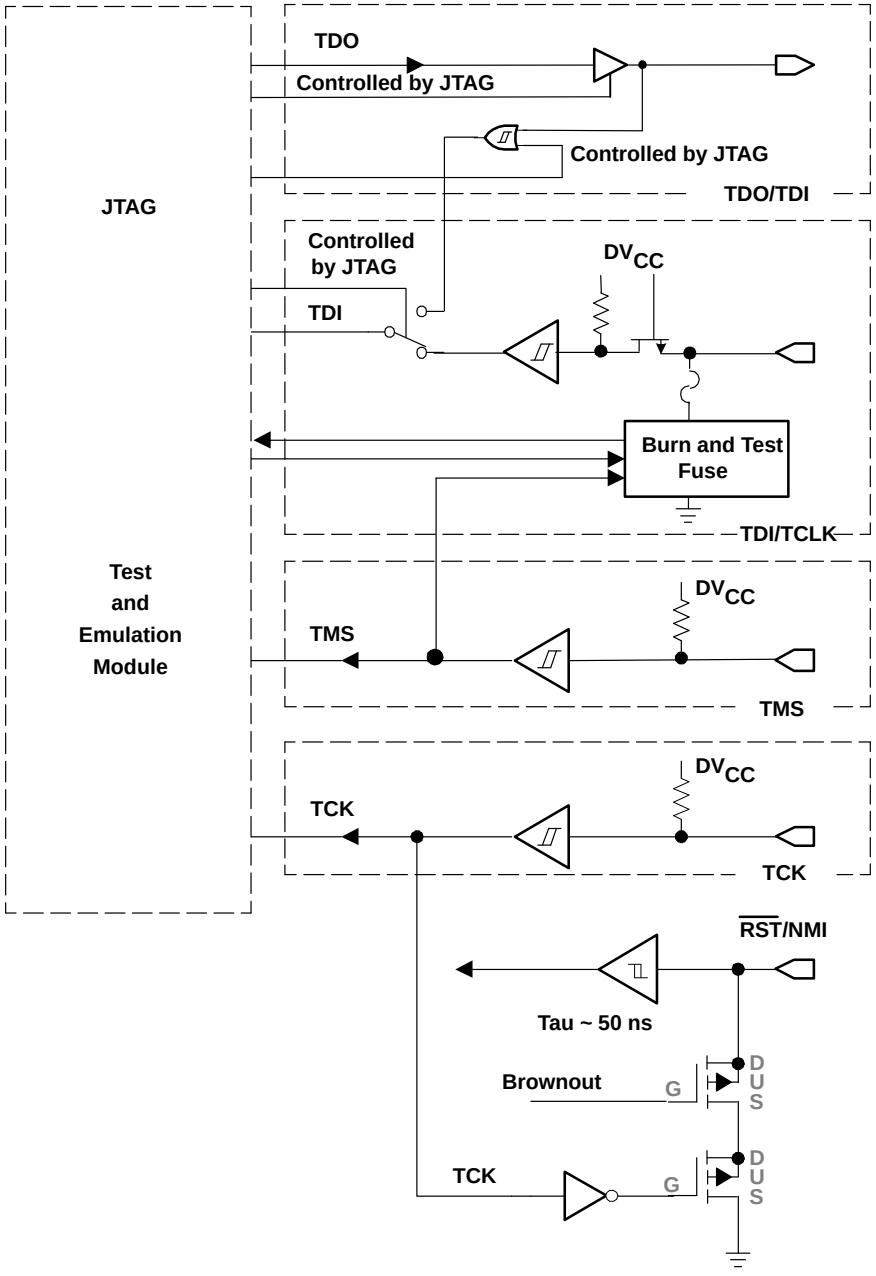
NOTES: 1. X: Don't care
2. N/A: Not available or not applicable.
3. Setting the P10SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Ve_{REF+}/DAC0



If the reference of DAC0 is taken from pin Ve_{REF+}/DAC0, unpredictable voltage levels will be on pin. In this situation, the DAC0 output is fed back to its own reference input.

JTAG pins TMS, TCK, TDI/TCLK, TDO/TDI, input/output with Schmitt trigger or output



JTAG fuse check mode

MSP430 devices that have the fuse on the TDI/TCLK terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current ($I_{(TF)}$) of 1 mA at 3 V can flow from the TDI/TCLK pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if the TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current only flows when the fuse check mode is active and the TMS pin is in a low state (see Figure 37). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition). The JTAG pins are terminated internally and therefore do not require external termination.

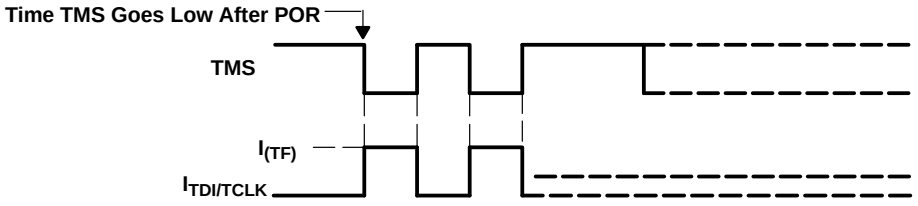


Figure 37. Fuse Check Mode Current

Data Sheet Revision History

Literature Number	Summary
SLAS508	Preliminary Product Preview datasheet release
SLAS508A	Production Data data sheet release
SLAS508B	Changed power consumption values in features (page 1)
SLAS508C	Changed $t_{VALID,MO}$, $t_{HD,SI}$, and $t_{VALID,SO}$ values (page 43)
SLAS508D	Changed $I_{(AM)}$ values for CG461x (page 29)
SLAS508E	Added ZQW package information Changed power consumption values for Standby and Off Modes in features (page 1) Corrected description of P7.3/UCA0CLK/S30 terminal (page 7) Clarified test conditions in recommended operating conditions table (page 30) Changed $I_{(AM)}$ values for CG461x and all TYP values for $I_{(LPM3)}$ in supply current into AV_{CC} + DV_{CC} table (page 31) Clarified test conditions in DCO table (page 42) Clarified test conditions in USART table (page 48) Clarified test conditions in operational amplifier OA, supply specifications table (page 59) Clarified test conditions in operational amplifier OA, input/output specifications table (page 60)
SLAS508F	Removed preview notice for MSP430CG461x in PZ package.
SLAS508G	Removed preview notice for all devices in ZQW package.
SLAS508H	Added “operational amplifier OA feedback network, noninverting amplifier mode (OAFCx = 4)” table and “operational amplifier OA feedback network, inverting amplifier mode (OAFCx = 6)” table (page 62)
SLAS508I	Changed limits on $t_{d(SVSon)}$ parameter (page 40)

NOTE: Page and figure numbers refer to the respective document revision.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
MSP430FG4616IPZ	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430FG4616IPZR	ACTIVE	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430FG4616IZQW	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	
MSP430FG4616IZQWR	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	
MSP430FG4616IZQWT	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	
MSP430FG4617IPZ	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430FG4617IPZR	ACTIVE	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430FG4617IZQW	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	
MSP430FG4617IZQWR	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	
MSP430FG4617IZQWT	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	
MSP430FG4618IPZ	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430FG4618IPZR	ACTIVE	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430FG4618IZQW	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
MSP430FG4618IZQWR	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	
MSP430FG4618IZQWT	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	
MSP430FG4619IPZ	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430FG4619IPZR	ACTIVE	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430FG4619IZQW	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	
MSP430FG4619IZQWR	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	
MSP430FG4619IZQWT	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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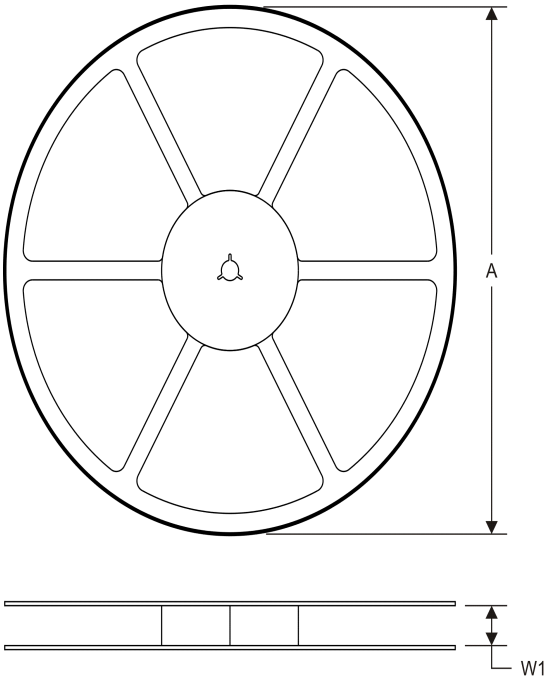
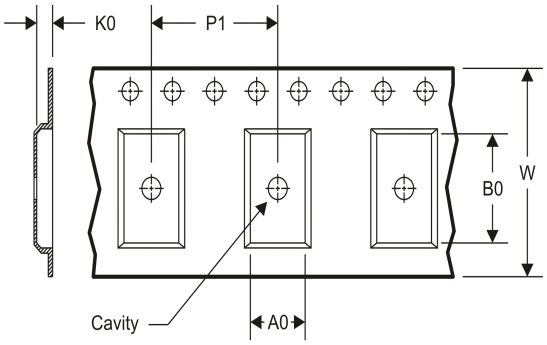
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

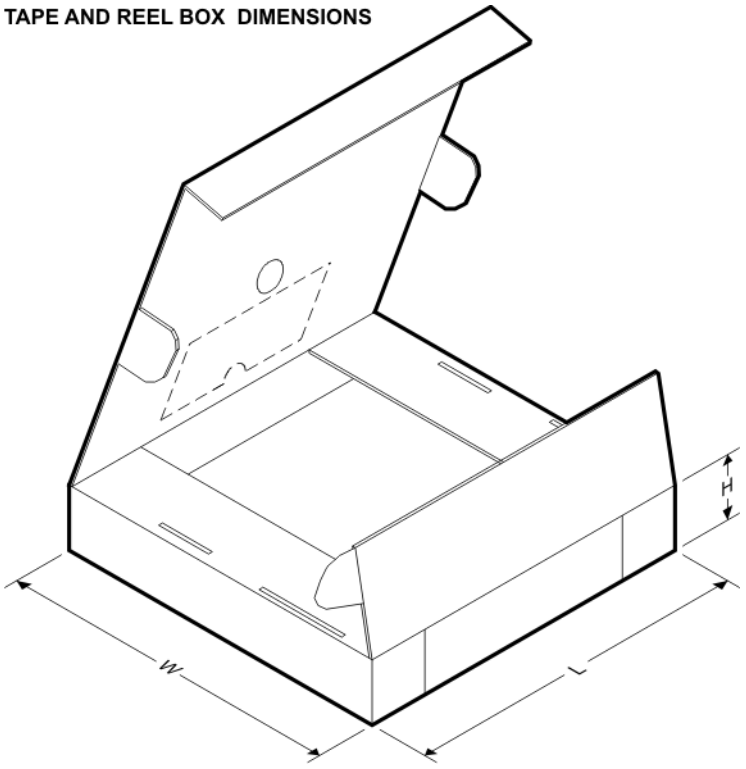
TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430FG4616IZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430FG4616IZQWT	BGA MICROSTAR JUNIOR	ZQW	113	250	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430FG4617IZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430FG4617IZQWT	BGA MICROSTAR JUNIOR	ZQW	113	250	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430FG4618IZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430FG4618IZQWT	BGA MICROSTAR JUNI	ZQW	113	250	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
	OR											
MSP430FG4619IZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430FG4619IZQWT	BGA MICROSTAR JUNIOR	ZQW	113	250	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

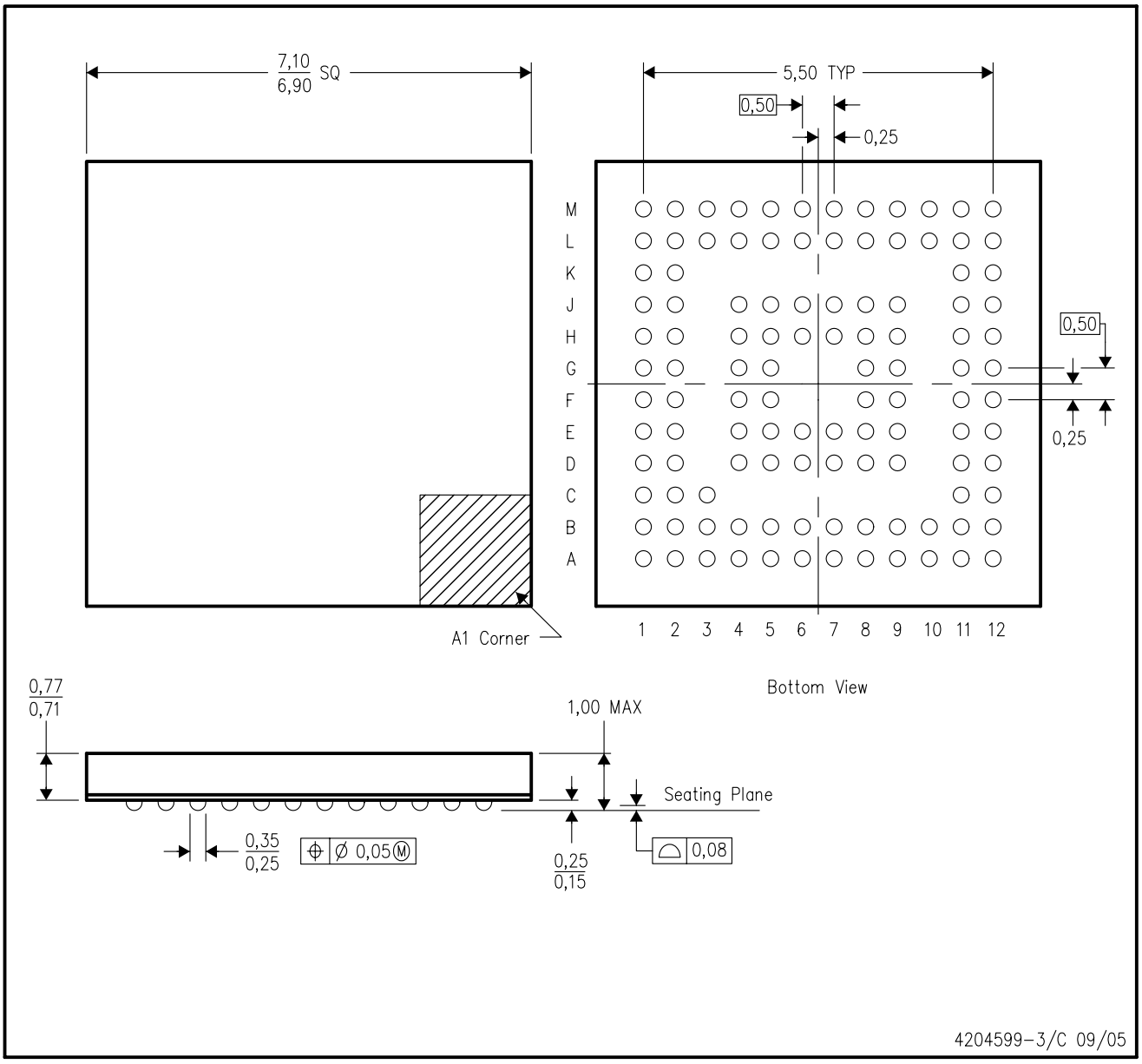


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430FG4616IZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	336.6	336.6	28.6
MSP430FG4616IZQWT	BGA MICROSTAR JUNIOR	ZQW	113	250	336.6	336.6	28.6
MSP430FG4617IZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	336.6	336.6	28.6
MSP430FG4617IZQWT	BGA MICROSTAR JUNIOR	ZQW	113	250	336.6	336.6	28.6
MSP430FG4618IZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	336.6	336.6	28.6
MSP430FG4618IZQWT	BGA MICROSTAR	ZQW	113	250	336.6	336.6	28.6

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
	JUNIOR						
MSP430FG4619IZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	336.6	336.6	28.6
MSP430FG4619IZQWT	BGA MICROSTAR JUNIOR	ZQW	113	250	336.6	336.6	28.6

ZQW (S–PBGA–N113) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225
D. This is a lead–free solder ball design.

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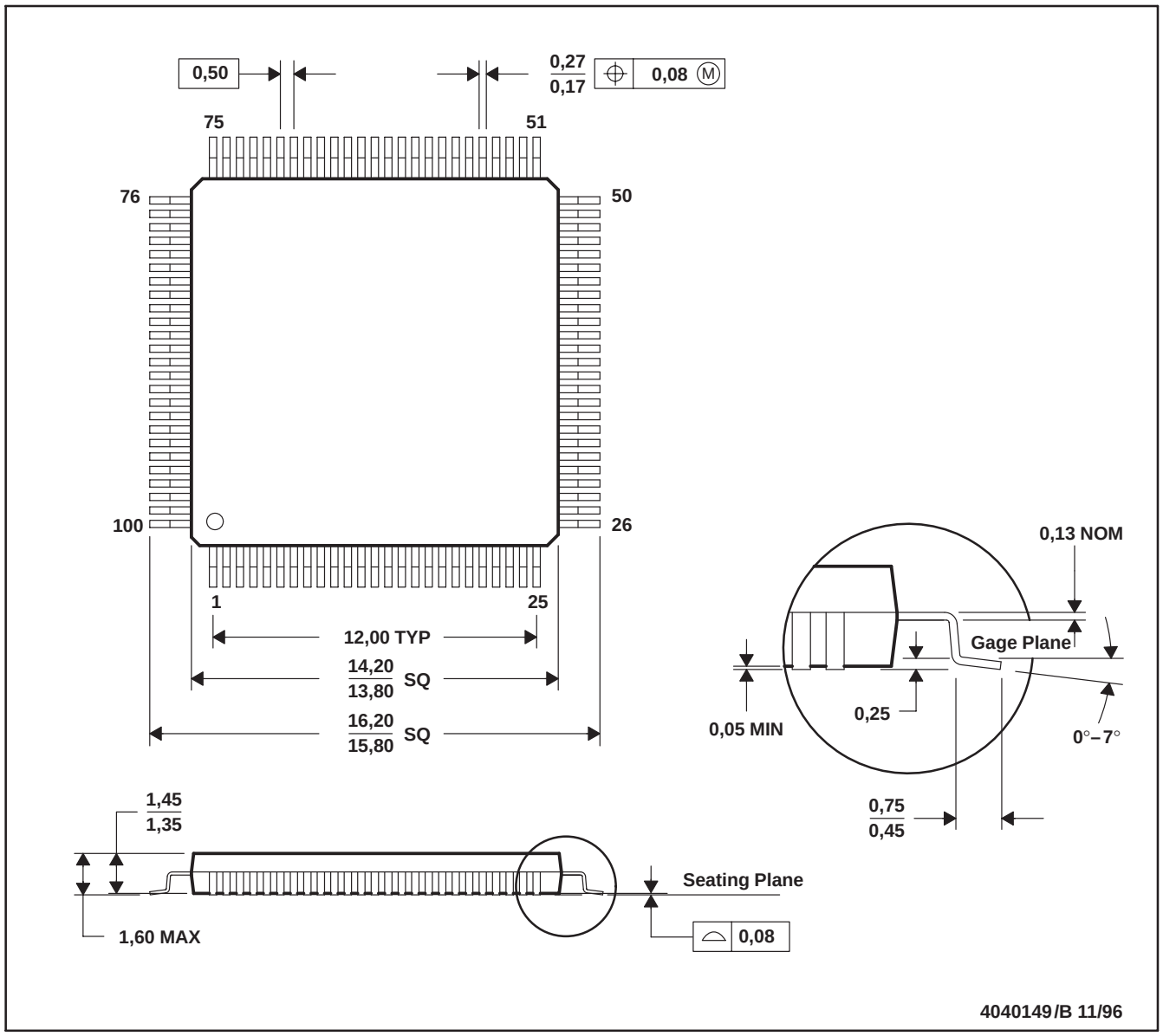
PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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