

# 74LS640, 74LS640-1 Transceiver

Inverting Octal Bus Transceiver (3-State)  
*Product Specification*

## Logic Products

### FEATURES

- Octal bidirectional bus interface
- Inverting 3-State buffer outputs
- PNP inputs for reduced loading
- Hysteresis on all Data inputs
- 48mA sink capability (LS640-1)

### DESCRIPTION

The LS640 is an octal transceiver featuring inverting 3-State bus compatible outputs in both send and receive directions. The outputs are all capable of sinking 24mA and sourcing up to 15mA, producing very good capacitive drive characteristics. In addition, the 74LS640-1 features a 48mA sink current capability. The device features a Chip Enable (CE) input for easy cascading and a Send/Receive (S/R) input for direction control. All Data inputs have hysteresis built in to minimize ac noise effects.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS640 & -1	7ns	58mA

### ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$ ; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS640N N74LS640-1N
Plastic SOL-20	N74LS640D

#### NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

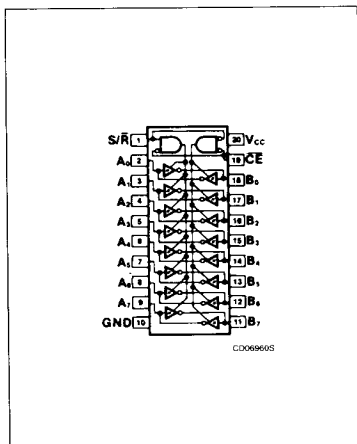
### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS & -1
All	Inputs	1LSul
All	Outputs	30LSul

#### NOTE:

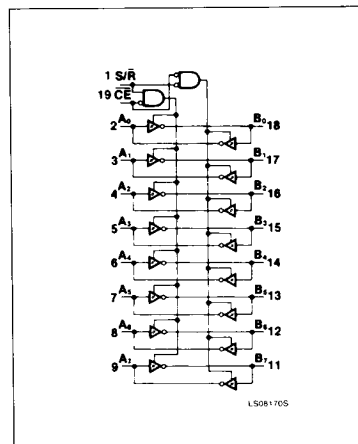
A 74LS unit load (LSul) is  $20\mu A$   $I_{IH}$  and  $-0.4mA$   $I_{IL}$ .

### PIN CONFIGURATION



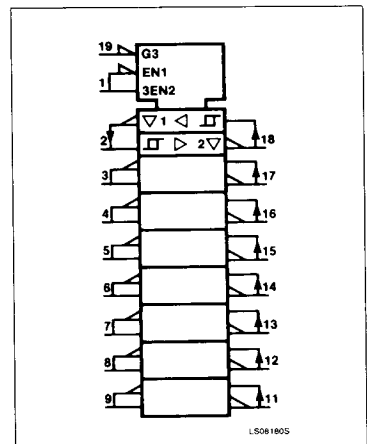
December 4, 1985

### LOGIC SYMBOL



5-597

### LOGIC SYMBOL (IEEE/IEC)



853-0425 81495

## Transceiver

74LS640, 74LS640-1

## FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{CE}$	S/ $\overline{R}$	$A_n$	$B_n$
L	L	$A = \overline{B}$	Inputs
L	H	Inputs	$B = \overline{A}$
H	X	(Z)	(Z)

H = HIGH voltage level  
 L = LOW voltage level  
 X = Don't care  
 (Z) = HIGH impedance "off" state

**ABSOLUTE MAXIMUM RATINGS** (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS & -1	UNIT
$V_{CC}$	Supply voltage	7.0	V
$V_{IN}$	Input voltage	-0.5 to +7.0	V
$I_{IN}$	Input current	-30 to +1	mA
$V_{OUT}$	Voltage applied to output in HIGH output state	-0.5 to $V_{CC}$	V
$T_A$	Operating free-air temperature range	0 to 70	°C

**NOTE**

$V_{IN}$  limited to 5.5V on A and B inputs only.

**RECOMMENDED OPERATING CONDITIONS**

PARAMETER		74LS & -1			UNIT
		Min	Nom	Max	
$V_{CC}$	Supply voltage	4.75	5.0	5.25	V
$V_{IH}$	HIGH-level input voltage	2.0			V
$V_{IL}$	LOW-level input voltage			+0.6	V
$I_{IK}$	Input clamp current			-18	mA
$I_{OH}$	HIGH-level output current			-15	mA
$I_{OL}$	LOW-level output current			24	mA
			74LS-1 only	48	mA
$T_A$	Operating free-air temperature	0		70	°C

# Transceiver

# 74LS640, 74LS640-1

## DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS <sup>1</sup>		74LS640			74LS640-1			UNIT
			Min	Typ <sup>2</sup>	Max	Min	Typ <sup>2</sup>	Max	
$\Delta V_T$ Hysteresis ( $V_{T+} - V_{T-}$ )	$V_{CC} = \text{MIN}$ , A or B input		0.2	0.4		0.2	0.4		V
$V_{OH}$ HIGH-level output voltage	$V_{CC} = \text{MIN}$ , $V_{IH} = \text{MIN}$ , $V_{IL} = \text{MAX}$	$I_{OH} = \text{MAX}$	2.0			2.0			V
		$I_{OH} = -3\text{mA}$	2.4	3.4		2.4	3.4		V
$V_{OL}$ LOW-level output voltage	$V_{CC} = \text{MIN}$ , $V_{IH} = \text{MIN}$ , $V_{IL} = \text{MAX}$	$I_{OL} = 12\text{mA}$		0.25	0.4		0.25	0.4	V
		$I_{OL} = 24\text{mA}$ (74LS)		0.35	0.5		0.35	0.5	V
		$I_{OL} = 48\text{mA}$ (74LS-1)					0.4	0.5	V
$V_{IK}$ Input clamp voltage	$V_{CC} = \text{MIN}$ , $I_I = I_{IK}$				-1.5			-1.5	V
$I_{OZH}$ Off-state output current, HIGH-level voltage applied	$V_{CC} = \text{MAX}$ , $\overline{CE}$ input = 2.0V, $V_O = 2.7\text{V}$				20			20	$\mu\text{A}$
$I_{OZL}$ Off-state output current, LOW-level voltage applied	$V_{CC} = \text{MAX}$ , $\overline{CE}$ input = 2.0V, $V_O = 0.4\text{V}$				-400			-400	$\mu\text{A}$
$I_I$ Input current at maximum input voltage	$V_{CC} = \text{MAX}$	$V_I = 5.5\text{V}$ A or B input			0.1			0.1	$\text{mA}$
		$V_I = 7.0\text{V}$ S/ $\overline{R}$ or $\overline{CE}$ input			0.1			0.1	$\text{mA}$
$I_{IH}$ HIGH-level input current	$V_{CC} = \text{MAX}$ , $V_I = 2.7\text{V}$				20			20	$\mu\text{A}$
$I_{IL}$ LOW-level input current	$V_{CC} = \text{MAX}$ , $V_I = 0.4\text{V}$				-0.4			-0.4	$\text{mA}$
$I_{OS}$ Short-circuit output current <sup>3</sup>	$V_{CC} = \text{MAX}$		-40		-130	-40		-130	$\text{mA}$
$I_{CC}$ Supply current <sup>4</sup> (total)	$V_{CC} = \text{MAX}$	$I_{CCH}$ Outputs HIGH		48	70		48	70	$\text{mA}$
		$I_{CCL}$ Outputs LOW		62	90		62	90	$\text{mA}$
		$I_{CCZ}$ Outputs OFF		64	95		64	95	$\text{mA}$

**NOTES:**

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^\circ\text{C}$ .
3.  $I_{OS}$  is tested with  $V_{OUT} = +0.5\text{V}$  and  $V_{CC} = V_{CC} \text{ MAX} + 0.5\text{V}$ . Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure  $I_{CC}$  with outputs open.

5

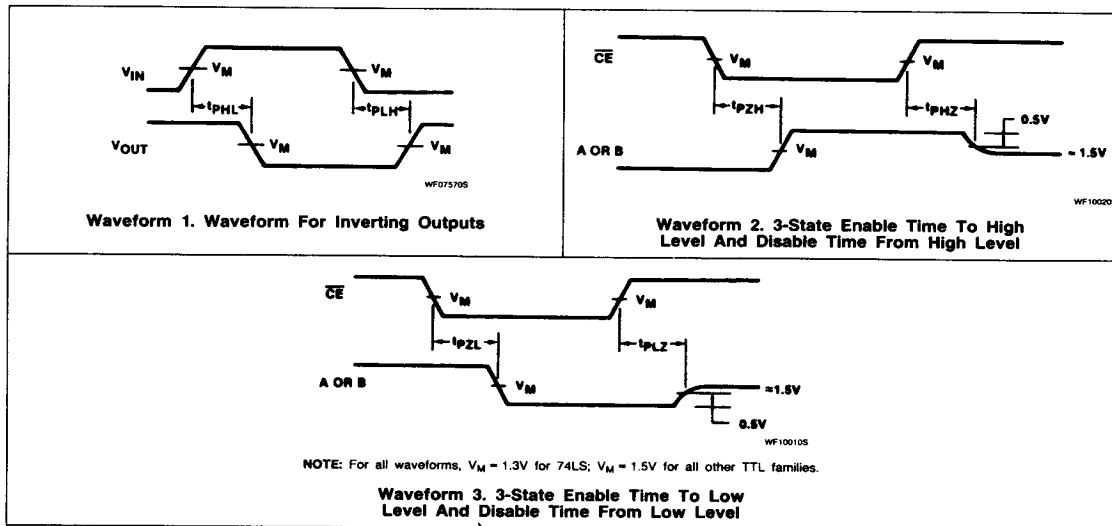
# Transceiver

# 74LS640, 74LS640-1

## AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ , $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74LS & -1		UNIT
		$C_L = 45\text{pF}$ , $R_L = 667\Omega$		
		Min	Max	
$t_{PLH}$ $t_{PHL}$	Propagation delay A input to B output	Waveform 1	10 15	ns
$t_{PLH}$ $t_{PHL}$	Propagation delay B input to A output	Waveform 1	10 15	ns
$t_{PZH}$	Enable to HIGH $\overline{CE}$ , $S/\overline{R}$ inputs to A output	Waveform 2	40	ns
$t_{PZH}$	Enable to HIGH $\overline{CE}$ , $S/\overline{R}$ inputs to B output	Waveform 2	40	ns
$t_{PZL}$	Enable to LOW $\overline{CE}$ , $S/\overline{R}$ inputs to A output	Waveform 3	40	ns
$t_{PZL}$	Enable to LOW $\overline{CE}$ , $S/\overline{R}$ inputs to B output	Waveform 3	40	ns
$t_{PHZ}$	Disable from HIGH $\overline{CE}$ , $S/\overline{R}$ inputs to A output	Waveform 2, $C_L = 5\text{pF}$	25	ns
$t_{PHZ}$	Disable from HIGH $\overline{CE}$ , $S/\overline{R}$ inputs to B output	Waveform 2, $C_L = 5\text{pF}$	25	ns
$t_{PLZ}$	Disable from LOW $\overline{CE}$ , $S/\overline{R}$ inputs to A output	Waveform 3, $C_L = 5\text{pF}$	25	ns
$t_{PLZ}$	Disable from LOW $\overline{CE}$ , $S/\overline{R}$ inputs to B output	Waveform 3, $C_L = 5\text{pF}$	25	ns

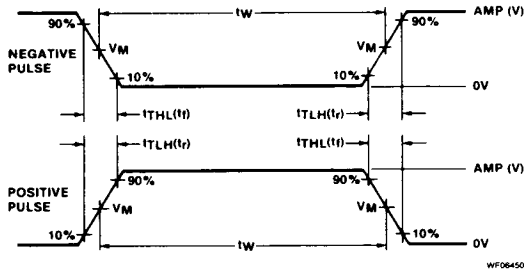
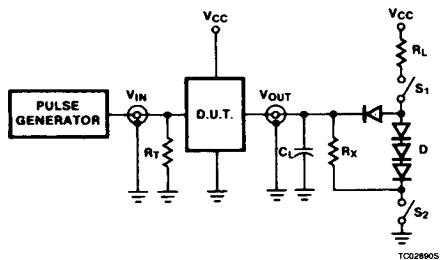
## AC WAVEFORMS



# Transceiver

# 74LS640, 74LS640-1

## TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$  for 74LS;  $V_M = 1.5V$  for all other TTL families.

### Input Pulse Definition

### Test Circuit For 3-State Outputs

### SWITCH POSITION

TEST	SWITCH 1	SWITCH 2
$t_{PZH}$	Open	Closed
$t_{PZL}$	Closed	Open
$t_{PHZ}$	Closed	Closed
$t_{PLZ}$	Closed	Closed

### DEFINITIONS

$R_L$  = Load resistor to  $V_{CC}$ ; see AC CHARACTERISTICS for value.

$C_L$  = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

$R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

$R_X = 1k\Omega$  for 74, 74S,  $R_X = 5k\Omega$  for 74LS.

$t_{LH}$ ,  $t_{HL}$  Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	$t_{TLH}$	$t_{THL}$
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns