

NE564 Series – Phase Locked Loop

GENERAL DESCRIPTION

The NE564 is a versatile, high frequency Phase Locked Loop designed for operation up to 50MHz. As shown in the block diagram, the NE564 consists of a VCO, limiter, phase comparator, and post detection processor.

The NE564 is a monolithic phase locked loop with a post detection processor. The use of Schottky clamped transistors and optimized device geometries extends the frequency of operation to 50MHz. In addition to the classical PLL applications, the NE564 can be used as a modulator with a controllable frequency deviation.

The output voltage of the PLL can be written as shown in the following equation:

$$V_O = \frac{(f_{in} - f_O)}{KVCO}$$

$KVCO$ = conversion gain of the VCO
 f_{in} = frequency of the input signal
 f_O = free running frequency of the VCO

The process of recovering FSK signals involves the conversion of the PLL output into digital, logic compatible signals. For high data rates, a considerable amount of carrier

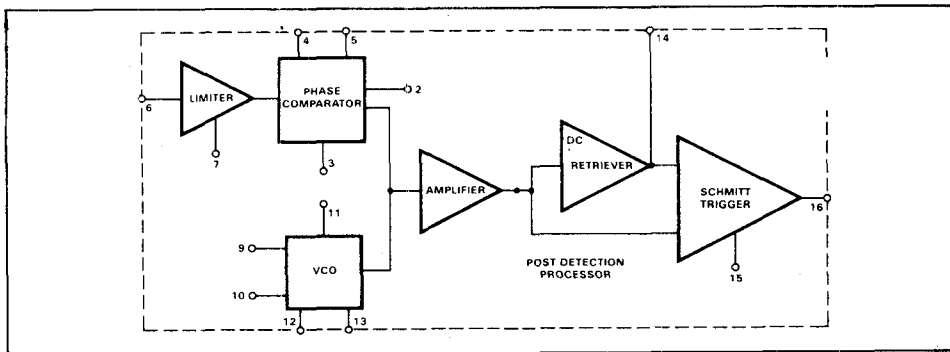
FEATURES

- Operation with single 5V supply
- TTL compatible inputs and outputs
- Operation to 50MHz
- Operates as a modulator
- External loop gain control
- Reduced carrier feedthrough
- No elaborate filtering needed in FSK applications

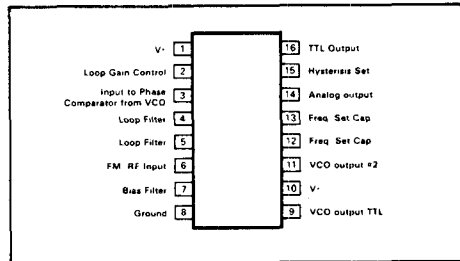
APPLICATIONS

- High speed modems
- FSK receivers and transmitters
- Frequency synthesizers
- Signal generators

BLOCK DIAGRAM



CONNECTION DIAGRAM



ABSOLUTE MAXIMUM RATINGS

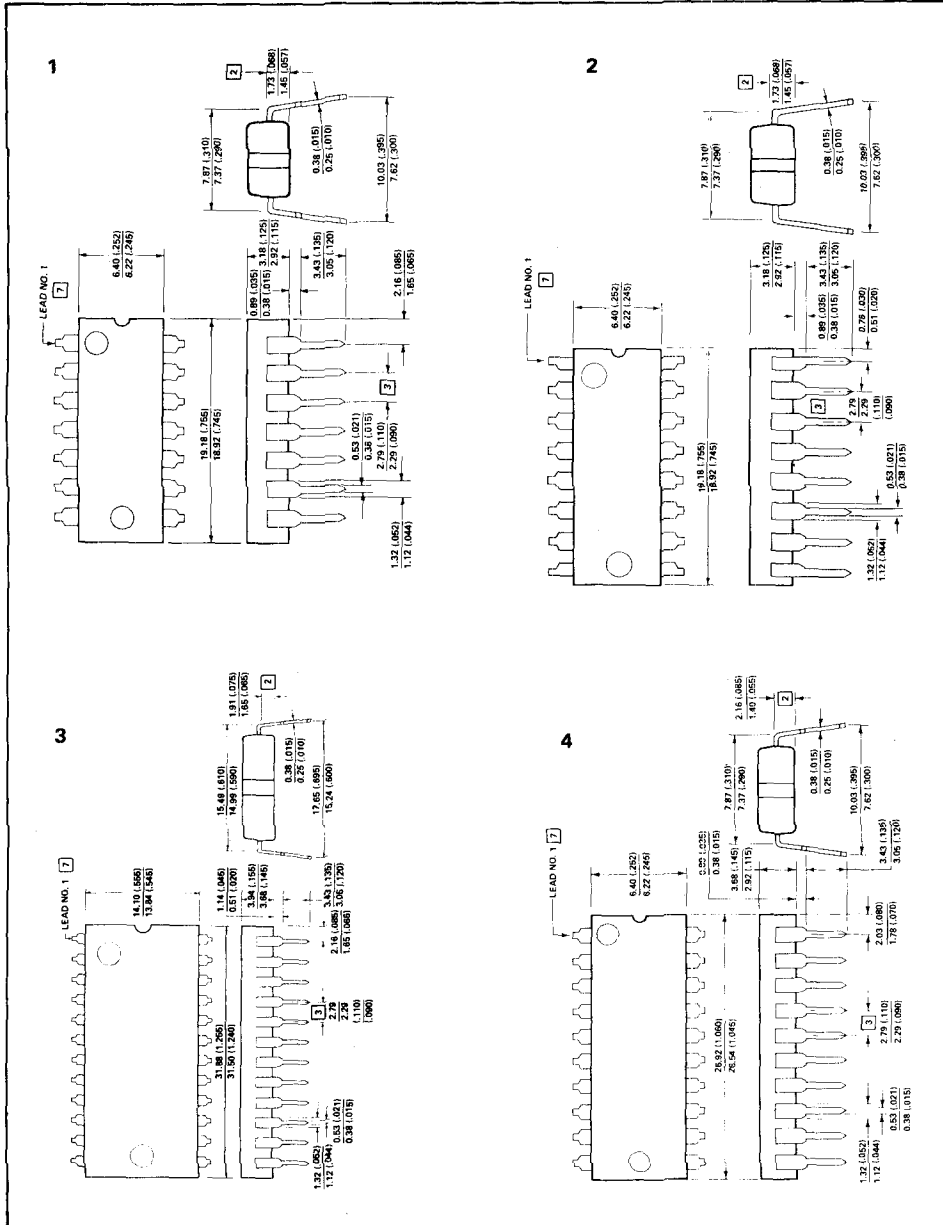
| PARAMETER | RATING | UNIT |
|-----------|-----------------------|---------------|
| V+ | Supply voltage | V |
| | Pin 1 | 14 |
| | Pin 10 | 6 |
| P_D | Power dissipation | 400 mW |
| T_A | Operating temperature | 0 to 70 °C |
| t_{stg} | Storage temperature | -65 to 150 °C |

REFERENCE TABLE

| TYPE NO. | STOCK NO. | OUTLINE DRWG. NO. |
|----------|-----------|-------------------|
| NE564N | 56046B | 2 |

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AND MANUFACTURERS PART NO. WHEN ORDERING

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Outline Drawings



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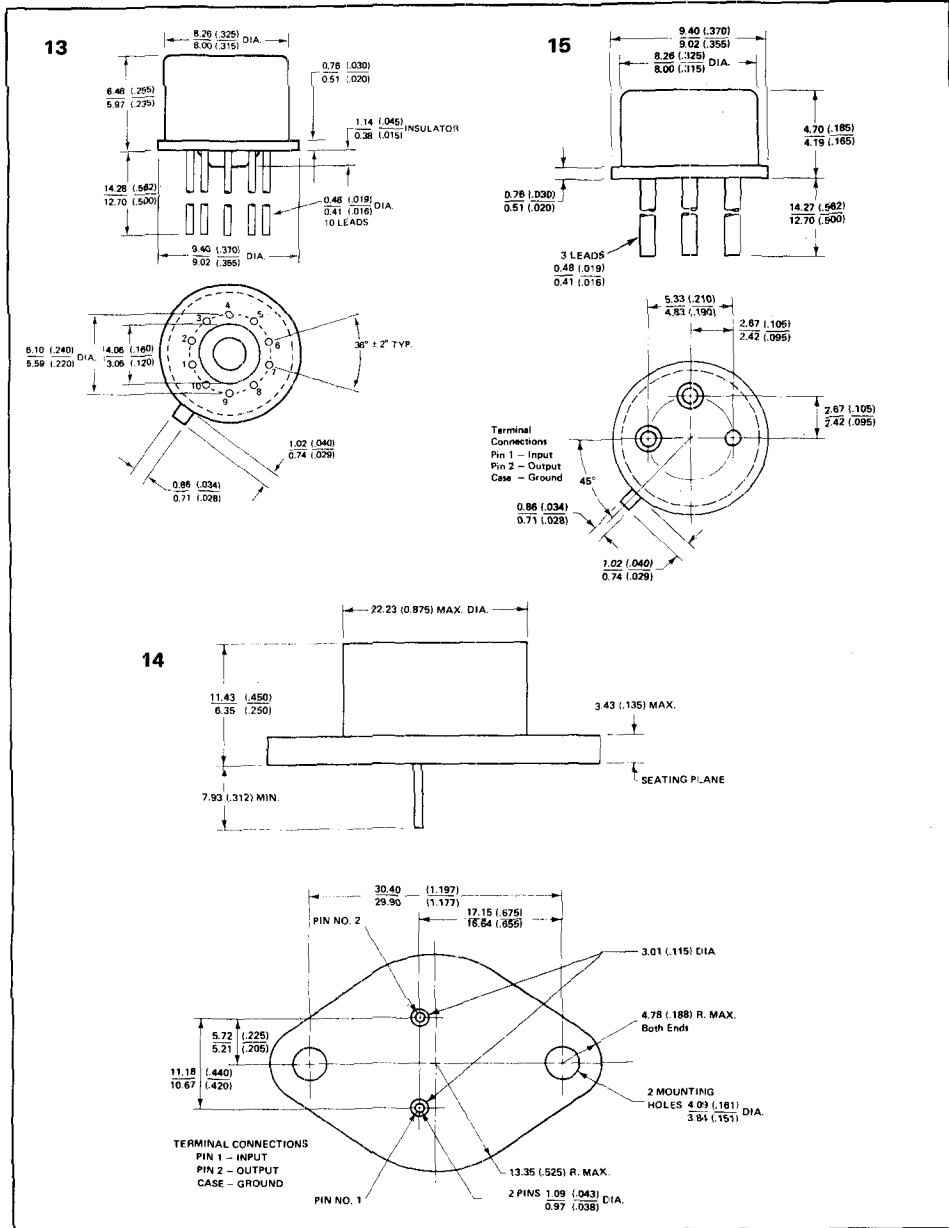


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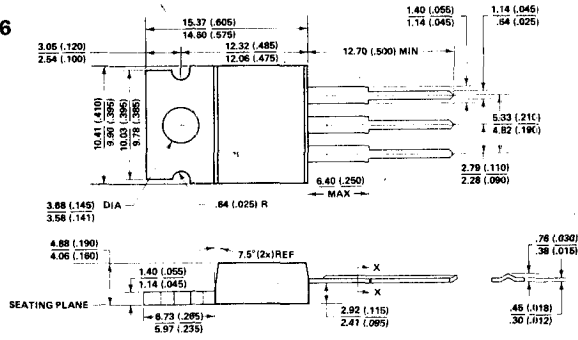
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