SN54159, SN74159 4-LINE TO 16-LINE DECODERS/DEMULTIPLEXERS WITH OPEN-COLLECTOR OUTPUTS

SDLS059

DECEMBER 1972 - REVISED MARCH 1988

- Open-Collector Outputs for Interfacing with MOS or Memory Decoders/Drivers
- Decodes 4 Binary-Coded Inputs into One of 16 Mutually Exclusive Outputs
- Performs the Demultiplexing Function by Distributing Data from One Input Line to Any One of 16 Outputs
- Typical Average Propagation Delay Times:
 24 ns through 3 levels of Logic
 19 ns from Strobe Input
- Output Off-State Current is Less Than 50 μA
- Fully Compatible with Most TTL and MSI Circuits

SN54159 . . . J OR W PACKAGE SN74159 ... N PACKAGE (TOP VIEW) U24∏ VCC 1 🗆 2 23 A 22 B 2 🗍 3 21 C 3 □4 20 D 19 G2 5 18∐ G1 6 17 15 8 7 14 16 9 15 13 10 14 12 11 GND ∏12 13 11

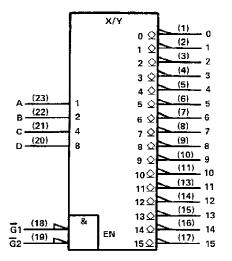
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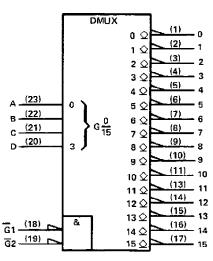
Each of these monolithic, 4-line-to-16 line decoders utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive open-collector outputs when both the strobe inputs, $\overline{G}1$ and $\overline{G}2$, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are ideally suited for implementing MOS memory decoding or for interfacing with discrete memory address drivers. For ultra-high-speed applications, the SN54S138/SN74S138 or SN54S139/SN74S139 is recommended.

These circuits are fully compatible for use with most other TTL circuits. Input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design. Input buffers are used to lower the fan-in requirement to only one normalized Series 54/74 load. A fan-out to 10 normalized Series 54/74 loads in the low-level state is available from each of the sixteen outputs. Typical power dissipation is 170 mW.

The SN54159 is characterized for operation over the full military temperature range of -55° C to 125° C; the SN74159 is characterized for operation from 0° C to 70° C.

logic symbols (alternatives)†





[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



SN54159, SN74159 4-LINE TO 16-LINE DECODERS/DEMULTIPLEXERS WITH OPEN-COLLECTOR OUTPUTS

	FUNCTION TABLE																				
		INP	UTS										OUT	PUTS					•		
Ğ1	Ğ2	D	С	В	Д	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	ᆫ	L	L	L	Ļ	L	Н	++	Н	Н	Н	Н	Н	H	Н	H	Н	Н	Н	H	н
L	L	L	L	L	Н	н	L	Н	н	Н	Н	Н	Н	Н	Н	Н	н	Н	H	Н	н
L	L	L	L	н	Ł	н	H	L	Н	Н	Н	Н	н	н	н	н	H	н	Н	Н	н
L	L	L	L	Н	Н	н	H	Н	L	Н	Н	Н	Н	Н	Н	н	н	н	н	н	н
L	L	L	Н	L	L	н	Н	Н	Н	L	Н	Н	H	н	н	н	H	н	н	н	н
L	L	L	Н	L	Н	н	Н	Н	H	Н	L	Н	H	Н	Н	H	H	H	Н	Н	н
L	L	L	Н	Н	L	н	Н	Н	Н	Н	Н	L	н	Н	H	Н	Н	н	н	н	н
L	L	L	н	Н	•н	н	н	Н	н	н	H	Н	L	Н	н	н	Н	Н	Н	Н	н
L	Ļ	н	L	L	L	H	Н	H	H	Н	н	Н	H	L	н	H	H	н	Н	Н	н
L	L	н	L	L	Н	н	Н	Н	н	Н	H	н	Н	Н	L	Н	Н	н	Н	Н	н
L	L	Н	L	Н	L	Н	Н	Н	н	H	H	Н	н	н	H	L	н	Н	Н	Н	н
L	L	H	L	Н	н	Н	Н	Н	н	н	H	н	н	Н	Н	Н	L	Н	н	н	н
L	Ł	H	Н	L	Ļ	Н	Н	Н	Н	H	Н	H	Н	Н	Н	Н	Н	L	Н	Н	н
L	L	H	Н	L	н	н	Н	н	H	н	Н	Н	н	Н	н	Н	Н	Н	L	н	н
L.	ŧ.	н	Н	Н	L	н	Н	Н	Н	Н	н	Н	н	Н	н	Н	Н	Н	Н	L	н
L	١	Н	Н	Н	Н	Н	Н	H	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	н	L,
L	н	х	×	×	×	Н	Н	н	Н	Н	Н	Н	Н	Н	Н	н	Н	Н	H	Н	н
Н	L	×	Х	Х	х	Н	Н	H	Н	Н	н	Н	Н	H	Н	Н	Н	Н	H	Н	н
Н	н	X	Х	Х	X	Н_	<u> </u>	Н.	_H	Н	Н	Н	Н	н	Н	<u> </u>	Н	н	н	н	Н

H = high level, L = low level, X = irrelevant

logic diagram

Same as SN54154, SN74154.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)		7 V
Input voltage		ōν
Off-state output voltage		
Operating free-air temperature range: SN54159 Circuits		
SN74159 Circuits	0°C to 70	ງ°c
Storage temperature range)°C

NOTE 1: Voltage values are with respect to network ground terminal,



recommended operating conditions

		SN5415	9		SN7415	9	
	MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, V _{CC}	4.5	5	5.5	4.75	5	5.25	V
Low-level autput current, IQL			16			16	mA
Operating free-air temperature, T _A	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS [†]	MIN	TYP# 1	MAX	UNIT
VIH	High-level input voltage		2			٧
VIL	Low-level input voltage		-		8.0	V
VIK	Input clamp voltage	V _{CC} = MIN, I ₁ = -12 mA			-1.5	V
Юн	High-level output current	V _{CC} = MIN, V _{IH} - 2 V, V _{IL} = 0.8 V, V _{OH} = 5.5 V			50	μА
VOL	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA			0.4	٧
Н	Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V		***	1	mΑ
Ιιн	High-level input current	V _{CC} = MAX, V ₁ = 2.4 V	- -		40	μД
ηL	Low-level input current	V _{CC} = MAX, V ₁ = 0.4 V			-1.6	mА
Icc	Supply current	V _{CC} = MAX, All inputs grounded		34	56	mΑ

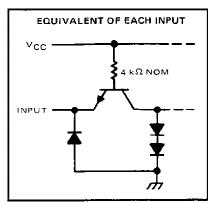
[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type. \ddagger AII typical values are at $V_{CC} = 5 \text{ V}$, $T_{\Delta} = 25^{\circ}\text{ C}$.

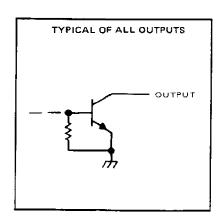
switching characteristics, VCC = 5 V, T_A = 25 $^{\circ}$ C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
tPLH	Propagation delay time, low-to-high-level output, from A, B, C, or D inputs through 3 levels of logic		23	36	ns	
¹PHŁ	Propagation delay time, high-to-low-level output, from A, B, C, or D inputs through 3 levels of logic	C ₁ - 15 pF, R ₁ = 400 Ω, See Note 2		24	36	ns
₹PLH	Propagation delay time, low-to-high-level output, from either strobe input	O[- 15 pr, N[- 400 32, 388 NOTE 2		15	25	ns
1PHL	Propagation delay time, high-to-low-level output, from either strobe input			22	36	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

schematics of inputs and outputs







PACKAGE OPTION ADDENDUM

17-May-2014

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
SN74159N	ACTIVE	PDIP	N	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74159N	Samples
SN74159NE4	ACTIVE	PDIP	N	24		TBD	Call TI	Call TI	0 to 70		Samples
SN74159NE4	ACTIVE	PDIP	N	24		TBD	Call TI	Call TI	0 to 70		Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE OPTION ADDENDUM

17-May-2014

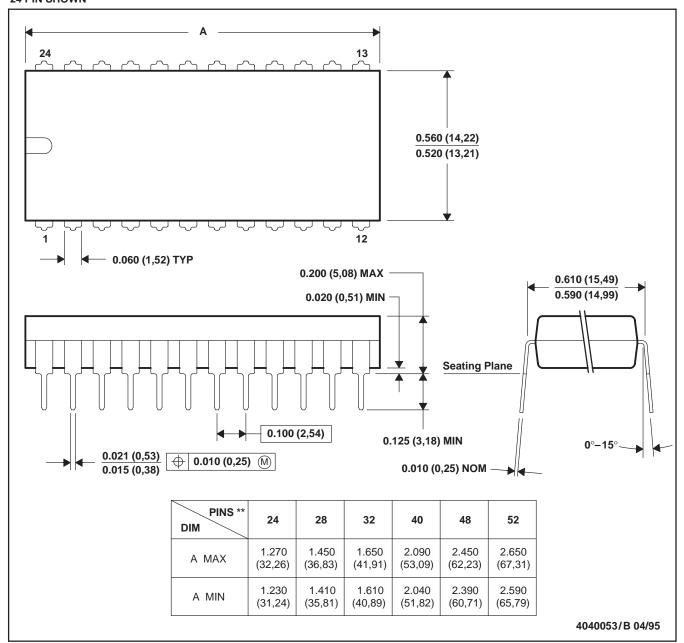
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N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

24 PIN SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-011
- D. Falls within JEDEC MS-015 (32 pin only)



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