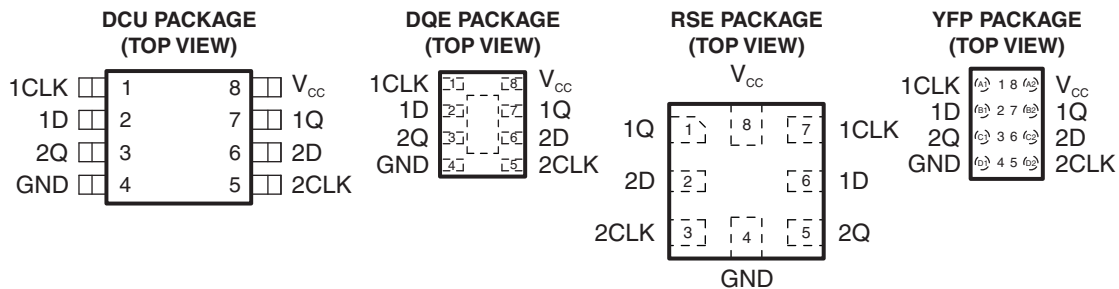


LOW-POWER DUAL POSITIVE EDGE-TRIGGERED D-TYPE FLIP-FLOP

Check for Samples: [SN74AUP2G79](#)

FEATURES

- Available in the Texas Instruments NanoStar™ Package
- Low Static-Power Consumption ($I_{CC} = 0.9 \mu\text{A}$ Maximum)
- Low Dynamic-Power Consumption ($C_{pd} = 3 \text{ pF}$ Typ at 3.3 V)
- Low Input Capacitance ($C_i = 1.5 \text{ pF}$ Typical)
- Low Noise – Overshoot and Undershoot <math><10\%</math> of V_{CC}
- I_{off} Supports Partial-Power-Down Mode Operation
- Wide Operating V_{CC} Range of 0.8 V to 3.6 V
- Optimized for 3.3-V Operation
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- $t_{pd} = 4 \text{ ns}$ Maximum at 3.3 V
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static- and dynamic-power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in increased battery life (see [Figure 1](#)). This product also maintains excellent signal integrity (see the very low undershoot and overshoot characteristics shown in [Figure 2](#)).

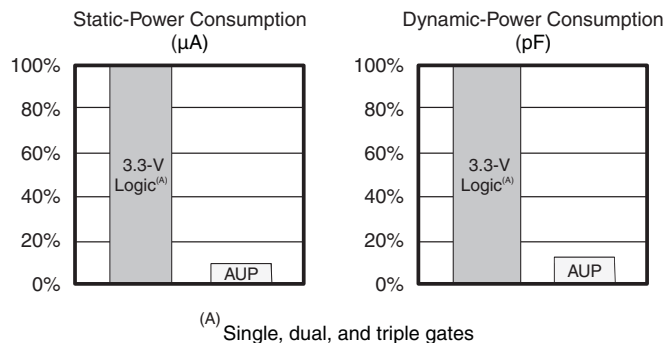

^(A) Single, dual, and triple gates

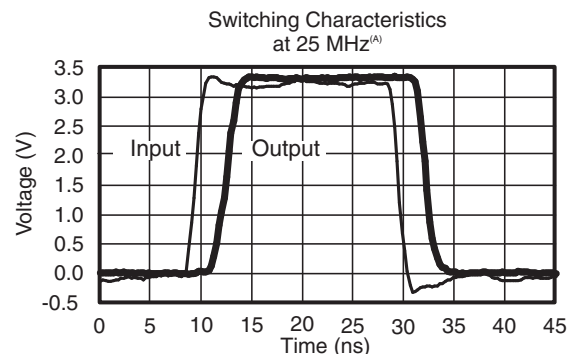
Figure 1. AUP – The Lowest-Power Family

^(A) SN74AUP2Gxx data at $C_L = 15 \text{ pF}$.

Figure 2. Excellent Signal Integrity


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoStar is a trademark of Texas Instruments.

When data at the data (D) input meets the setup time requirement, the data is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION⁽¹⁾

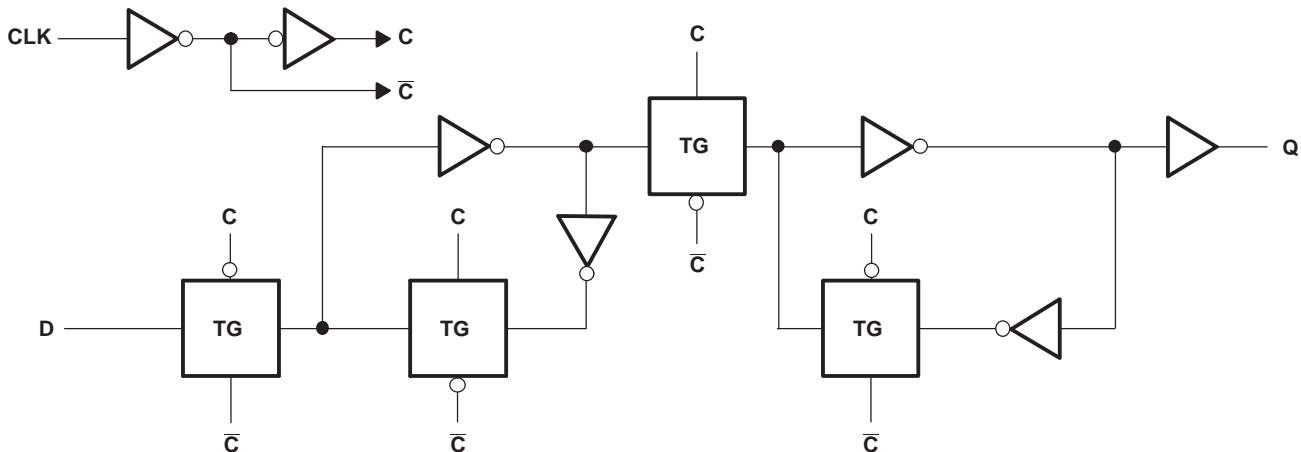
T _A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽³⁾
-40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YFP (Pb-free)	Reel of 3000	SN74AUP2G79YFPR	_ _ H W _
	uQFN – DQE	Reel of 5000	SN74AUP2G79DQER	PT
	QFN – RSE	Reel of 5000	SN74AUP2G79RSEER	PT
	SSOP – DCU	Reel of 3000	SN74AUP2G79DCUR	H79_

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
- (3) DCU: The actual top-side marking has one additional character that designates the wafer fab/assembly site.
YFP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate wafer fab/assembly site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

FUNCTION TABLE

INPUTS		OUTPUT
CLK	D	Q
↑	H	H
↑	L	L
L	X	Q ₀
H	X	Q ₀

LOGIC DIAGRAM, EACH FLIP-FLOP (POSITIVE LOGIC)



Pin numbers shown are for the DCU and DQE packages.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	4.6	V
V_I	Input voltage range ⁽²⁾	-0.5	4.6	V
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	4.6	V
V_O	Output voltage range in the high or low state ⁽²⁾	-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$	-50	mA
I_{OK}	Output clamp current	$V_O < 0$	-50	mA
I_O	Continuous output current		±20	mA
	Continuous current through V_{CC} or GND		±50	mA
θ_{JA}	Package thermal impedance ⁽³⁾	DCU package	220	°C/W
		DQE package	261	
		RSE package	253	
		YFP package	132	
T_{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JEDEC 51-7.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	0.8	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 0.8 V	V _{CC}	V
		V _{CC} = 1.1 V to 1.95 V	0.65 × V _{CC}	
		V _{CC} = 2.3 V to 2.7 V	1.6	
		V _{CC} = 3 V to 3.6 V	2	
V _{IL}	Low-level input voltage	V _{CC} = 0.8 V	0	V
		V _{CC} = 1.1 V to 1.95 V	0.35 × V _{CC}	
		V _{CC} = 2.3 V to 2.7 V	0.7	
		V _{CC} = 3 V to 3.6 V	0.9	
V _I	Input voltage	0	3.6	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 0.8 V	–20	μA
		V _{CC} = 1.1 V	–1.1	
		V _{CC} = 1.4 V	–1.7	
		V _{CC} = 1.65 V	–1.9	
		V _{CC} = 2.3 V	–3.1	
		V _{CC} = 3 V	–4	
I _{OL}	Low-level output current	V _{CC} = 0.8 V	20	μA
		V _{CC} = 1.1 V	1.1	
		V _{CC} = 1.4 V	1.7	
		V _{CC} = 1.65 V	1.9	
		V _{CC} = 2.3 V	3.1	
		V _{CC} = 3 V	4	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 0.8 V to 3.6 V	200	ns/V
T _A	Operating free-air temperature	–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			T _A = –40°C to 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V _{OH}	I _{OH} = –20 μA	0.8 V to 3.6 V	V _{CC} – 0.1			V _{CC} – 0.1		V
	I _{OH} = –1.1 mA	1.1 V	0.75 × V _{CC}			0.7 × V _{CC}		
	I _{OH} = –1.7 mA	1.4 V	1.11			1.03		
	I _{OH} = –1.9 mA	1.65 V	1.32			1.3		
	I _{OH} = –2.3 mA	2.3 V	2.05			1.97		
	I _{OH} = –3.1 mA		1.9			1.85		
	I _{OH} = –2.7 mA	3 V	2.72			2.67		
	I _{OH} = –4 mA		2.6			2.55		
V _{OL}	I _{OL} = 20 μA	0.8 V to 3.6 V	0.1			0.1		V
	I _{OL} = 1.1 mA	1.1 V	0.3 × V _{CC}			0.3 × V _{CC}		
	I _{OL} = 1.7 mA	1.4 V	0.31			0.37		
	I _{OL} = 1.9 mA	1.65 V	0.31			0.35		
	I _{OL} = 2.3 mA	2.3 V	0.31			0.33		
	I _{OL} = 3.1 mA		0.44			0.45		
	I _{OL} = 2.7 mA	3 V	0.31			0.33		
	I _{OL} = 4 mA		0.44			0.45		
I _I	A or B input	V _I = GND to 3.6 V	0 V to 3.6 V			0.1	0.5	μA
I _{off}		V _I or V _O = 0 V to 3.6 V	0 V			0.2	0.6	μA
ΔI _{off}		V _I or V _O = 0 V to 3.6 V	0 V to 0.2 V			0.2	0.6	μA
I _{CC}		V _I = GND or (V _{CC} to 3.6 V), I _O = 0	0.8 V to 3.6 V			0.5	0.9	μA
ΔI _{CC}		V _I = V _{CC} – 0.6 V ⁽¹⁾ , I _O = 0	3.3 V			40	50	μA
C _i		V _I = V _{CC} or GND	0 V			1.5		pF
			3.6 V			1.5		
C _o		V _O = GND	0 V			3		pF

 (1) One input at V_{CC} – 0.6 V, other input at V_{CC} or GND

TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 4](#))

		V _{CC}	T _A = 25°C	T _A = -40°C to 85°C	UNIT
			TYP	MIN	
f _{clock}	Clock frequency	0.8 V		20	MHz
		1.2 V ± 0.1 V		80	
		1.5 V ± 0.1 V		100	
		1.8 V ± 0.15 V		140	
		2.5 V ± 0.2 V		210	
		3.3 V ± 0.3 V		260	
t _w	Pulse duration, CLK high or low	0.8 V		4.8	ns
		1.2 V ± 0.1 V		2.2	
		1.5 V ± 0.1 V		1.5	
		1.8 V ± 0.15 V		1.6	
		2.5 V ± 0.2 V		1.7	
		3.3 V ± 0.3 V		1.9	
t _{su}	Data high	0.8 V	2.9	4.2	ns
		1.2 V ± 0.1 V		1.4	
		1.5 V ± 0.1 V		1	
		1.8 V ± 0.15 V		0.9	
		2.5 V ± 0.2 V		0.7	
		3.3 V ± 0.3 V		0.6	
	Data low	0.8 V	3.5	5.3	
		1.2 V ± 0.1 V		1.8	
		1.5 V ± 0.1 V		1.2	
		1.8 V ± 0.15 V		1.1	
		2.5 V ± 0.2 V		1	
		3.3 V ± 0.3 V		1	
t _h	Hold time, data after CLK↑	0.8 V	0	0	ns
		1.2 V ± 0.1 V		0	
		1.5 V ± 0.1 V		0	
		1.8 V ± 0.15 V		0	
		2.5 V ± 0.2 V		0	
		3.3 V ± 0.3 V		0	

SWITCHING CHARACTERISTICS

 over recommended operating free-air temperature range, $C_L = 5$ pF (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{\max}			0.8 V		93		90		MHz
			$1.2\text{ V} \pm 0.1\text{ V}$		199		220		
			$1.5\text{ V} \pm 0.1\text{ V}$		250		230		
			$1.8\text{ V} \pm 0.15\text{ V}$		271		240		
			$2.5\text{ V} \pm 0.2\text{ V}$		280		250		
			$3.3\text{ V} \pm 0.3\text{ V}$		280		260		
t_{pd}	CLK	Q	0.8 V		15.9				ns
			$1.2\text{ V} \pm 0.1\text{ V}$	3.7	6.9	11	2.6	13.1	
			$1.5\text{ V} \pm 0.1\text{ V}$	3	4.8	7.6	2	8.8	
			$1.8\text{ V} \pm 0.15\text{ V}$	2.4	3.8	6.1	1.5	7.1	
			$2.5\text{ V} \pm 0.2\text{ V}$	1.8	2.7	4.4	1.1	5	
			$3.3\text{ V} \pm 0.3\text{ V}$	1.5	2.1	3.6	0.9	4	

SWITCHING CHARACTERISTICS

 over recommended operating free-air temperature range, $C_L = 10$ pF (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{\max}			0.8 V		62		50		MHz
			$1.2\text{ V} \pm 0.1\text{ V}$		147		160		
			$1.5\text{ V} \pm 0.1\text{ V}$		189		200		
			$1.8\text{ V} \pm 0.15\text{ V}$		180		240		
			$2.5\text{ V} \pm 0.2\text{ V}$		260		250		
			$3.3\text{ V} \pm 0.3\text{ V}$		280		260		
t_{pd}	CLK	Q	0.8 V		18				ns
			$1.2\text{ V} \pm 0.1\text{ V}$	4.3	7.8	12.3	3.2	14.4	
			$1.5\text{ V} \pm 0.1\text{ V}$	3.5	5.5	8.4	2.5	9.8	
			$1.8\text{ V} \pm 0.15\text{ V}$	2.8	4.4	6.8	1.9	8	
			$2.5\text{ V} \pm 0.2\text{ V}$	2.2	3.2	5	1.5	5.7	
			$3.3\text{ V} \pm 0.3\text{ V}$	1.8	2.6	4.1	1.3	4.5	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L = 15$ pF (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{\max}			0.8 V	48			30		MHz
			$1.2\text{ V} \pm 0.1\text{ V}$	112			120		
			$1.5\text{ V} \pm 0.1\text{ V}$	151			160		
			$1.8\text{ V} \pm 0.15\text{ V}$	194			220		
			$2.5\text{ V} \pm 0.2\text{ V}$	248			250		
			$3.3\text{ V} \pm 0.3\text{ V}$	280			260		
t_{pd}	CLK	Q	0.8 V	20.3					ns
			$1.2\text{ V} \pm 0.1\text{ V}$	5	8.7	13.6	3.9	15.6	
			$1.5\text{ V} \pm 0.1\text{ V}$	4.1	6.3	9.3	3.1	10.7	
			$1.8\text{ V} \pm 0.15\text{ V}$	3.3	4	7.6	2.4	8.7	
			$2.5\text{ V} \pm 0.2\text{ V}$	2.6	3.6	5.5	1.9	6.3	
			$3.3\text{ V} \pm 0.3\text{ V}$	2.2	3	4.5	1.6	5	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L = 30$ pF (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

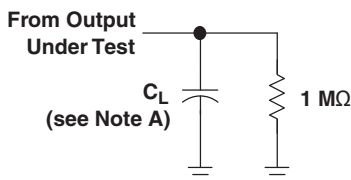
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{\max}			0.8 V	24			20		MHz
			$1.2\text{ V} \pm 0.1\text{ V}$	72			80		
			$1.5\text{ V} \pm 0.1\text{ V}$	100			100		
			$1.8\text{ V} \pm 0.15\text{ V}$	127			140		
			$2.5\text{ V} \pm 0.2\text{ V}$	185			210		
			$3.3\text{ V} \pm 0.3\text{ V}$	266			260		
t_{pd}	CLK	Q	0.8 V	27.2					ns
			$1.2\text{ V} \pm 0.1\text{ V}$	7	11.5	17.3	5.9	24	
			$1.5\text{ V} \pm 0.1\text{ V}$	5.7	8.3	13.3	4.6	15.9	
			$1.8\text{ V} \pm 0.15\text{ V}$	4.7	6.7	11.3	3.8	13	
			$2.5\text{ V} \pm 0.2\text{ V}$	3.7	4.9	7.8	2.9	9	
			$3.3\text{ V} \pm 0.3\text{ V}$	3.2	4.1	6.3	2.6	7.2	

OPERATING CHARACTERISTICS

$T_A = 25^\circ\text{C}$

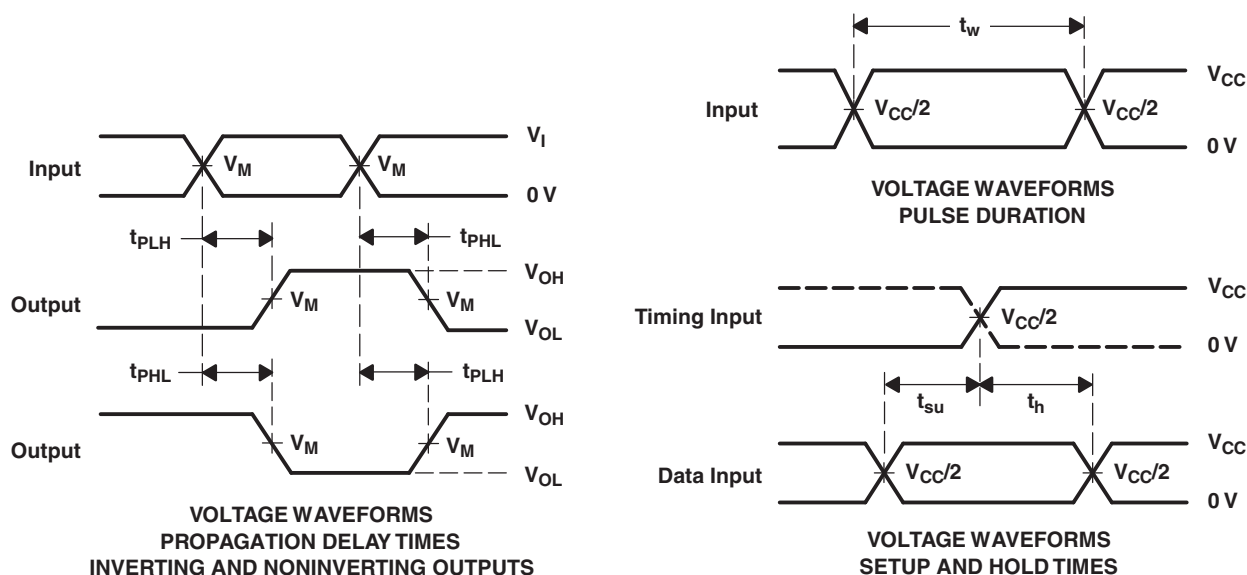
PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$f = 10\text{ MHz}$	0.8 V	2.5	pF
			$1.2\text{ V} \pm 0.1\text{ V}$	2.5	
			$1.5\text{ V} \pm 0.1\text{ V}$	2.5	
			$1.8\text{ V} \pm 0.15\text{ V}$	2.5	
			$2.5\text{ V} \pm 0.2\text{ V}$	3	
			$3.3\text{ V} \pm 0.3\text{ V}$	3	

PARAMETER MEASUREMENT INFORMATION
(Propagation Delays, Setup and Hold Times, and Pulse Width)



LOAD CIRCUIT

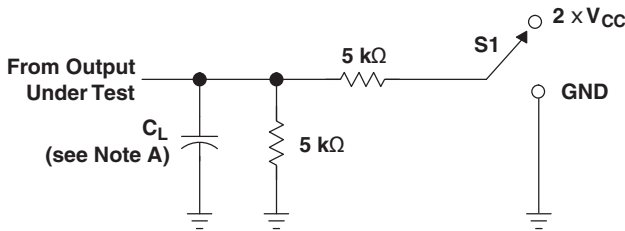
	$V_{CC} = 0.8\text{ V}$	$V_{CC} = 1.2\text{ V}$ $\pm 0.1\text{ V}$	$V_{CC} = 1.5\text{ V}$ $\pm 0.1\text{ V}$	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}



- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, for propagation delays $t_r/t_f = 3\text{ ns}$, for setup and hold times and pulse width $t_r/t_f = 1.2\text{ ns}$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLH} and t_{PHL} are the same as t_{pd} .
- F. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

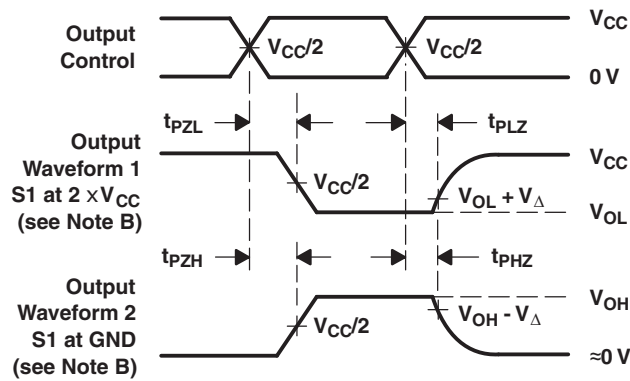
**PARAMETER MEASUREMENT INFORMATION
(Enable and Disable Times)**



TEST	S1
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PHL}	GND

LOAD CIRCUIT

	$V_{CC} = 0.8\text{ V}$	$V_{CC} = 1.2\text{ V}$ $\pm 0.1\text{ V}$	$V_{CC} = 1.5\text{ V}$ $\pm 0.1\text{ V}$	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_{Δ}	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r/t_f = 3\text{ ns}$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PLH} and t_{PHL} are the same as t_{pd} .
- G. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

REVISION HISTORY

Changes from Revision B (March 2010) to Revision C	Page
• Added clock high to FUNCTION TABLE.	2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74AUP2G79DCUR	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H79R	Samples
SN74AUP2G79DQER	ACTIVE	X2SON	DQE	8	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PT	Samples
SN74AUP2G79RSER	ACTIVE	UQFN	RSE	8	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PT	Samples
SN74AUP2G79YFPR	ACTIVE	DSBGA	YFP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HWN	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

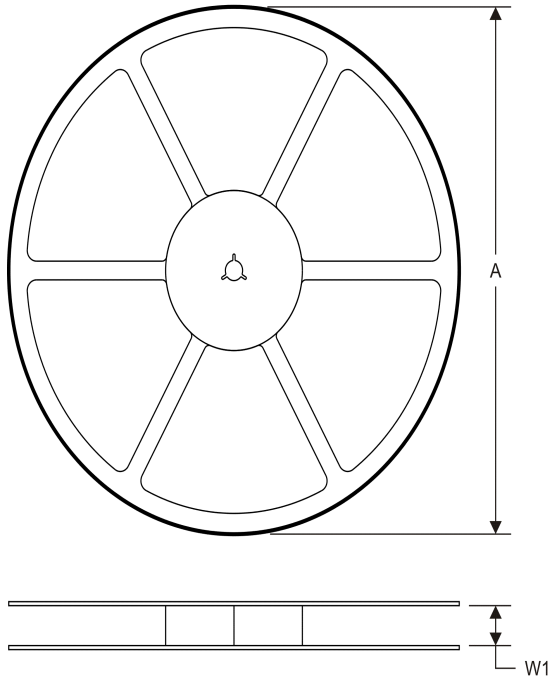
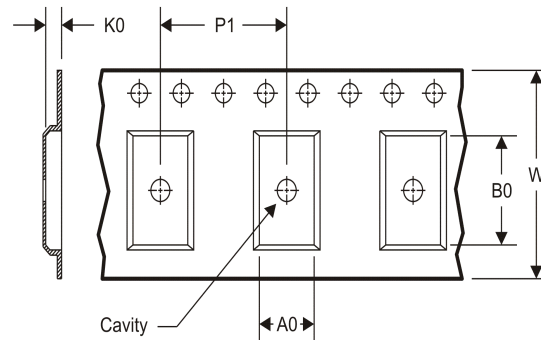
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP2G79DCUR	US8	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUP2G79DQER	X2SON	DQE	8	5000	180.0	8.4	1.2	1.6	0.55	4.0	8.0	Q1
SN74AUP2G79RSER	UQFN	RSE	8	5000	180.0	8.4	1.6	1.6	0.66	4.0	8.0	Q2
SN74AUP2G79YFPR	DSBGA	YFP	8	3000	178.0	9.2	0.9	1.75	0.6	4.0	8.0	Q1

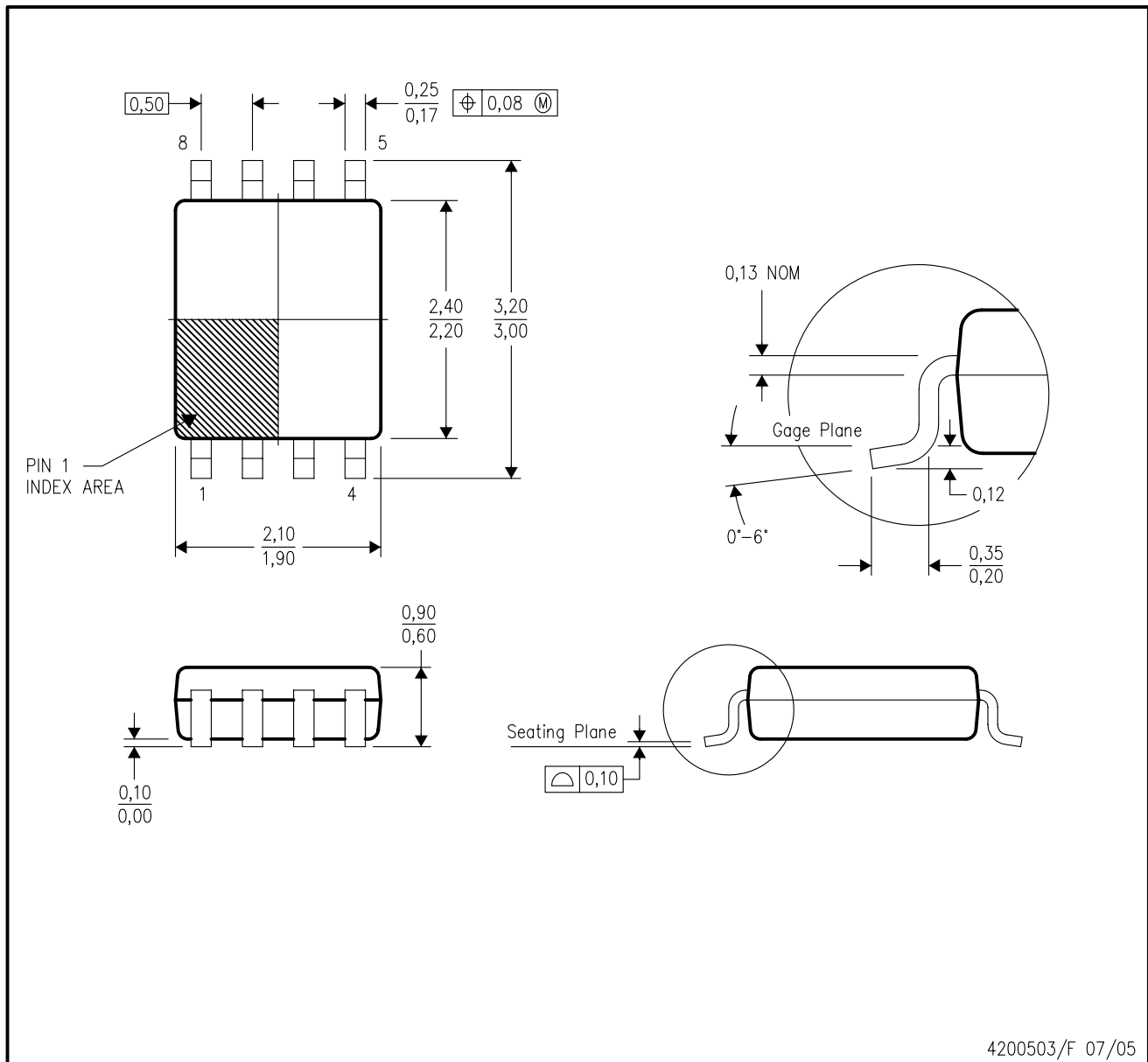
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP2G79DCUR	US8	DCU	8	3000	202.0	201.0	28.0
SN74AUP2G79DQER	X2SON	DQE	8	5000	202.0	201.0	28.0
SN74AUP2G79RSER	UQFN	RSE	8	5000	202.0	201.0	28.0
SN74AUP2G79YFPR	DSBGA	YFP	8	3000	220.0	220.0	35.0

DCU (R-PDSO-G8)

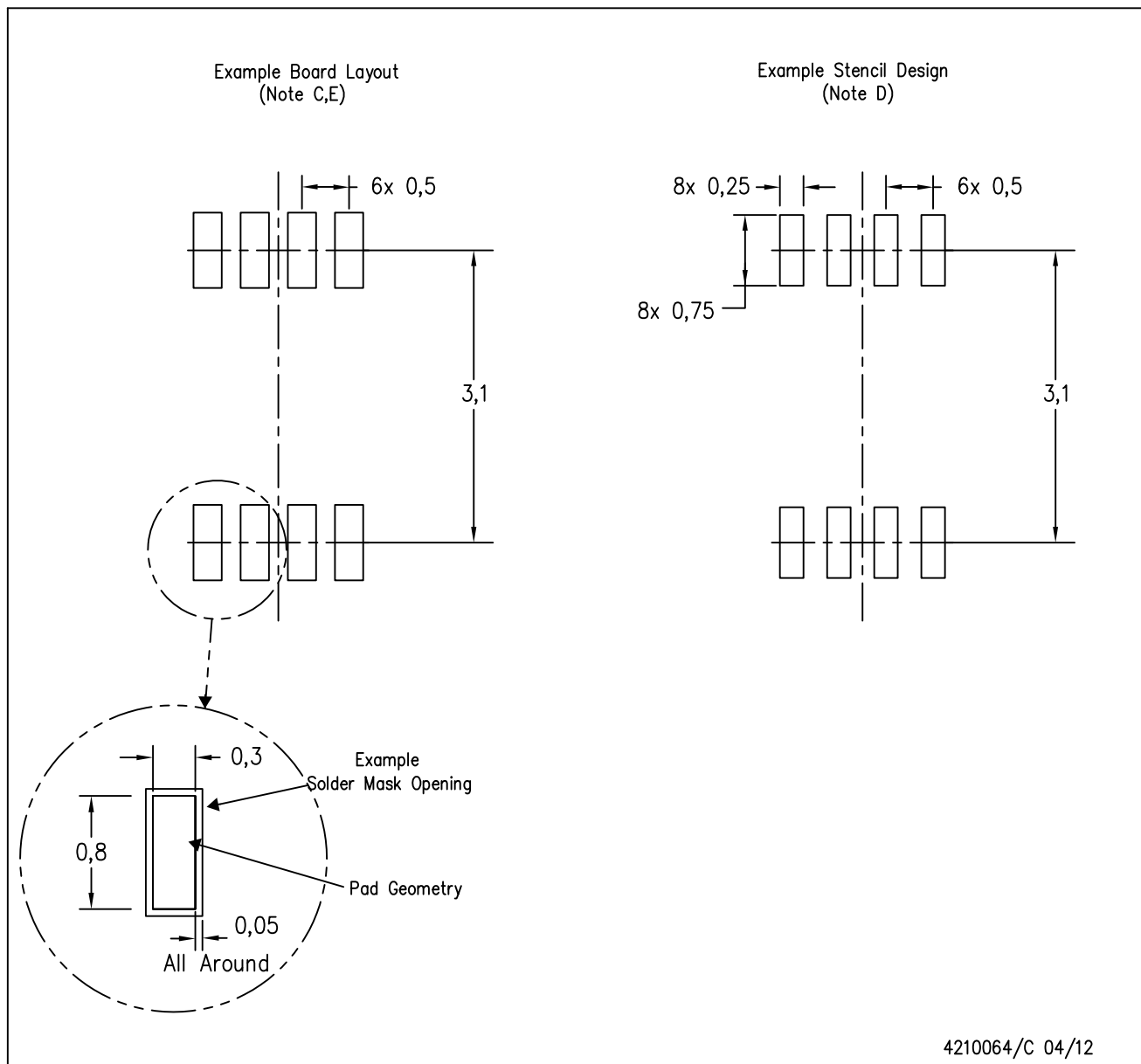
PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-187 variation CA.

DCU (S-PDSO-G8)

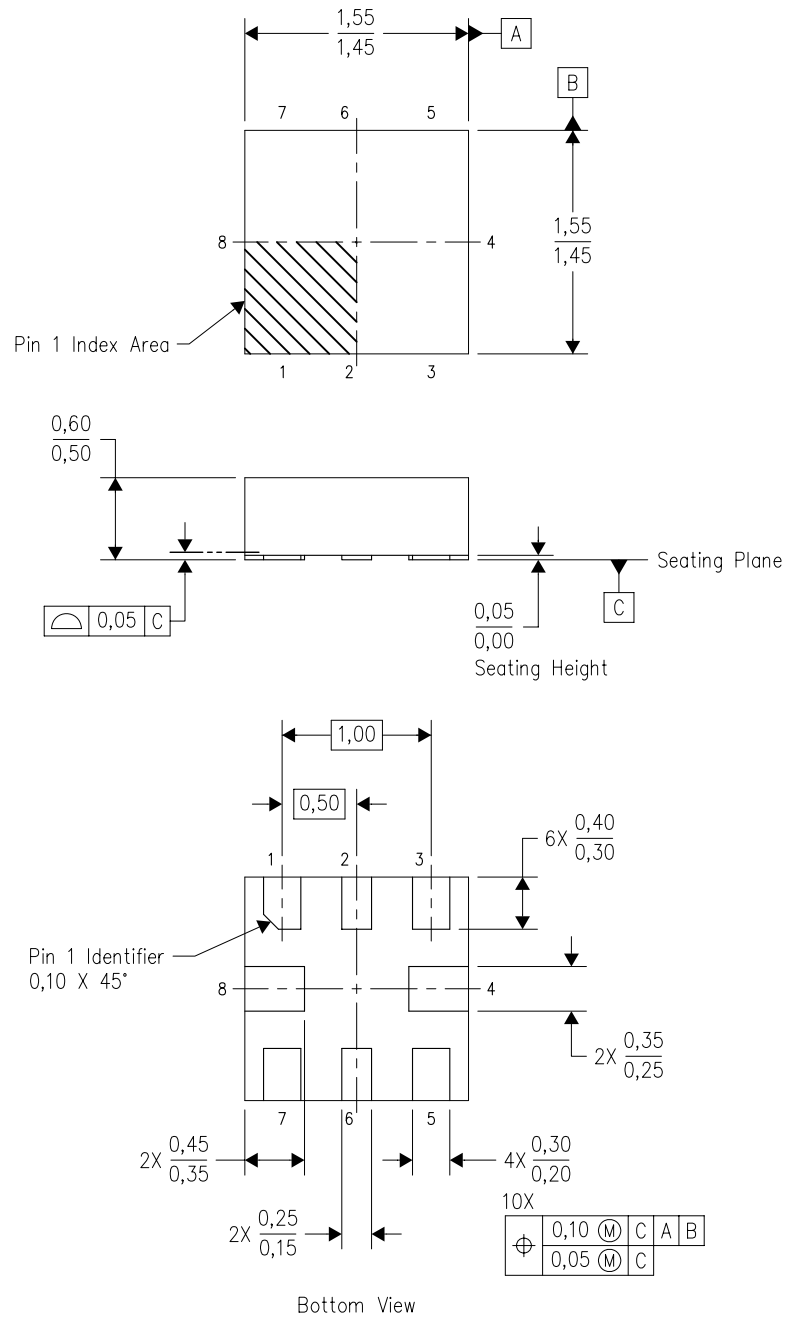
PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RSE (S-PUQFN-N8)

PLASTIC QUAD FLATPACK NO-LEAD

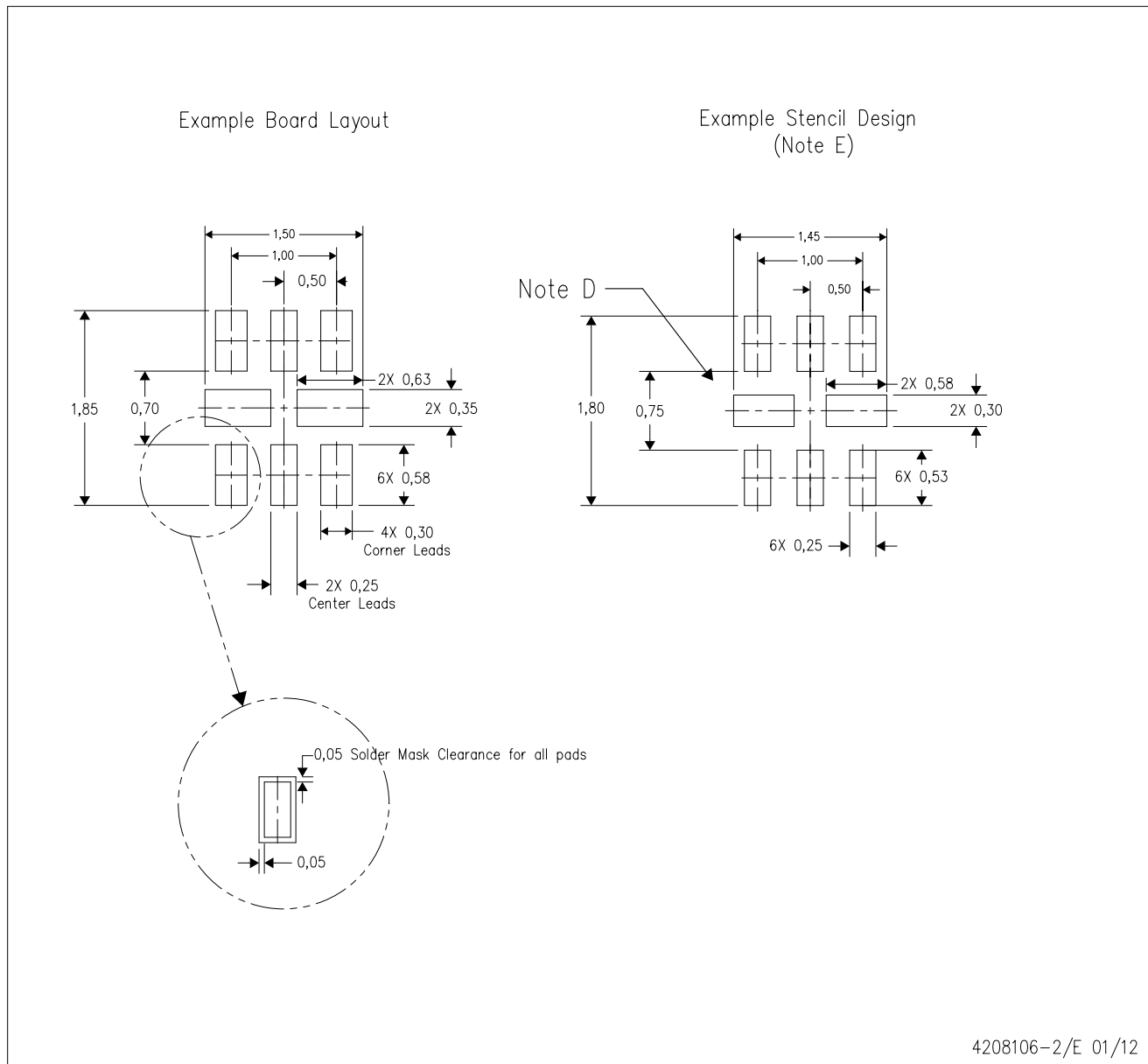


4207268-2/D 01/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - D. This package complies to JEDEC MO-288 variation UECD.

RSE (S-PUQFN-N8)

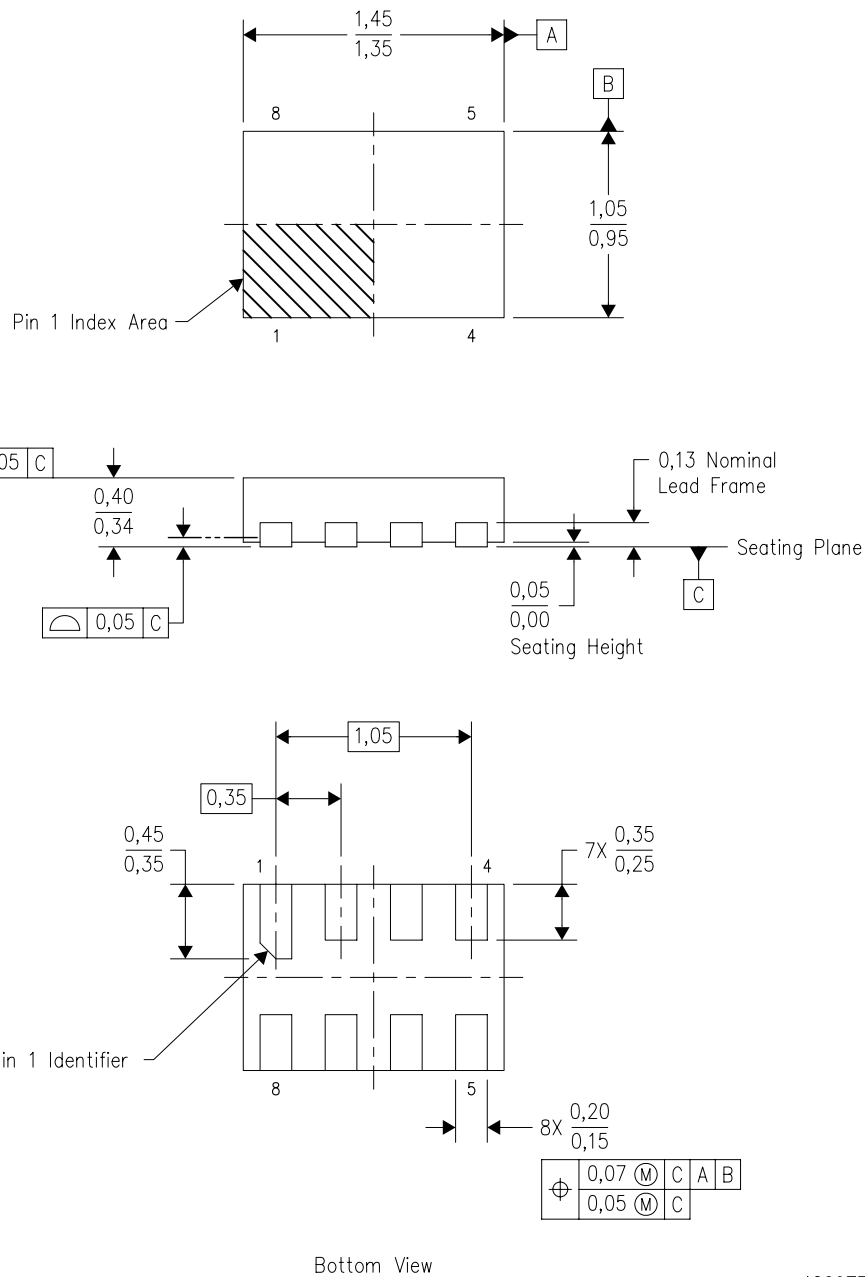
PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DQE (R-PX2SON-N8)

PLASTIC SMALL OUTLINE NO-LEAD

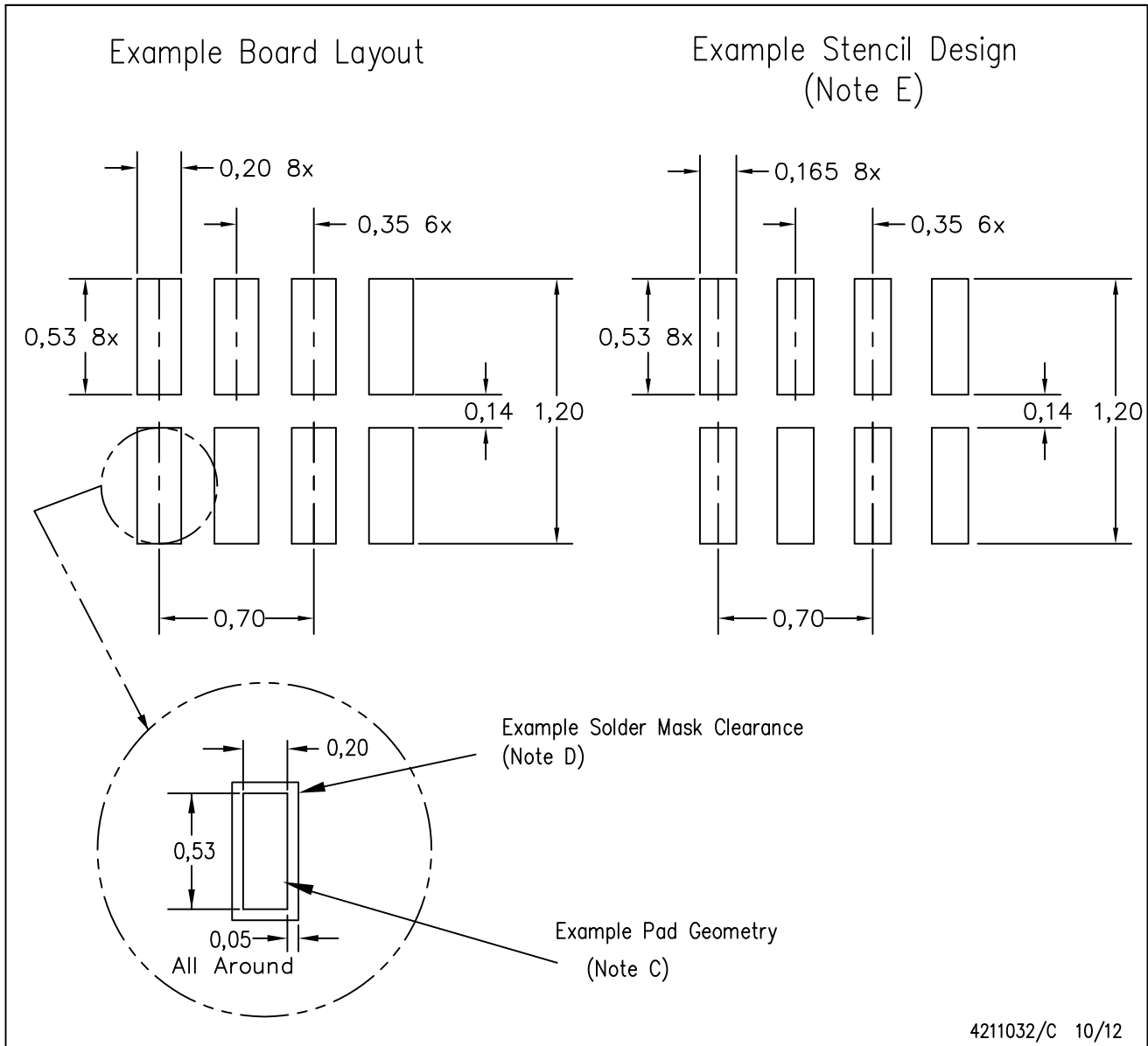


4209779/B 10/2008

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - SON (Small Outline No-Lead) package configuration.
 - This package complies to JEDEC MO-287 variation X2EAF.

DQE (R-PX2SON-N8)

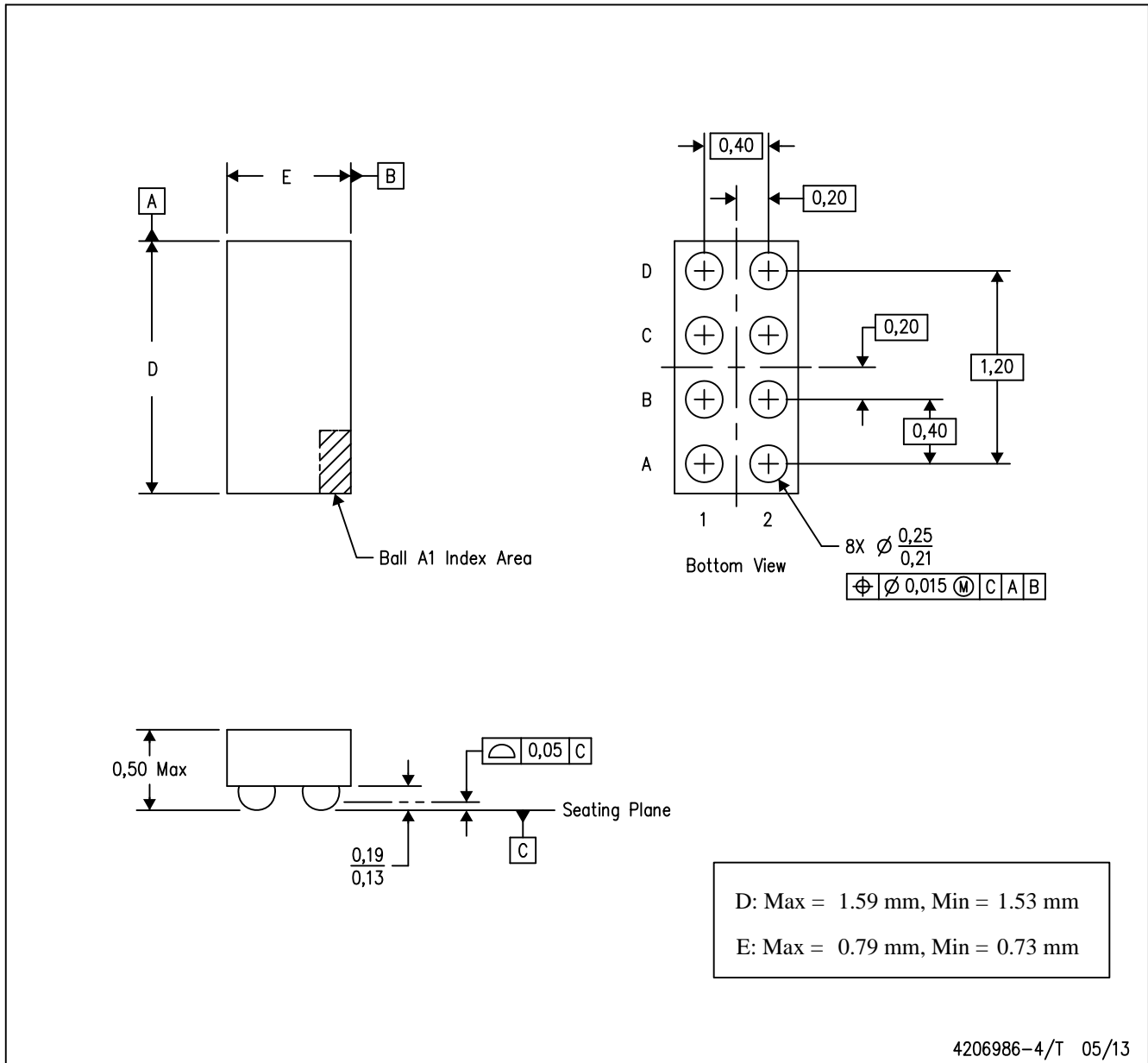
PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
 - E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Over-printing land for acceptable area ratio is not viable due to land width and bridging potential. Customer may further reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.
 - H. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
 - I. Component placement force should be minimized to prevent excessive paste block deformation.

YFP (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com