4-BIT BIDIRECTIONAL VOLTAGE-LEVEL TRANSLATOR WITH AUTOMATIC DIRECTION SENSING

Check for Samples: TXB0304

FEATURES

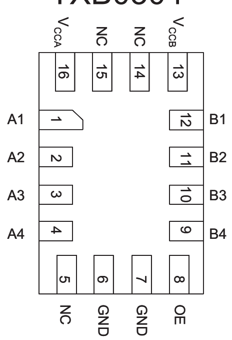
- **Fully Symmetric Supply Voltages. 0.9 V to 3.6 V on A Port and 0.9 V to 3.6 V**
- **V_{CC} Isolation Feature – If Either V_{CC} Input Is at GND, All Outputs Are in the High-Impedance State**
- **OE Input Circuit Referenced to V_{CCA}**
- **Low Power Consumption, 5-µA Max (I_{CCA} or I_{CCB})**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **8000-V Human-Body Model (A114-B)**
  - **1000-V Charged-Device Model (C101)**

DESCRIPTION

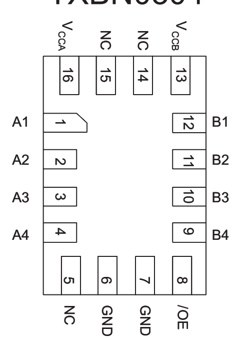
This 4-bit non-inverting translator uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 0.9 V to 3.6 V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 0.9 V to 3.6 V. This allows for low-voltage bidirectional translation between 1-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V and 3.3-V voltage nodes. For the TXB0304, when the output-enable (OE) input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver. The TXB0304 is designed so that the OE input circuit is supplied by V_{CCA}. This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

RSV PACKAGE (TOP VIEW)

TXB0304

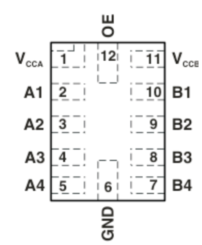


TXBN0304

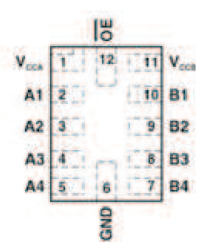


RUT PACKAGE (TOP VIEW)

TXB0304



TXBN0304



A. Pull up resistors are not required on both sides for Logic I/O.

B. If pull up or pull down resistors are needed, the resistor value must be over 20 kΩ.

C. 20 kΩ is a safe recommended value, if the customer can accept higher Vol or lower Voh, smaller pull up or pull down resistor is allowed, the draft estimation is Vol = Vccout × 1.5k/(1.5k + Rpu) and Voh = Vccout × Rdw/(1.5k + Rdw).

D. If pull up resistors are needed, please refer to the TXS0104 or contact TI.

E. For detailed information, please refer to application note SCEA043.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40 to 85°C	RUT – MicroQFN	TXB0304RUTR	73R
	RSV – QFN	TXB0304RSVR	ZTJ
	RUT – MicroQFN	TXBN0304RUTR	74R
	RSV – QFN	TXBN0304RSVR	ZTK

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com.

DEVICE INFORMATION

Table 1. SIGNAL DESCRIPTIONS

PIN NO.		NAME		FUNCTION	
RSV	RUT	TXB0304	TXBN0304		
16	1	V_{CCA}		A-port supply voltage 0.9V ≤ V_{CCA} ≤ 3.6V	
1	2	A1		Input/output 1	Referenced to V_{CCA}
2	3	A2		Input/output 2	
3	4	A3		Input/output 3	
4	5	A4		Input/output 4	
5	–	NC		No connection; not internally connected	
6,7	6	GND		Ground	
8	12	OE	$\overline{OE}$	3-state output-mode enable. Pull OE (TXB0304) low to place all outputs in 3-state mode. 3-state output-mode enable. Pull $\overline{OE}$ (TXBN0304) high to place all outputs in 3-state mode. Referenced to VCCA.	
9	7	B4		Input/output 1	Referenced to V_{CCB}
10	8	B3		Input/output 2	
11	9	B2		Input/output 3	
12	10	B1		Input/output 4	
13	11	V_{CCB}		B-port supply voltage 0.9V ≤ V_{CCB} ≤ 3.6V	
14	–	NC		No connection; not internally connected	
15	–	NC		No connection; not internally connected	

ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
VCCA	Supply voltage range		–0.5	4.6	V
VCCB			–0.5	4.6	
V_I	Input voltage range	A port	–0.5	4.6	V
		B port	–0.5	4.6	
V_O	Voltage range applied to any output in the high-impedance or power-off state	A port	–0.5	4.6	V
		B port	-0.5	4.6	
V_O	Voltage range applied to any output in the high or low state[2]	A port	–0.5	VCCA + 0.5	V
		B port	–0.5	VCCB + 0.5	
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through VCCA, VCCB, or GND			±100	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The value of VCCA and VCCB are provided in the recommended operating conditions table.

THERMAL IMPEDANCE RATINGS

over operating free-air temperature range (unless otherwise noted)

				UNIT
θ_{JA}	Package thermal impedance	RUT package[1]	87	°C/W
		RSV package[2]	184	

(1) The package thermal impedance is calculated in accordance with JESD 51-7
(2) The package thermal impedance is calculated in accordance with JESD 51-5.

RECOMMENDED OPERATING CONDITIONS[1][2]

			V_{CCA}	V_{CCB}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				0.9	3.6	V
V_{CCB}					0.9	3.6	
V_{IH}	High-level input voltage	Data inputs	0.9 V to 3.6 V	0.9 V to 3.6 V	V_{CCI} × 0.65	VCCI	V
		OE	0.9 V to 3.6 V	0.9 V to 3.6 V	V_{CCA} × 0.65	3.6	
V_{IL}	Low-level input voltage	Data inputs	0.9 V to 3.6 V	0.9 V to 3.6 V	0	VCCI × 0.35	V
		OE	0.9 V to 3.6 V	0.9 V to 3.6 V	0	VCCA × 0.35	
V_O	Voltage range applied to any output in the high-impedance or power-off state	A-port	0.9 V to 3.6 V	0.9 V to 3.6 V	0	3.6	V
		B-port	0.9 V to 3.6 V	0.9 V to 3.6 V	0	3.6	
Δt/Δv	Input transition rise or fall rate	A-port inputs	0.9 V to 3.6 V	0.9 V to 3.6 V		40	ns/V
		B-port inputs	0.9 V to 3.6 V	0.9 V to 3.6 V		40	
T_A	Operating free-air temperature				–40	85	°C

(1) The A and B sides of an unused data I/O pair must be held in the same state, i.e., both at V_{CCI} or both at GND.
(2) V_{CCI} is the supply voltage associated with the input port.

ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	T_A = 25°C			–40°C to 85°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
V_{OHA}		I_{OH} = –20 μA	0.9 V to 3.6 V				0.9 x V_{CCA}			V
V_{OLA}		I_{OL} = 20 μA	0.9 V to 3.6 V					0.2		V
V_{OHB}		I_{OH} = –20 μA		0.9 V to 3.6 V			0.9 x V_{CCB}			V
V_{OLB}		I_{OL} = 20 μA		0.9 V to 3.6 V				0.2		V
I_I	OE	V_I = V_{CCI} or GND	0.9 V to 3.6 V	0.9 V to 3.6 V			±1		±2	μA
I_{off}	A port	V_I or V_O = 0 to 3.6 V	0 V	0 V to 3.6 V			±1		±2	μA
	B port	V_I or V_O = 0 to 3.6 V	0.9 V to 3.6 V	0 V			±1		±2	
I_{OZ}	A or B port	OE = GND	0.9 V to 3.6 V	0.9 V to 3.6 V			±1		±2	μA
I_{CCA}		V_I = V_{CCI} or GND, I_O = 0	0.9 V to 3.6 V	0.9 V to 3.6 V					5	μA
I_{CCB}		V_I = V_{CCI} or GND, I_O = 0	0.9 V to 3.6 V	0.9 V to 3.6 V					5	μA
I_{CCA} + I_{CCB}		V_I = V_{CCI} or GND, I_O = 0	0.9 V to 3.6 V	0.9 V to 3.6 V					10	μA
I_{CCZA}		V_I = V_{CCI} or GND, I_O = 0, OE = GND	0.9 V to 3.6 V	0.9 V to 3.6 V					5	μA
I_{CCZB}		V_I = V_{CCI} or GND, I_O = 0, OE = GND	0.9 V to 3.6 V	0.9 V to 3.6 V					5	μA
C_i	OE		0.9 V to 3.6 V	0.9 V to 3.6 V		3				pF
C_{io}	A port		0.9 V to 3.6 V	0.9 V to 3.6 V		6.7				pF
	B port					6.7				

TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted)

			VCCA	VCCB	MIN	MAX	UNIT
	Data rate	C_L = 15 pF	0.9 to 3.6 V	0.9 to 3.6 V		50	Mbps
		C_L = 15 pF	1.2 to 3.6 V	1.2 to 3.6 V		100	Mbps
		C_L = 15 pF	1.8 to 3.6 V	1.8 to 3.6 V		140	Mbps
		C_L = 30 pF	0.9 to 3.6 V	0.9 to 3.6 V		40	Mbps
		C_L = 30 pF	1.2 to 3.6 V	1.2 to 3.6 V		90	Mbps
		C_L = 30 pF	1.8 to 3.6 V	1.8 to 3.6 V		130	Mbps
		C_L = 50 pF	1.2 to 3.6 V	1.2 to 3.6 V		80	Mbps
		C_L = 50 pF	1.8 to 3.6 V	1.8 to 3.6 V		120	Mbps
		C_L = 100 pF	1.2 to 3.6 V	1.2 to 3.6 V		70	Mbps
		C_L = 100 pF	1.8 to 3.6 V	1.8 to 3.6 V		100	Mbps

SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		VCCA	VCCB	MIN	TYP T_A = 25°C	MAX	UNIT
t_{pd}	A	B	C_L = 15	0.9-3.6	0.9-3.6		18.9	30	ns
	A	B	C_L = 15	1.2-3.6	1.2-3.6		7.5	11.5	
	A	B	C_L = 15	1.8-3.6	1.8-3.6		3.7	4.8	
	A	B	C_L = 30	0.9-3.6	0.9-3.6		19.5	34	
	A	B	C_L = 30	1.2-3.6	1.2-3.6		7.8	11.9	
	A	B	C_L = 30	1.8-3.6	1.8-3.6		3.8	5.2	
	A	B	C_L = 50	1.2-3.6	1.2-3.6		8	12.3	
	A	B	C_L = 50	1.8-3.6	1.8-3.6		4	5.4	
	A	B	C_L = 100	1.2-3.6	1.2-3.6		8.6	13.5	
	A	B	C_L = 100	1.8-3.6	1.8-3.6		4.5	6	
	B	A	C_L = 15	0.9-3.6	0.9-3.6		18.9	30	ns
	B	A	C_L = 15	1.2-3.6	1.2-3.6		7.5	11.5	
	B	A	C_L = 15	1.8-3.6	1.8-3.6		3.7	5	
	B	A	C_L = 30	0.9-3.6	0.9-3.6		19.5	34	
	B	A	C_L = 30	1.2-3.6	1.2-3.6		7.8	11.9	
	B	A	C_L = 30	1.8-3.6	1.8-3.6		3.8	5.2	
	B	A	C_L = 50	1.2-3.6	1.2-3.6		8	12.3	
	B	A	C_L = 50	1.8-3.6	1.8-3.6		4	5.4	
	B	A	C_L = 100	1.2-3.6	1.2-3.6		8.6	13.5	
	B	A	C_L = 100	1.8-3.6	1.8-3.6		4.5	6	
t_{en}	OE	A	C_L = 15	0.9-3.6	0.9-3.6			173	ns
		B	C_L = 15	0.9-3.6	0.9-3.6			213	
t_{dis}	OE	A	C_L = 15	0.9-3.6	0.9-3.6			172	ns
		B	C_L = 15	0.9-3.6	0.9-3.6			169	ns
t_{rB}, t_{fB}	B-port rise and fall times		C_L = 15	0.9-3.6	0.9-3.6		2.95		ns
t s, t s	A-port rise and fall times		C_L = 15	0.9-3.6	0.9-3.6		3.1		ns
$t_{SK(O)}$	Channel-to-channel skew		C_L = 15	0.9-3.6	0.9-3.6			0.15	ns

OPERATING CHARACTERISTICS

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CCA}, V_{CCB} 0.9 V to 3.6 V TYP	UNIT
C_{pdA}	A-port input, B-port output	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns, OE = V_{CCA} (outputs enabled)	34	pF
	B-port input, A-port output		34	
C_{pdB}	A-port input, B-port output		34	pF
	B-port input, A-port output		34	
C_{pdA}	A-port input, B-port output	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns, OE = GND (outputs disabled)	0.01	pF
	B-port input, A-port output		0.01	
C_{pdB}	A-port input, B-port output		0.01	pF
	B-port input, A-port output		0.01	

PRINCIPLES OF OPERATION

Applications

The TXB0304 can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another.

Architecture

The TXB0304 architecture (see Figure 1) does not require a direction-control signal to control the direction of data flow from A to B or from B to A. In a dc state, the output drivers of the TXB0304 can maintain a high or low, but are designed to be weak, so that they can be overdriven by an external driver when data on the bus starts flowing the opposite direction. The output one shots detect rising or falling edges on the A or B ports. During a rising edge, the one shot turns on the PMOS transistors (T1, T3) for a short duration, which speeds up the low-to-high transition. Similarly, during a falling edge, the one shot turns on the NMOS transistors (T2, T4) for a short duration, which speeds up the high-to-low transition. The typical output impedance during output transition is 30 Ω at V_{CCO} = 0.9 V to 1 V, 10 Ω at V_{CCO} = 1.1 V to 1.7 V, and 5 Ω at V_{CCO} = 1.8 V to 3.3 V.

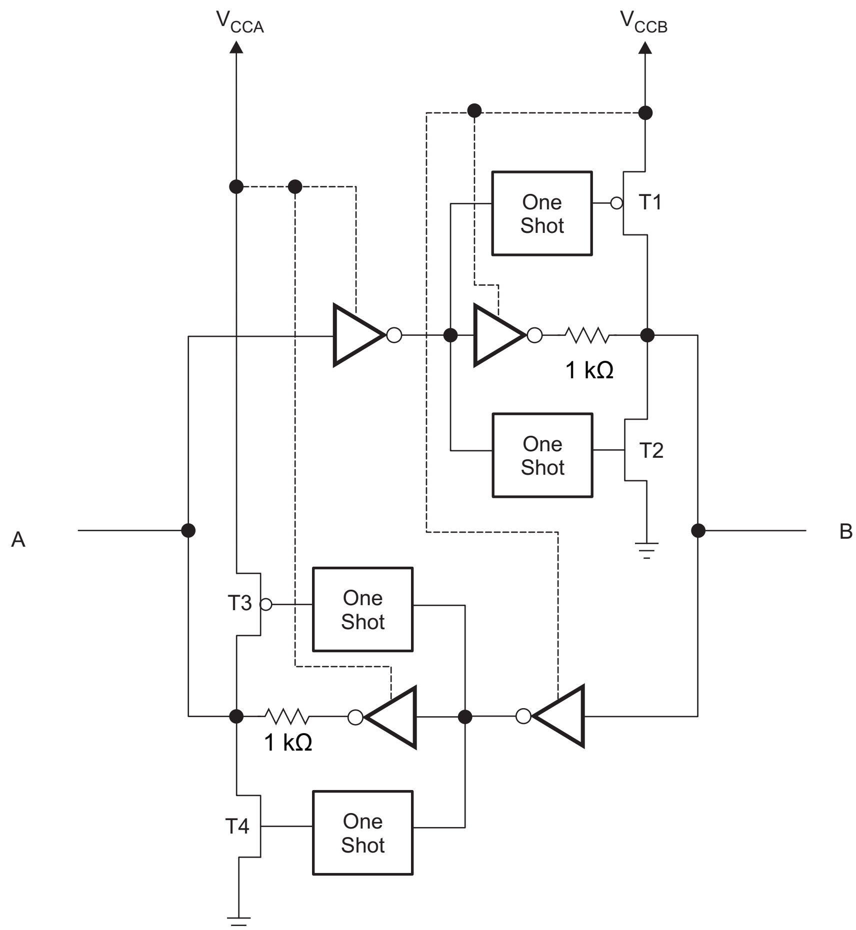
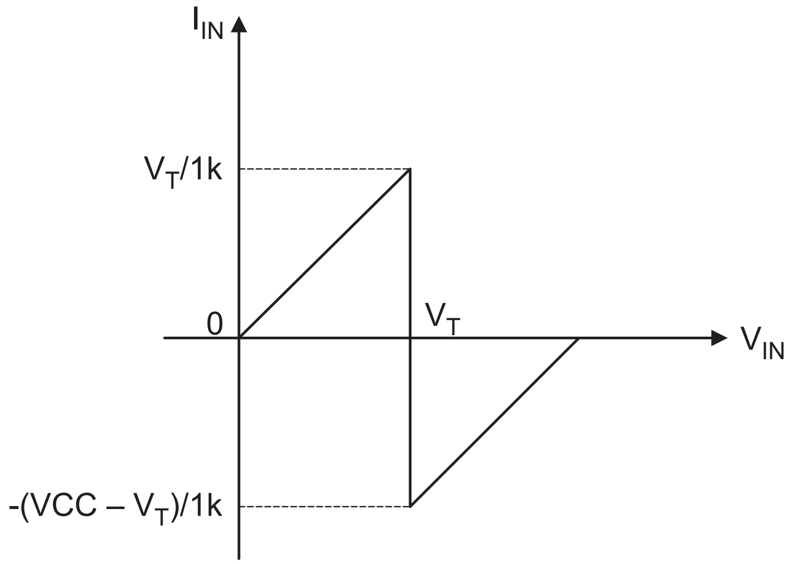


Figure 1. Architecture of TXB0302 I/O Cell

Input Driver Requirements

Typical I_{IN} vs V_{IN} characteristics of the TXB0304 are shown in Figure 2. For proper operation, the device driving the data I/Os of the TXB0304 must have drive strength of at least ±3 mA.



(1) V_{CC} is power supply of TXB0304.

(2) V_T is the input threshold voltage of TXB0304 (typically it is V_{CC}/2).

Figure 2. Typical I_{IN} vs V_{IN} Curve

Power Up

There is no requirement for the power sequence. During operation, TXB0304 can work at both $V_{CCA} \leq V_{CCB}$ and $V_{CCA} \geq V_{CCB}$, During power-up sequencing, any power supply can be ramped up first. The TXB0304 has circuitry that disables all output ports when either V_{CC} is switched off ($V_{CCA/B}$ = 0 V).

Enable and Disable

The TXB0304 has an OE input that is used to disable the device by setting OE = low, which places all I/Os in the high-impedance (Hi-Z) state. The disable time (t_{dis}) indicates the delay between when OE goes low and when the outputs actually get disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken high.

Pullup or Pulldown Resistor on I/O Lines

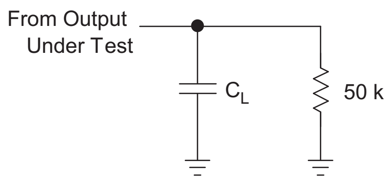
The TXB0304 is designed to drive capacitive loads of up to 100 pF. The output drivers of the TXB0304 have low dc drive strength. If pullup or pulldown resistors are connected externally to the data I/Os, their values must be kept higher than 20 kΩ to ensure that they do not contend with the output drivers of the TXB0304. but if the receiver is integrated with the smaller pull down or pull up resistor, below formula can be used for estimation to evaluate the Voh and Vol.

$$V_{ol} = V_{CCout} \times \frac{1.5k\Omega}{1.5k\Omega + R_{pu}} \tag{1}$$

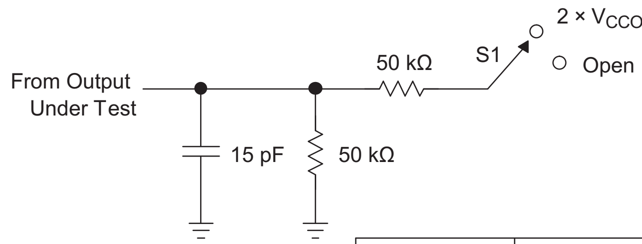
$$V_{oh} = V_{CCout} \times \frac{R_{pd}}{1.5k\Omega + R_{pd}} \tag{2}$$

For the same reason, the TXB0304 should not be used in applications such as I^2C or 1-Wire where an open-drain driver is connected on the bidirectional data I/O. For these applications, use a device from the TI TXS01xx series of level translators.

PARAMETER MEASUREMENT INFORMATION

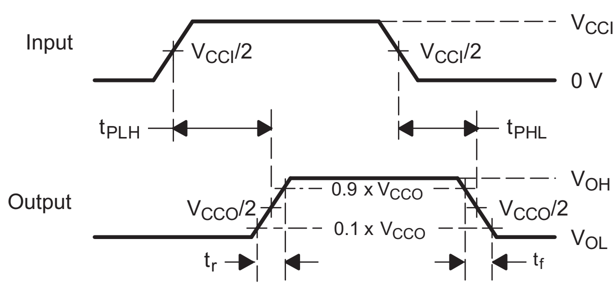


LOAD CIRCUIT FOR MAX DATA RATE, PULSE DURATION PROPAGATION DELAY OUTPUT RISE AND FALL TIME MEASUREMENT

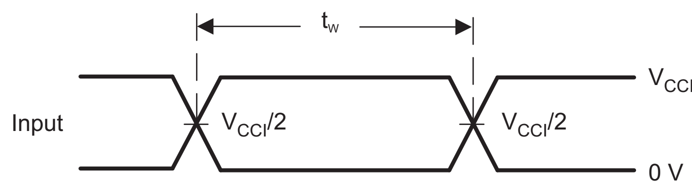


LOAD CIRCUIT FOR ENABLE/DISABLE TIME MEASUREMENT

TEST	S1
t_{PZL}/t_{PLZ}	2 × V_{CCO}
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS PULSE DURATION

A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.
E. V_{CCI} is the V_{CC} associated with the input port.
F. V_{CCO} is the V_{CC} associated with the output port.
G. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuits and Voltage Waveforms

REVISION HISTORY

Changes from Revision B (September 2011) to Revision C	Page
• Added package pin out diagram notes.	1

Changes from Revision C (May 2012) to Revision D	Page
• Added Application Information Section	6

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TXB0304RSVR	ACTIVE	UQFN	RSV	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZTJ	Samples
TXB0304RUTR	ACTIVE	UQFN	RUT	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(737 ~ 73R)	Samples
TXBN0304RSVR	ACTIVE	UQFN	RSV	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZTK	Samples
TXBN0304RUTR	ACTIVE	UQFN	RUT	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	74R	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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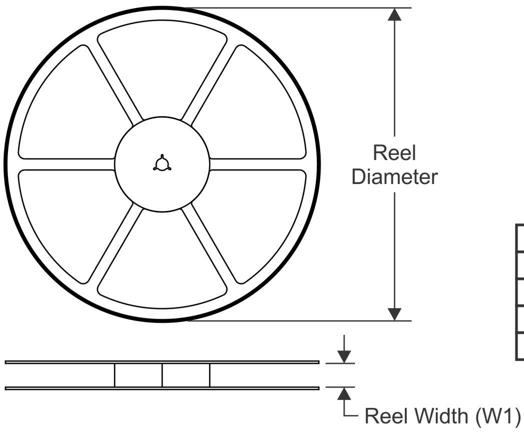
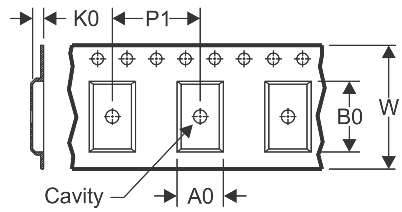
TAPE AND REEL INFORMATION

REEL DIMENSIONS

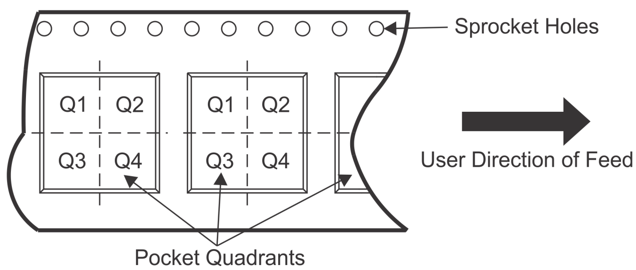


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

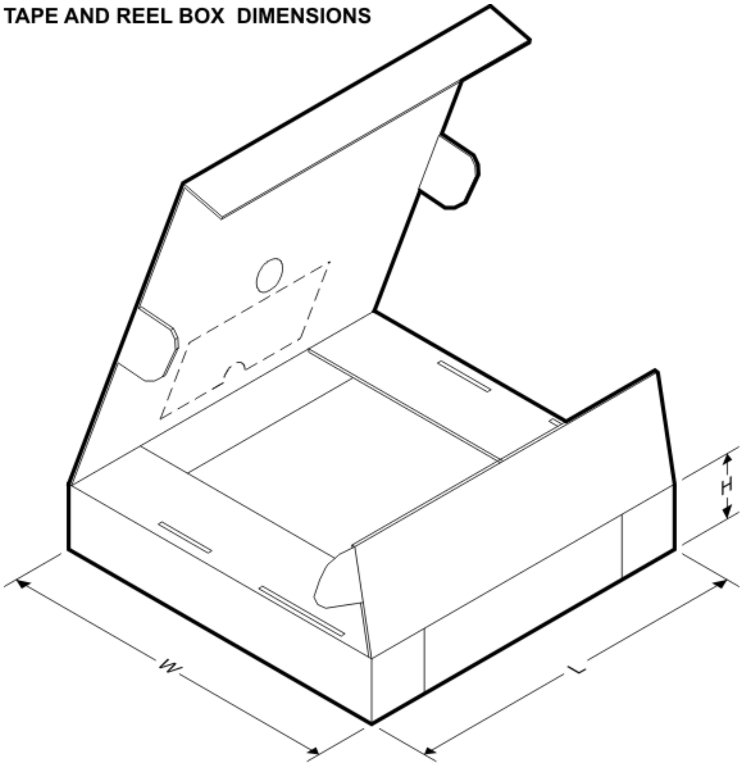
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXB0304RSVR	UQFN	RSV	16	3000	177.8	12.4	2.0	2.8	0.7	4.0	12.0	Q1
TXB0304RUTR	UQFN	RUT	12	3000	180.0	9.5	1.9	2.3	0.75	4.0	8.0	Q1
TXBN0304RSVR	UQFN	RSV	16	3000	330.0	12.4	2.1	2.9	0.75	4.0	12.0	Q1
TXBN0304RSVR	UQFN	RSV	16	3000	177.8	12.4	2.0	2.8	0.7	4.0	12.0	Q1
TXBN0304RUTR	UQFN	RUT	12	3000	180.0	8.4	1.95	2.3	0.75	4.0	8.0	Q1

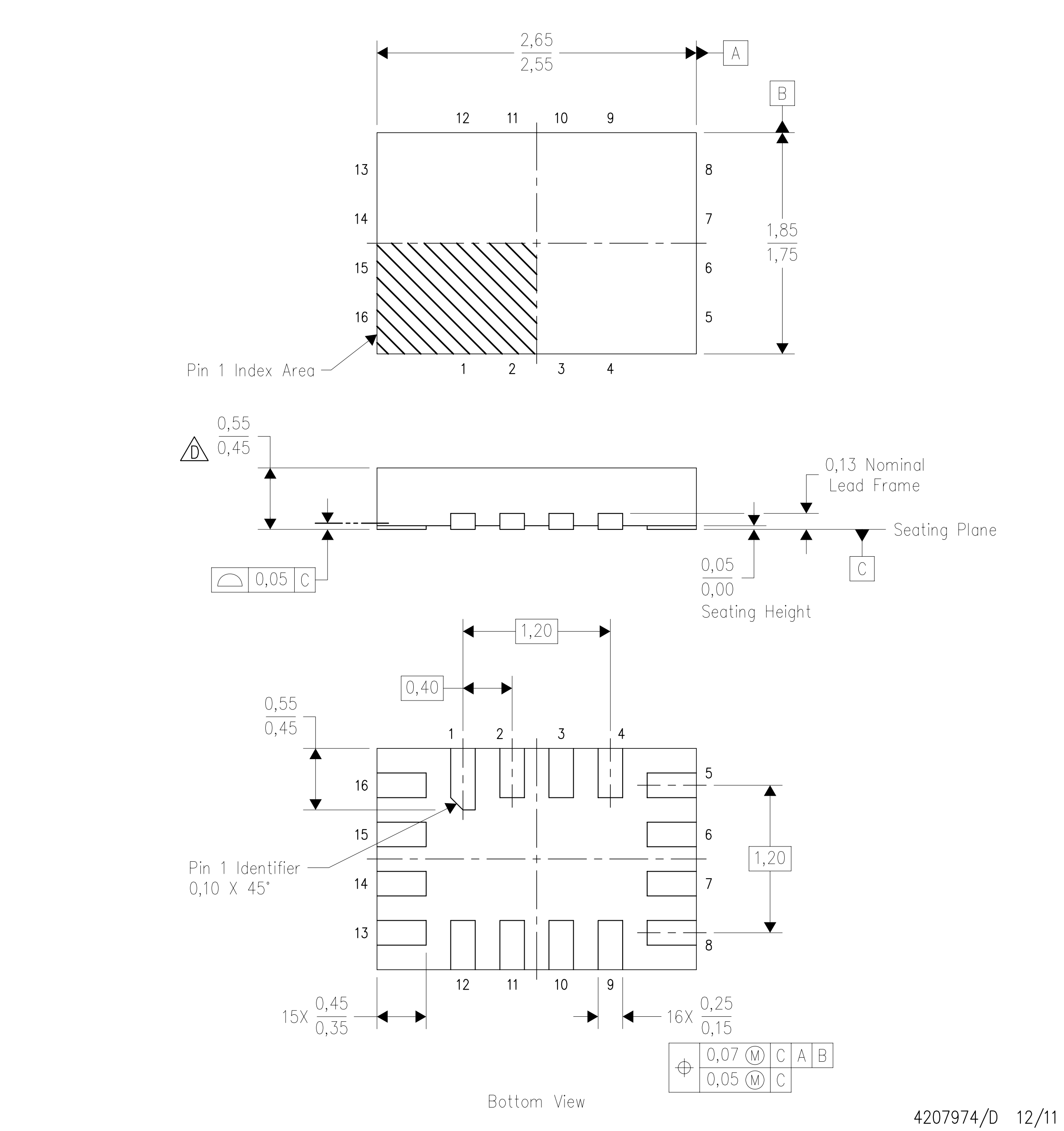
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXB0304RSVR	UQFN	RSV	16	3000	202.0	201.0	28.0
TXB0304RUTR	UQFN	RUT	12	3000	180.0	180.0	30.0
TXBN0304RSVR	UQFN	RSV	16	3000	180.0	180.0	30.0
TXBN0304RSVR	UQFN	RSV	16	3000	202.0	201.0	28.0
TXBN0304RUTR	UQFN	RUT	12	3000	202.0	201.0	28.0

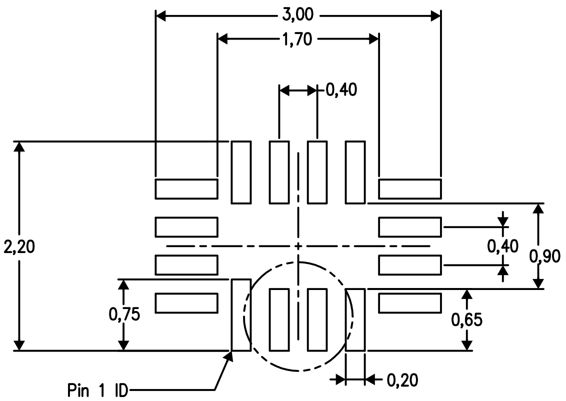
RSV (R-PUQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD



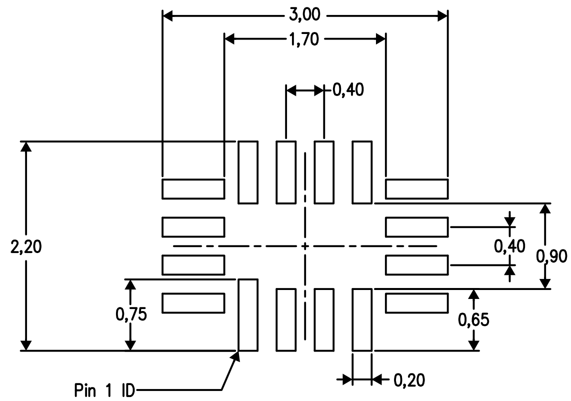
NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) package configuration.
- D. This package complies to JEDEC MO-288 variation UFHE, except minimum package thickness.

RSV (R–PUQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

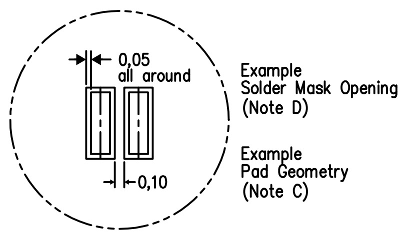
Example Board Layout



Example Stencil Design
0.125mm Stencil Thickness
(Note F&G)



Non Solder Mask Defined Pad



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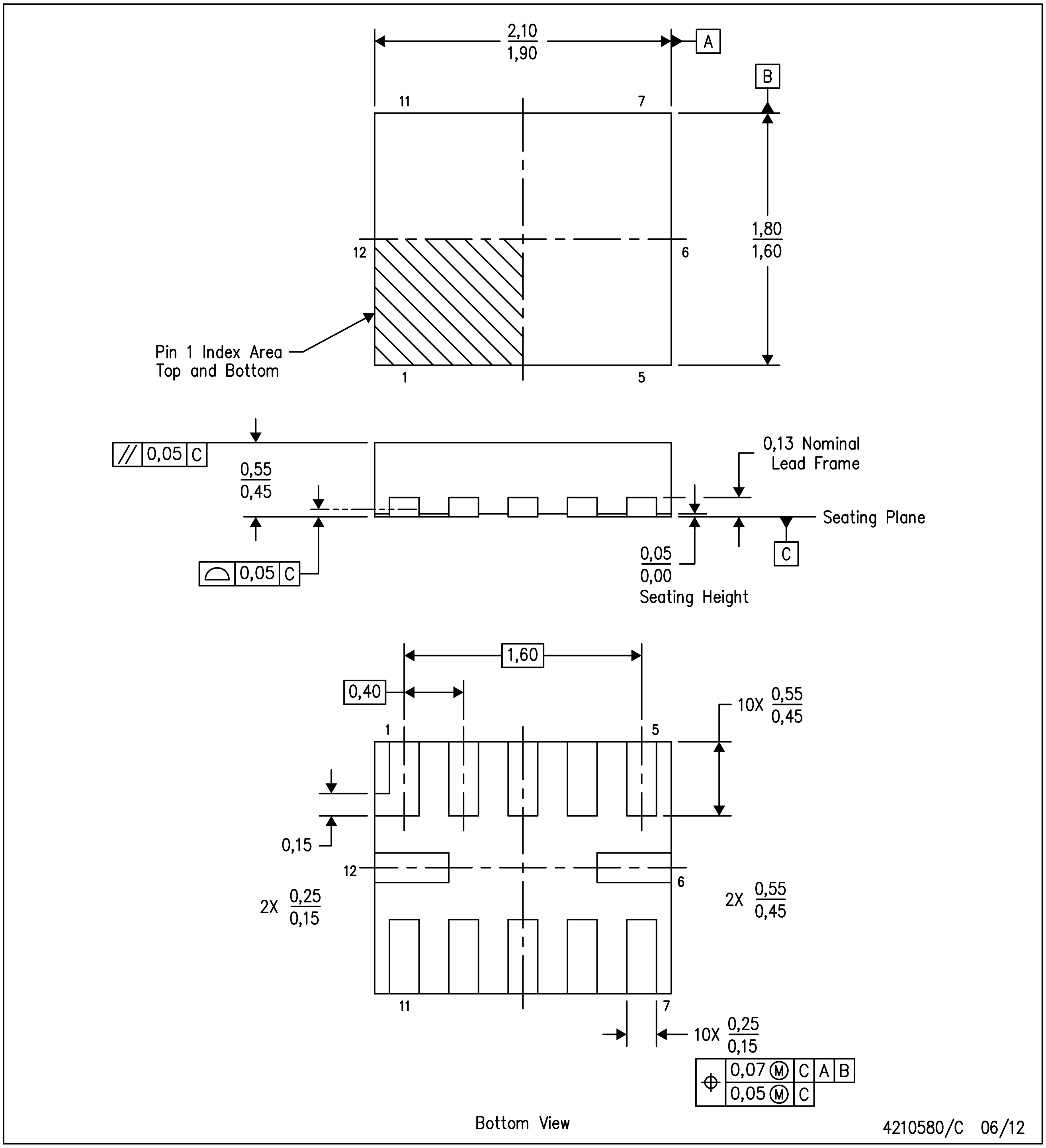
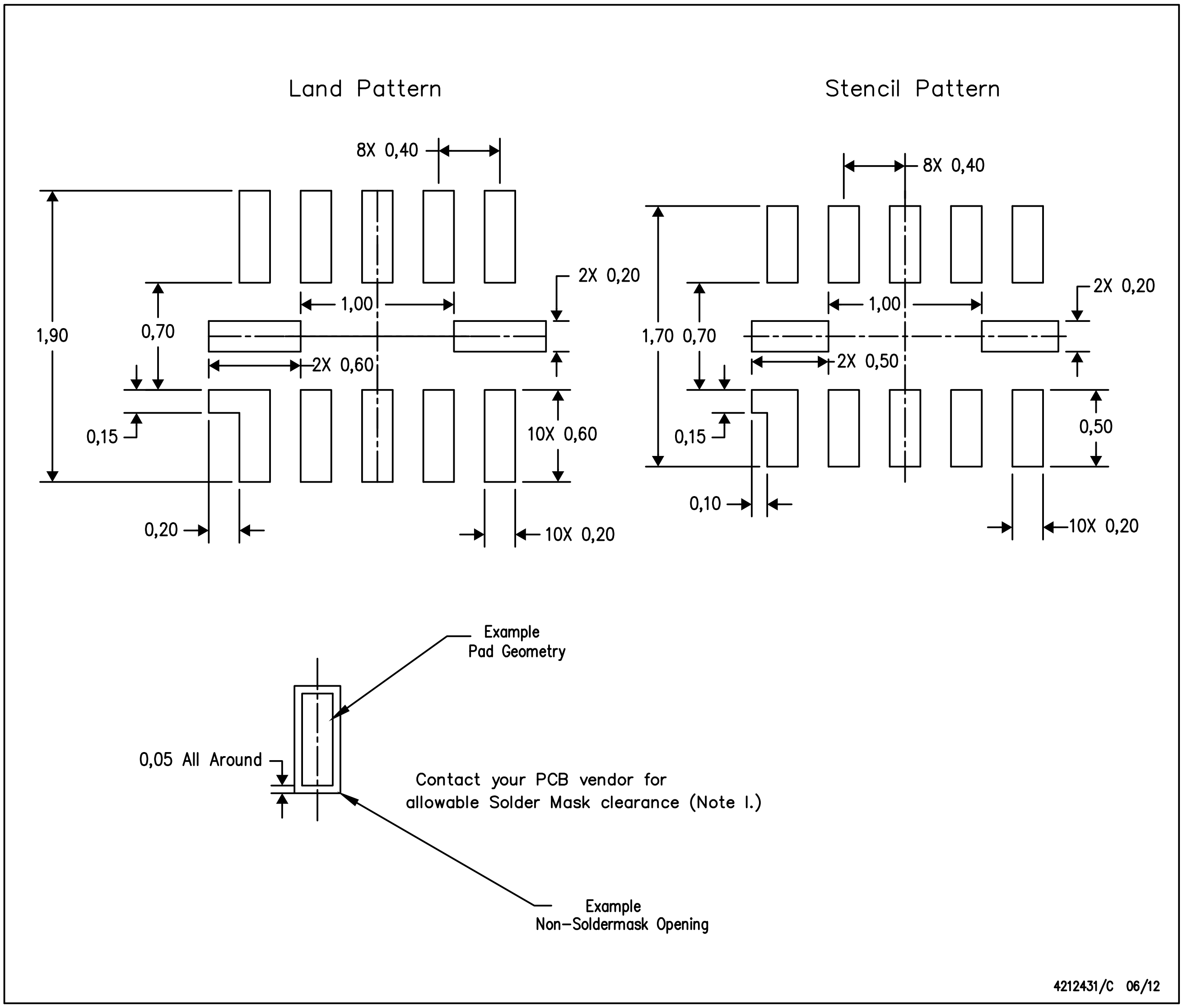
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

RUT (R–PUQFN–N12) PLASTIC QUAD FLATPACK NO–LEAD



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.

RUT (R-PUQFN-N12) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Over-printing land for larger area ratio is not advised due to land width and bridging potential. Exersize extreme caution.
- H. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
- I. Component placement force should be minimized to prevent excessive paste block deformation.

IMPORTANT NOTICE

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