

# Z8® Z8681/82 ROMless Microcomputer

# Zilog

## Product Specification

April 1985

### FEATURES

- Complete microcomputer, 24 I/O lines, and up to 64K bytes of addressable external space each for program and data memory.
- 143-byte register file, including 124 general-purpose registers, 3 I/O port registers, and 16 status and control registers.
- Vectored, priority interrupts for I/O, counter/timers, and UART.
- On-chip oscillator that accepts crystal or external clock drive.
- Full-duplex UART and two programmable 8-bit counter/timers, each with a 6-bit programmable prescaler.
- Register Pointer so that short, fast instructions can access any one of the nine working-register groups.
- Single +5V power supply—all I/O pins TTL compatible.
- Z8681/82 available in 8 MHz. Z8681 also available in 12 MHz.

### GENERAL DESCRIPTION

The Z8681 and Z8682 are ROMless versions of the Z8 single-chip microcomputer. The Z8682 is usually more cost effective. These products differ only slightly and can be used interchangeably with proper system design to provide maximum flexibility in meeting price and delivery needs.

The Z8681/82 offers all the outstanding features of the Z8 family architecture except an on-chip program ROM. Use of external memory rather than a preprogrammed ROM enables this Z8 microcomputer to be used in low volume applications or where code flexibility is required.

Z8681/82 MCU

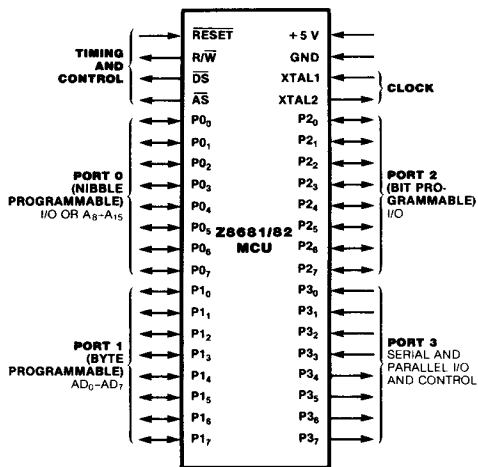


Figure 1. Pin Functions

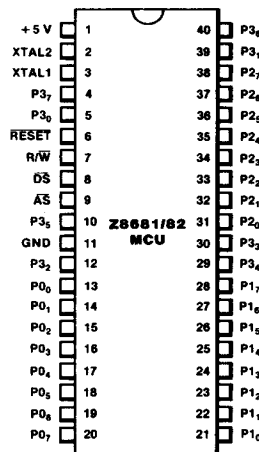


Figure 2a. 40-pin Dual-In-Line Package (DIP), Pin Assignments

The Z8681/82 can provide up to 16 output address lines, thus permitting an address space of up to 64K bytes of data or program memory. Eight address outputs (AD<sub>0</sub>-AD<sub>7</sub>) are provided by a multiplexed, 8-bit, Address/Data bus. The remaining 8 bits can be provided by the software configuration of Port 0 to output address bits A<sub>8</sub>-A<sub>15</sub>.

Available address space can be doubled (up to 128K bytes for the Z8681 and 124K bytes for the Z8682) by programming bit 4 of Port 3 (P3<sub>4</sub>) to act as a data memory select output (DM). The two states of DM together with the 16 address outputs can define separate data and memory address spaces of up to 64K/62Kbytes each.

There are 143 bytes of RAM located on-chip and organized as a register file of 124 general-purpose registers, 16 control and status registers, and three I/O port registers. This register file can be divided into nine groups of 16 working registers each. Configuring the register file in this manner allows the use of short format instructions; in addition, any of the individual registers can be accessed directly.

The pin functions and the pin assignments of the Z8681/82 40-pin package are illustrated in Figures 1 and 2, respectively.

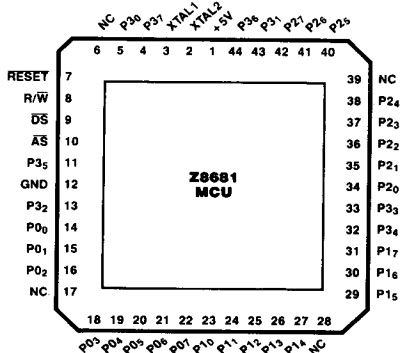


Figure 2b. 44-pin Chip Carrier, Pin Assignments

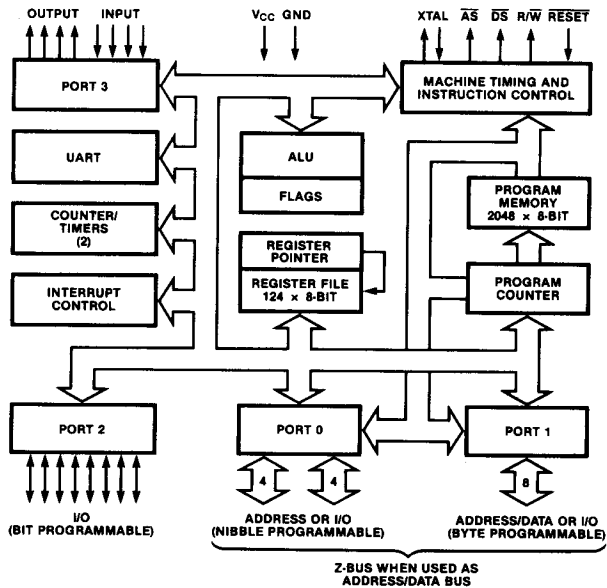


Figure 3. Functional Block Diagram

## ARCHITECTURE

Z8681/82 architecture is characterized by a flexible I/O scheme, an efficient register and address space structure and a number of ancillary features that are helpful in many applications.

Microcomputer applications demand powerful I/O capabilities. The Z8681/82 fulfills this with 24 pins available for input and output. These lines are grouped into three ports of eight lines each and are configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an Address bus for interfacing external memory.

Three basic address spaces are available: program

memory, data memory and the register file (internal). The 143-byte random-access register file is composed of 124 general-purpose registers, three I/O port registers, and 16 control and status registers.

To unburden the program from coping with real-time problems such as serial data communication and counting/timing, an asynchronous receiver/transmitter (UART) and two counter/timers with a large number of user-selectable modes are offered on-chip. Hardware support for the UART is minimized because one of the on-chip timers supplies the bit rate. Figure 3 shows the Z8681/82 block diagram.

## PIN DESCRIPTION

**$\overline{AS}$ .** *Address Strobe* (output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle. Addresses output via Port 1 for all external program or data memory transfers are valid at the trailing edge of  $\overline{AS}$ .

**$\overline{DS}$ .** *Data Strobe* (output, active Low). Data Strobe is activated once for each external memory transfer.

**P0<sub>0</sub>-P0<sub>7</sub>, P2<sub>0</sub>-P2<sub>7</sub>, P3<sub>0</sub>-P3<sub>7</sub>.** *I/O Port Lines* (input/outputs, TTL-compatible). These 24 lines are divided into three 8-bit I/O ports that can be configured under program control for I/O or external memory interface (Figure 3).

**P1<sub>0</sub>-P1<sub>7</sub>.** *Address/Data Port* (bidirectional). Multiplexed address (A<sub>0</sub>-A<sub>7</sub>) and data (D<sub>0</sub>-D<sub>7</sub>) lines used to interface with

program and data memory.

**$\overline{RESET}$ .** *Reset* (input, active Low).  $\overline{RESET}$  initializes the Z8681/82. After  $\overline{RESET}$  the Z8681 is in the extended memory mode. When  $\overline{RESET}$  is deactivated, program execution begins from program location 000C<sub>H</sub> for the Z8681 and 0812<sub>H</sub> for the Z8682.

**$R/\overline{W}$ .** *Read/Write* (output).  $R/\overline{W}$  is Low when the Z8681/82 is writing to external program or data memory.

**XTAL1, XTAL2.** *Crystal 1, Crystal 2* (time-base input and output). These pins connect a parallel-resonant crystal to the on-chip clock oscillator and buffer.

## SUMMARY OF Z8681 AND Z8682 DIFFERENCES

Feature	Z8681	Z8682
Address of first instruction executed after Reset	12	2066
Addressable memory space	0-64K	2K-64K
Address of interrupt vectors	0-11	2048-2065
Reset input high voltage	TTL levels *	7.35-8.0V
Port 0 configuration after Reset	Input, float after reset. Can be programmed as Address bits.	Output, configured as Address bit A <sub>8</sub> -A <sub>15</sub> .
External memory timing start-up configurations	Extended Timing	Normal Timing
Interrupt vectors	2 byte vectors point directly to service routines.	2 byte vectors in internal ROM point to 3 byte Jump instructions, which point to service routines.
Interrupt response time	26 clocks	36 clocks

\* 8.0V V<sub>IN</sub> max.

## ADDRESS SPACES

**Program Memory\*.** The Z8681/82 addresses 64K/62K bytes of external program memory space (Figure 4).

For the Z8681, the first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Program execution begins at location 000C<sub>H</sub> after a reset.

The Z8682 has six 24-bit interrupt vectors beginning at address 0800<sub>H</sub>. The vectors consist of Jump Absolute instructions. After a reset, program execution begins at location 0812<sub>H</sub> for the Z8682.

**Data Memory\*.** The Z8681/82 can address 64K/62K bytes of external data memory. External data memory may be included with or separated from the external program memory space. DM, an optional I/O function that can be programmed to appear on pin P3<sub>4</sub>, is used to distinguish between data and program memory space.

**Register File.** The 143-byte register file includes three I/O

port registers (R0, R2, R3), 124 general-purpose registers (R4-R127) and 16 control and status registers (R240-R255). These registers are assigned the address locations shown in Figure 5.

Z8681/82 instructions can access registers directly or indirectly with an 8-bit address field. This also allows short 4-bit register addressing using the Register Pointer (one of the control registers). In the 4-bit mode, the register file is divided into nine working-register groups, each occupying 16 contiguous locations (Figure 5). The Register Pointer addresses the starting location of the active working-register group (Figure 6).

**Stacks.** Either the internal register file or the external data memory can be used for the stack. A 16-bit Stack Pointer (R254 and R255) is used for the external stack, which can reside anywhere in data memory. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 124 general-purpose registers (R4-R127).

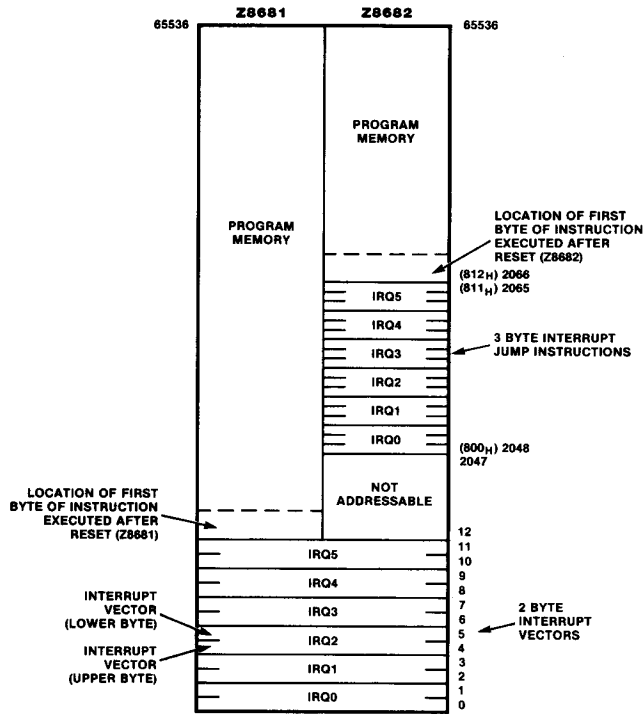


Figure 4. Z8681/82 Program Memory Map

\*This feature differs in the Z8681 and Z8682.



## COUNTER/TIMERS

The Z8681/82 contains two 8-bit programmable counter/timers ( $T_0$  and  $T_1$ ), each driven by its own 6-bit programmable prescaler. The  $T_1$  prescaler can be driven by internal or external clock sources; however, the  $T_0$  prescaler is driven by the internal clock only.

The 6-bit prescalers can divide the input frequency of the clock source by any number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of count, a timer interrupt request—IRQ4 ( $T_0$ ) or IRQ5 ( $T_1$ )—is generated.

The counters can be started, stopped, restarted to continue, or restarted from the initial value. The counters can also be programmed to stop upon reaching zero (single-pass

mode) or to automatically reload the initial value and continue counting (modulo- $n$  continuous mode). The counters, but not the prescalers, can be read any time without disturbing their value or count mode.

The clock source for  $T_1$  is user-definable; it can be either the internal microprocessor clock divided by four, or an external signal input via Port 3. The Timer Mode register configures the external timer input as an external clock, a trigger input that can be retriggerable or nonretriggerable, or as a gate input for the internal clock. The counter/timers can be programmably cascaded by connecting the  $T_0$  output to the input of  $T_1$ . Port 3 line P3<sub>6</sub> also serves as a timer output ( $T_{OUT}$ ) through which  $T_0$ ,  $T_1$  or the internal clock can be output.

## I/O PORTS

The Z8681/82 has 24 lines available for input and output. These lines are grouped into three ports of eight lines each and are configurable as input, output or address. Under software control, the ports can be programmed to provide

address outputs, timing, status signals, serial I/O, and parallel I/O with or without handshake. All ports have active pull-ups and pull-downs compatible with TTL loads.

**Port 1** is a dedicated Z-BUS compatible memory interface. The operations of Port 1 are supported by the Address Strobe ( $\overline{AS}$ ) and Data Strobe ( $\overline{DS}$ ) lines, and by the Read/Write ( $\overline{R/W}$ ) and Data Memory ( $\overline{DM}$ ) control lines. The low-order program and data memory addresses ( $A_0$ - $A_7$ ) are output through Port 1 (Figure 8) and are multiplexed with data in/out ( $D_0$ - $D_7$ ). Instruction fetch and data memory read/write operations are done through this port.

Port 1 cannot be used as a register nor can a handshake mode be used with this port.

Both the Z8681 and Z8682 wake up with the 8 bits of Port 1 configured as address outputs for external memory. If more than eight address lines are required with the Z8681, additional lines can be obtained by programming Port 0 bits as address bits. The least-significant four bits of Port 0 can

be configured to supply address bits  $A_8$ - $A_{11}$  for 4K byte addressing or both nibbles of Port 0 can be configured to supply address bits  $A_8$ - $A_{15}$  for 64K byte addressing.

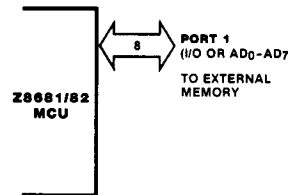


Figure 8. Port 1

**Port 0\*** can be programmed as a nibble I/O port, or as an address port for interfacing external memory (Figure 9). When used as an I/O port, Port 0 can be placed under handshake control. In this configuration, Port 3 lines P3<sub>2</sub> and P3<sub>5</sub> are used as the handshake controls  $\overline{DAV}_0$  and  $\overline{RDY}_0$ . Handshake signal assignment is dictated by the I/O direction of the upper nibble P0<sub>4</sub>-P0<sub>7</sub>.

For external memory references, Port 0 can provide address bits  $A_8$ - $A_{11}$  (lower nibble) or  $A_8$ - $A_{15}$  (lower and upper nibbles) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing.

In the Z8681\*, Port 0 lines float after reset; their logic state is unknown until the execution of an initialization routine that configures Port 0.

\*This feature differs in the Z8681 and Z8682.

Such an initialization routine must reside within the first 256 bytes of executable code and must be physically mapped into memory by forcing the Port 0 address lines to a known state (Figure 10). The proper port initialization sequence is:

1. Write initial address ( $A_8$ - $A_{15}$ ) of initialization routine to Port 0 address lines.
2. Configure Port 0 Mode register to output  $A_8$ - $A_{15}$  (or  $A_8$ - $A_{11}$ ).

To permit the use of slow memory, an automatic wait mode of two oscillator clock cycles is configured for the bus timing of the Z8681 after each reset. The initialization routine could include reconfiguration to eliminate this extended timing mode.

The following example illustrates the manner in which an initialization routine can be mapped in a Z8681 system with 4K of memory.

*Example.* In Figure 10, the initialization routine is mapped to the first 256 bytes of program memory. Pull-down resistors maintain the address lines at a logic 0 level when these lines are floating. The leakage current caused by fanout must be taken into consideration when selecting the value of the pull-down resistors. The resistor value must be large enough to allow the Port 0 output driver to pull the line to a logic 1. Generally, pulldown resistors are incompatible with TTL loads. If Port 0 drives into TTL input loads ( $I_{LOW} = 1.6 \text{ mA}$ ) the external resistors should be tied to  $V_{CC}$  and the initialization routine put in address space  $FF00_H$ – $FFFF_H$ .

In the Z8682\*, Port 0 lines are configured as address lines  $A_8$ – $A_{15}$  after a Reset. If one or both nibbles are needed for

I/O operation, they must be configured by writing to the Port 0 Mode register. The Z8682 is in the fast memory timing mode after Reset, so the initialization routine must be in fast memory.

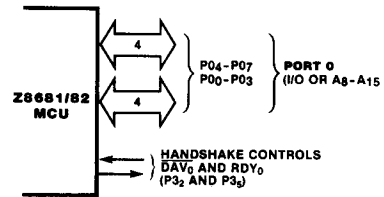


Figure 9. Port 0

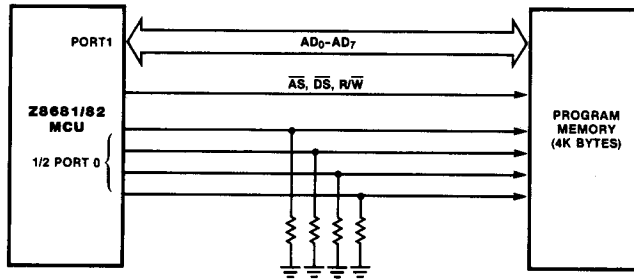


Figure 10. Port 0 Address Lines Tied to Logic 0

Port 2 bits can be programmed independently as input or output (Figure 11). This port is always available for I/O operations. In addition, Port 2 can be configured to provide open-drain outputs.

Like Port 0, Port 2 may also be placed under handshake control. In this configuration, Port 3 lines  $P_{31}$  and  $P_{36}$  are used as the handshake controls lines  $DAV_2$  and  $RDY_2$ . The handshake signal assignment for Port 3 lines  $P_{31}$  and  $P_{36}$  is dictated by the direction (input or output) assigned to bit 7 of Port 2.

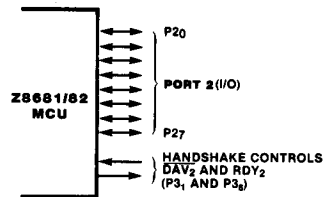


Figure 11. Port 2

Port 3 lines can be configured as I/O or control lines (Figure 12). In either case, the direction of the eight lines is fixed as four input ( $P_{30}$ – $P_{33}$ ) and four output ( $P_{34}$ – $P_{37}$ ). For serial I/O, lines  $P_{30}$  and  $P_{37}$  are programmed as serial in and serial out, respectively.

Port 3 can also provide the following control functions: handshake for Ports 0 and 2 ( $DAV$  and  $RDY$ ); four external interrupt request signals ( $IRQ_0$ – $IRQ_3$ ); timer input and output signals ( $T_{IN}$  and  $T_{OUT}$ ) and Data Memory Select ( $DM$ ).

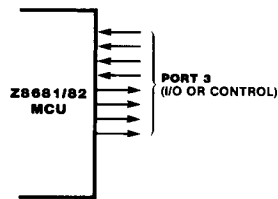


Figure 12. Port 3

\*This feature differs in the Z8681 and Z8682.

## INTERRUPTS\*

The Z8681/82 allows six different interrupts from eight sources: the four Port 3 lines P3<sub>0</sub>-P3<sub>3</sub>, Serial In, Serial Out, and the two counter/timers. These interrupts are both maskable and prioritized. The Interrupt Mask register globally or individually enables or disables the six interrupt requests. When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register.

All Z8681 and Z8682 interrupts are vectored through locations in program memory. When an interrupt request is granted, an interrupt machine cycle is entered. This disables all subsequent interrupts, saves the Program Counter and status flags, and accesses the program memory vector location reserved for that interrupt. In the Z8681, this memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. The Z8681 takes 26 system clock cycles to enter an interrupt subroutine.

The Z8682 has a small internal ROM that contains six 2-byte interrupt vectors pointing to addresses 2048-2065, where 3-byte jump absolute instructions are located (Figure 4 and Table 1). These jump instructions each contain a 1-byte

opcode and a 2-byte starting address for the interrupt service routine. The Z8682 takes 36 system clock cycles to enter an interrupt subroutine.

**Table 1. Z8682 Interrupt Processing**

Hex Address	Contains Jump Instruction and Subroutine Address For
800-802	IRQ0
803-805	IRQ1
806-808	IRQ2
809-80B	IRQ3
80C-80E	IRQ4
80F-811	IRQ5

Polled interrupt systems are also supported. To accommodate a polled structure, any or all of the interrupt inputs can be masked and the Interrupt Request register polled to determine which of the interrupt requests needs service.

## CLOCK

The on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal or to any suitable external clock source (XTAL1 = Input, XTAL2 = Output).

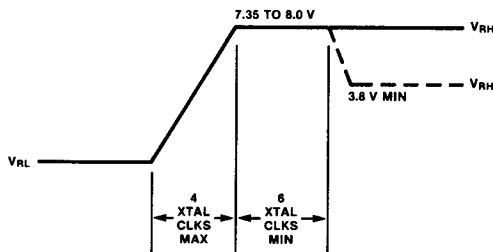
The crystal source is connected across XTAL1 and XTAL2, using the recommended capacitance ( $C_L = 15$  pf maximum) from each pin to ground. The specifications for the crystal are as follows:

- AT cut, parallel-resonant
- Fundamental type
- Series resistance,  $R_s \leq 100\Omega$
- For Z8681/Z8682, 8 MHz maximum
- For Z8681-12, 12 MHz maximum

## Z8681/Z8682 INTERCHANGEABILITY

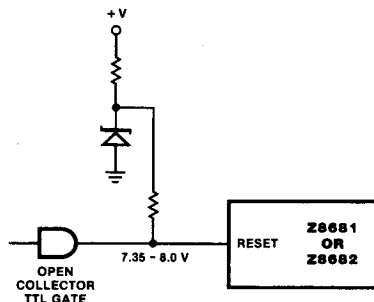
Although the Z8681 and Z8682 have minor differences, a system can be designed for compatibility with both ROMless versions. To achieve interchangeability, the design must take into account the special requirements of each device in the external interface, initialization, and memory mapping.

**External Interface.** The Z8682 requires a 7.5V positive logic level on the RESET pin for at least 6 clock periods immediately following reset, as shown in Figure 13. The Z8681 requires a 3.8V or higher positive logic level, but is compatible with the Z8682 RESET waveform. Figure 14 shows a simple circuit for generating the 7.5V level.



**Figure 13. Z8682 RESET Pin Input Waveform**

\*This feature differs in the Z8681 and Z8682.



**Figure 14. RESET Circuit**

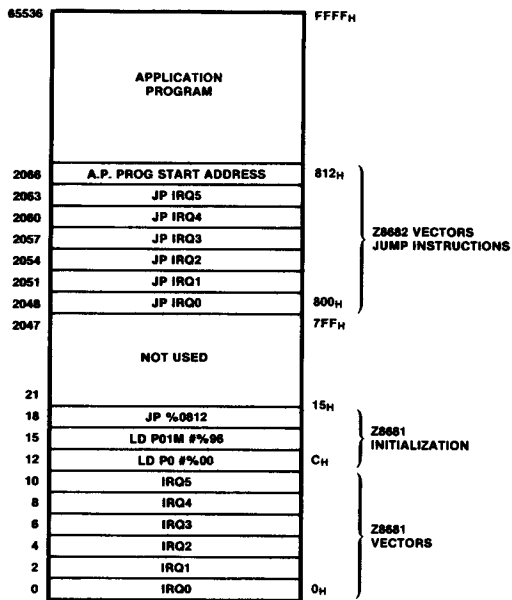


**Initialization.** The Z8681 wakes up after reset with Port 0 configured as an input, which means Port 0 lines are floating in a high-impedance state. Because of this pullup or pulldown, resistors must be attached to Port 0 lines to force them to a valid logic level until Port 0 is configured as an address port.

Port 0 initialization is discussed in the section on ports. An example of an initialization routine for Z8681/Z8682 compatibility is shown in Table 2. Only the Z8681 need execute this program.

**Table 2. Initialization Routine**

Address	Opcodes	Instruction	Comments
000C	E6 00 00	LD PO #%%00	Set A <sub>8</sub> -A <sub>15</sub> to 0.
000F	E6 F8 96	LD P01M #%%96	Configure Port 0 as A <sub>8</sub> -A <sub>15</sub> . Eliminate extended memory timing.
0012	8D 08 12	JP START ADDRESS	Execute application program.

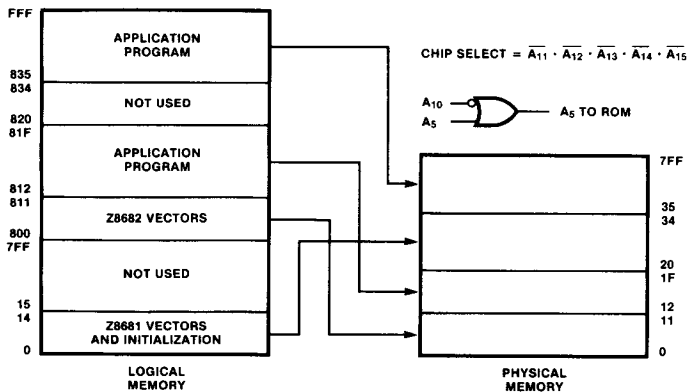
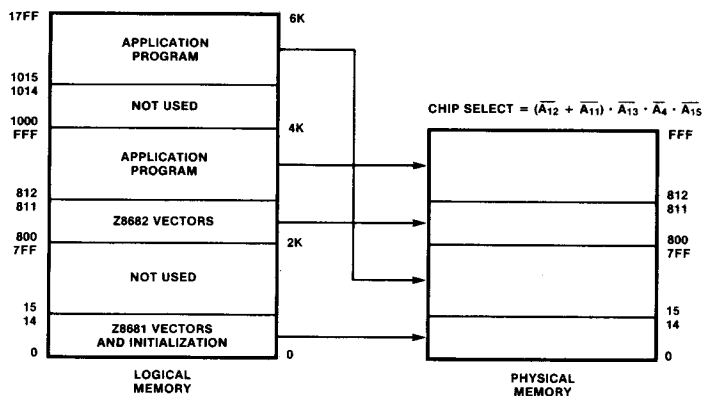


**Figure 15. Z8681/82 Logical Program Memory Mapping**

Z8681/82 MCT

**Memory Mapping.** The Z8681 and Z8682 lower memory boundaries are located at 0 and 2048, respectively. A single program ROM can be used with either product if the logical program memory map shown in Figure 15 is followed. The Z8681 vectors and initialization routine must be starting at

address 0 and the Z8682 3-byte vectors (jump instructions) must be at address 2048 and higher. Addresses in the range 21-2047 are not used. Figure 16 shows practical schemes for implementing this memory map using 4K and 2K ROMs.



**Figure 16. Practical Schemes for Implementing Z8681 and Z8682 Compatible Memory Map**

## INSTRUCTION SET NOTATION

**Addressing Modes.** The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

<b>IRR</b>	Indirect register pair or indirect working-register pair address
<b>irr</b>	Indirect working-register pair only
<b>X</b>	Indexed address
<b>DA</b>	Direct address
<b>RA</b>	Relative address
<b>IM</b>	Immediate
<b>R</b>	Register or working-register address
<b>r</b>	Working-register address only
<b>IR</b>	Indirect-register or indirect working-register address
<b>ir</b>	Indirect working-register address only
<b>RR</b>	Register pair or working register pair address

**Symbols.** The following symbols are used in describing the instruction set.

<b>dst</b>	Destination location or contents
<b>src</b>	Source location or contents
<b>cc</b>	Condition code (see list)
<b>@</b>	Indirect address prefix
<b>SP</b>	Stack pointer (control registers 254-255)
<b>PC</b>	Program counter
<b>FLAGS</b>	Flag register (control register 252)
<b>RP</b>	Register pointer (control register 253)
<b>IMR</b>	Interrupt mask register (control register 251)

Assignment of a value is indicated by the symbol "←". For example,

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr(n)" is used to refer to bit "n" of a given location. For example,

dst (7)

refers to bit 7 of the destination operand.

**Flags.** Control Register R252 contains the following six flags:

<b>C</b>	Carry flag
<b>Z</b>	Zero flag
<b>S</b>	Sign flag
<b>V</b>	Overflow flag
<b>D</b>	Decimal-adjust flag
<b>H</b>	Half-carry flag

Affected flags are indicated by:

<b>0</b>	Cleared to zero
<b>1</b>	Set to one
<b>*</b>	Set or cleared according to operation
<b>—</b>	Unaffected
<b>X</b>	Undefined

Z8681/82 MCU

## CONDITION CODES

Value	Mnemonic	Meaning	Flags Set
1000		Always true	—
0111	C	Carry	C = 1
1111	NC	No carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not equal	Z = 0
1001	GE	Greater than or equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater than	[Z OR (S XOR V)] = 0
0010	LE	Less than or equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned greater than or equal	C = 0
0111	ULT	Unsigned less than	C = 1
1011	UGT	Unsigned greater than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned less than or equal	(C OR Z) = 1
0000		Never true	—

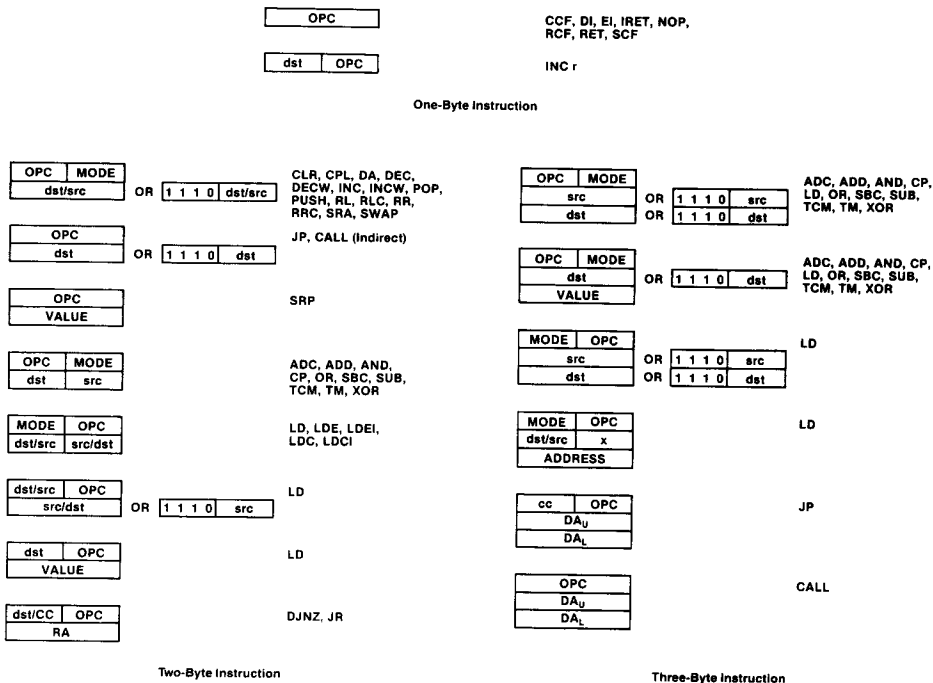


Figure 17. Instruction Formats

## INSTRUCTION SUMMARY

Instruction and Operation	Addr Mode		Opcode Byte (Hex)	Flags Affected					
	dst	src		C	Z	S	V	D	H
<b>ADC</b> dst,src dst ← dst + src + C	(Note 1)		1□	*	*	*	*	0	*
<b>ADD</b> dst,src dst ← dst + src	(Note 1)		0□	*	*	*	*	0	*
<b>AND</b> dst,src dst ← dst AND src	(Note 1)		5□	—	*	*	*	0	—
<b>CALL</b> dst SP ← SP - 2 @SP ← PC; PC ← dst	DA IRR		D6 D4	—	—	—	—	—	—
<b>CCF</b> C ← NOT C			EF	*	—	—	—	—	—
<b>CLR</b> dst dst ← 0	R IR		B0 B1	—	—	—	—	—	—
<b>COM</b> dst dst ← NOT dst	R IR		60 61	—	*	*	*	0	—
<b>CP</b> dst,src dst - src	(Note 1)		A□	*	*	*	*	*	—
<b>DA</b> dst dst ← DA dst	R IR		40 41	*	*	*	*	X	—

Instruction and Operation	Addr Mode		Opcode Byte (Hex)	Flags Affected					
	dst	src		C	Z	S	V	D	H
<b>DEC</b> dst dst ← dst - 1	R IR		00 01	—	*	*	*	*	—
<b>DECW</b> dst dst ← dst - 1	RR IR		80 81	—	*	*	*	*	—
<b>DI</b> IMR (7) ← 0			8F	—	—	—	—	—	—
<b>DJNZ</b> r,dst r ← r - 1 if r ≠ 0 PC ← PC + dst Range: +127, -128	RA		rA	—	—	—	—	—	—
<b>EI</b> IMR (7) ← 1			9F	—	—	—	—	—	—
<b>INC</b> dst dst ← dst + 1	r R IR		rE 20 21	—	*	*	*	*	—
<b>INCW</b> dst dst ← dst + 1	RR IR		A0 A1	—	*	*	*	*	—

# INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Addr Mode		Opcode Byte (Hex)	Flags Affected						
	dst	src		C	Z	S	V	D	H	
<b>IRET</b> FLAGS ← @SP; SP ← SP + 1 PC ← @SP; SP ← SP + 2; IMR(7) ← 1			BF	*	*	*	*	*	*	
<b>JP</b> cc, dst if cc is true PC ← dst	DA		cD 30	-	-	-	-	-	-	
<b>JR</b> cc, dst if cc is true, PC ← PC + dst Range: +127, -128	RA		cB 30	-	-	-	-	-	-	
<b>LD</b> dst, src dst ← src	r R	lm R	rC r8 r9	-	-	-	-	-	-	
	r	X	C7							
	X	r	D7							
	r	lr	E3							
	lr	r	F3							
	R	R	E4							
	R	IR	E5							
	R	IM	E6							
	IR	IM	E7							
	IR	R	F5							
<b>LDC</b> dst, src dst ← src	r	lrr	C2 D2	-	-	-	-	-	-	
<b>LDCI</b> dst, src dst ← src r ← r + 1; rr ← rr + 1	lr	lrr	C3 D3	-	-	-	-	-	-	
<b>LDE</b> dst, src dst ← src	r	lrr	82 92	-	-	-	-	-	-	
<b>LDEI</b> dst, src dst ← src r ← r + 1; rr ← rr + 1	lr	lrr	83 93	-	-	-	-	-	-	
<b>NOP</b>			FF	-	-	-	-	-	-	
<b>OR</b> dst, src dst ← dst OR src	(Note 1)		4□	-	*	*	0	-	-	
<b>POP</b> dst dst ← @SP; SP ← SP + 1	R		50 51	-	-	-	-	-	-	
<b>PUSH</b> src SP ← SP - 1; @SP ← src	R		70 71	-	-	-	-	-	-	
<b>RCF</b> C ← 0			CF	0	-	-	-	-	-	
<b>RET</b> PC ← @SP; SP ← SP + 2			AF	-	-	-	-	-	-	
<b>RL</b> dst		R IR	90 91	*	*	*	*	-	-	

Instruction and Operation	Addr Mode		Opcode Byte (Hex)	Flags Affected						
	dst	src		C	Z	S	V	D	H	
<b>RLC</b> dst		R IR	10 11	*	*	*	*	-	-	
<b>RR</b> dst		R IR	E0 E1	*	*	*	*	-	-	
<b>RRC</b> dst		R IR	C0 C1	*	*	*	*	-	-	
<b>SBC</b> dst, src dst ← dst ← src ← C	(Note 1)		3□	*	*	*	*	1	*	
<b>SCF</b> C ← 1			DF	1	-	-	-	-	-	
<b>SRA</b> dst		R IR	D0 D1	*	*	*	0	-	-	
<b>SRP</b> src RP ← src		lm	31	-	-	-	-	-	-	
<b>SUB</b> dst, src dst ← dst ← src	(Note 1)		2□	*	*	*	*	1	*	
<b>SWAP</b> dst		R IR	F0 F1	X	*	*	X	-	-	
<b>TCM</b> dst, src (NOT dst) AND src	(Note 1)		6□	-	*	*	0	-	-	
<b>TM</b> dst, src dst AND src	(Note 1)		7□	-	*	*	0	-	-	
<b>XOR</b> dst, src dst ← dst XOR src	(Note 1)		B□	-	*	*	0	-	-	

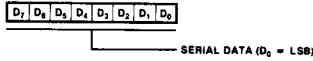
NOTE: These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a □ in this table, and its value is found in the following table to the left of the applicable addressing mode pair. For example, the opcode of an ADC instruction using the addressing modes r (destination) and lr (source) is 13.

Addr Mode		Lower Opcode Nibble
dst	src	
r	r	2
r	lr	3
R	R	4
R	IR	5
R	IM	6
IR	IM	7

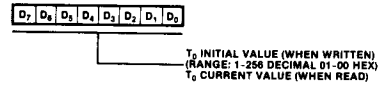
Z8681/82 MCU

# REGISTERS

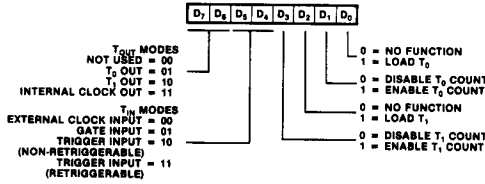
## R240 SIO Serial I/O Register (F0H; Read/Write)



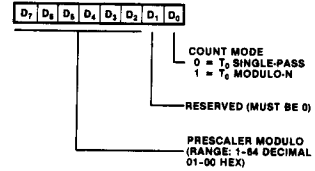
## R244 TO Counter/Timer 0 Register (F4H; Read/Write)



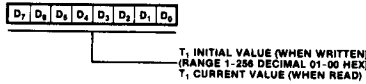
## R241 TMR Time Mode Register (F1H; Read/Write)



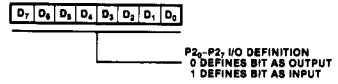
## R245 PRE0 Prescaler 0 Register (F5H; Write Only)



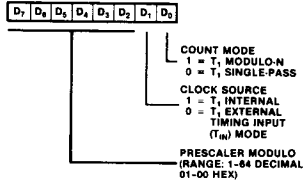
## R242 T1 Counter Timer 1 Register (F2H; Read/Write)



## R246 P2M Port 2 Mode Register (F6H; Write Only)



## R243 PRE1 Prescaler 1 Register (F3H; Write Only)



## R247 P3M Port 3 Mode Register (F7H; Write Only)

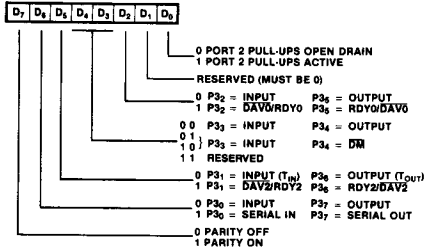
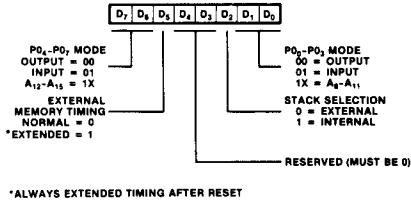


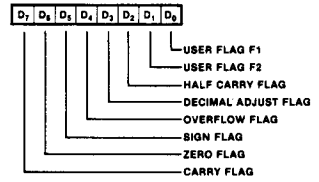
Figure 18. Control Registers

**REGISTERS**  
(Continued)

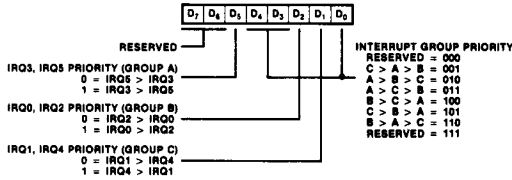
**R248 P01M**  
**Port 0 Register**  
(F8H; Write Only)



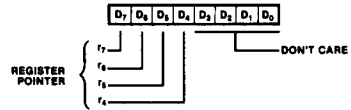
**R252 FLAGS**  
**Flag Register**  
(FCH; Read/Write)



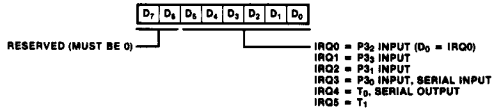
**R249 IPR**  
**Interrupt Priority Register**  
(F9H; Write Only)



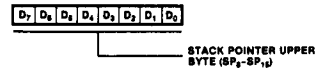
**R253 RP**  
**Register Pointer**  
(FDH; Read/Write)



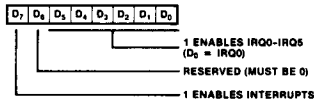
**R250 IRQ**  
**Interrupt Request Register**  
(FAH; Read/Write)



**R254 SPH**  
**Stack Pointer**  
(FEH; Read/Write)



**R251 IMR**  
**Interrupt Mask Register**  
(FBH; Read/Write)



**R255 SPL**  
**Stack Pointer**  
(FFH; Read/Write)

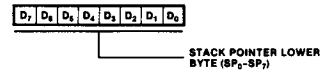
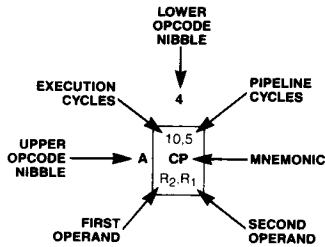


Figure 18. Control Registers (Continued)

Z8681/82 MCU

# Z86L81/85 OPCODE MAP

		Lower Nibble (Hex)															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Upper Nibble (Hex)	0	6.5 DEC R <sub>1</sub>	6.5 DEC IR <sub>1</sub>	6.5 ADD r <sub>1</sub> ,r <sub>2</sub>	6.5 ADD r <sub>1</sub> ,IR <sub>2</sub>	10.5 ADD R <sub>2</sub> ,R <sub>1</sub>	10.5 ADD IR <sub>2</sub> ,R <sub>1</sub>	10.5 ADD R <sub>1</sub> ,IM	10.5 ADD IR <sub>1</sub> ,IM	6.5 LD r <sub>1</sub> ,R <sub>2</sub>	6.5 LD r <sub>2</sub> ,R <sub>1</sub>	12/10.5 DJNZ r <sub>1</sub> ,RA	12/10.0 JR cc,RA	6.5 LD r <sub>1</sub> ,IM	12/10.0 JP cc,DA	6.5 INC r <sub>1</sub>	
	1	6.5 RLC R <sub>1</sub>	6.5 RLC IR <sub>1</sub>	6.5 ADC r <sub>1</sub> ,r <sub>2</sub>	6.5 ADC r <sub>1</sub> ,IR <sub>2</sub>	10.5 ADC R <sub>2</sub> ,R <sub>1</sub>	10.5 ADC IR <sub>2</sub> ,R <sub>1</sub>	10.5 ADC R <sub>1</sub> ,IM	10.5 ADC IR <sub>1</sub> ,IM								
	2	6.5 INC R <sub>1</sub>	6.5 INC IR <sub>1</sub>	6.5 SUB r <sub>1</sub> ,r <sub>2</sub>	6.5 SUB r <sub>1</sub> ,IR <sub>2</sub>	10.5 SUB R <sub>2</sub> ,R <sub>1</sub>	10.5 SUB IR <sub>2</sub> ,R <sub>1</sub>	10.5 SUB R <sub>1</sub> ,IM	10.5 SUB IR <sub>1</sub> ,IM								
	3	8.0 JP IRR <sub>1</sub>	6.1 SRP IM	6.5 SBC r <sub>1</sub> ,r <sub>2</sub>	6.5 SBC r <sub>1</sub> ,IR <sub>2</sub>	10.5 SBC R <sub>2</sub> ,R <sub>1</sub>	10.5 SBC IR <sub>2</sub> ,R <sub>1</sub>	10.5 SBC R <sub>1</sub> ,IM	10.5 SBC IR <sub>1</sub> ,IM								
	4	8.5 DA R <sub>1</sub>	8.5 DA IR <sub>1</sub>	6.5 OR r <sub>1</sub> ,r <sub>2</sub>	6.5 OR r <sub>1</sub> ,IR <sub>2</sub>	10.5 OR R <sub>2</sub> ,R <sub>1</sub>	10.5 OR IR <sub>2</sub> ,R <sub>1</sub>	10.5 OR R <sub>1</sub> ,IM	10.5 OR IR <sub>1</sub> ,IM								
	5	10.5 POP R <sub>1</sub>	10.5 POP IR <sub>1</sub>	6.5 AND r <sub>1</sub> ,r <sub>2</sub>	6.5 AND r <sub>1</sub> ,IR <sub>2</sub>	10.5 AND R <sub>2</sub> ,R <sub>1</sub>	10.5 AND IR <sub>2</sub> ,R <sub>1</sub>	10.5 AND R <sub>1</sub> ,IM	10.5 AND IR <sub>1</sub> ,IM								
	6	6.5 COM R <sub>1</sub>	6.5 COM IR <sub>1</sub>	6.5 TCM r <sub>1</sub> ,r <sub>2</sub>	6.5 TCM r <sub>1</sub> ,IR <sub>2</sub>	10.5 TCM R <sub>2</sub> ,R <sub>1</sub>	10.5 TCM IR <sub>2</sub> ,R <sub>1</sub>	10.5 TCM R <sub>1</sub> ,IM	10.5 TCM IR <sub>1</sub> ,IM								
	7	10/12.1 PUSH R <sub>2</sub>	12/14.1 PUSH IR <sub>2</sub>	6.5 TM r <sub>1</sub> ,r <sub>2</sub>	6.5 TM r <sub>1</sub> ,IR <sub>2</sub>	10.5 TM R <sub>2</sub> ,R <sub>1</sub>	10.5 TM IR <sub>2</sub> ,R <sub>1</sub>	10.5 TM R <sub>1</sub> ,IM	10.5 TM IR <sub>1</sub> ,IM								
	8	10.5 DECW RR <sub>1</sub>	10.5 DECW IR <sub>1</sub>	12.0 LDE r <sub>1</sub> ,IR <sub>2</sub>	18.0 LDEI IR <sub>1</sub> ,IR <sub>2</sub>												6.1 DI
	9	6.5 RL R <sub>1</sub>	6.5 RL IR <sub>1</sub>	12.0 LDE r <sub>2</sub> ,IR <sub>1</sub>	18.0 LDEI IR <sub>2</sub> ,IR <sub>1</sub>												6.1 EI
	A	10.5 INCW RR <sub>1</sub>	10.5 INCW IR <sub>1</sub>	6.5 CP r <sub>1</sub> ,r <sub>2</sub>	6.5 CP r <sub>1</sub> ,IR <sub>2</sub>	10.5 CP R <sub>2</sub> ,R <sub>1</sub>	10.5 CP IR <sub>2</sub> ,R <sub>1</sub>	10.5 CP R <sub>1</sub> ,IM	10.5 CP IR <sub>1</sub> ,IM								14.0 RET
	B	6.5 CLR R <sub>1</sub>	6.5 CLR IR <sub>1</sub>	6.5 XOR r <sub>1</sub> ,r <sub>2</sub>	6.5 XOR r <sub>1</sub> ,IR <sub>2</sub>	10.5 XOR R <sub>2</sub> ,R <sub>1</sub>	10.5 XOR IR <sub>2</sub> ,R <sub>1</sub>	10.5 XOR R <sub>1</sub> ,IM	10.5 XOR IR <sub>1</sub> ,IM								16.0 IRET
	C	6.5 RRC R <sub>1</sub>	6.5 RRC IR <sub>1</sub>	12.0 LDC r <sub>1</sub> ,IR <sub>2</sub>	18.0 LDCI IR <sub>1</sub> ,IR <sub>2</sub>					10.5 LD r <sub>1</sub> ,x,R <sub>2</sub>							6.5 RCF
	D	6.5 SRA R <sub>1</sub>	6.5 SRA IR <sub>1</sub>	12.0 LDC r <sub>2</sub> ,IR <sub>1</sub>	18.0 LDCI IR <sub>2</sub> ,IR <sub>1</sub>	20.0 CALL* IRR <sub>1</sub>		20.0 CALL DA	10.5 LD r <sub>2</sub> ,x,R <sub>1</sub>								6.5 SCF
	E	6.5 RR R <sub>1</sub>	6.5 RR IR <sub>1</sub>		6.5 LD r <sub>1</sub> ,IR <sub>2</sub>	10.5 LD R <sub>2</sub> ,R <sub>1</sub>	10.5 LD IR <sub>2</sub> ,R <sub>1</sub>	10.5 LD R <sub>1</sub> ,IM	10.5 LD IR <sub>1</sub> ,IM								6.5 CCF
	F	8.5 SWAP R <sub>1</sub>	8.5 SWAP IR <sub>1</sub>		6.5 LD r <sub>1</sub> ,r <sub>2</sub>		10.5 LD R <sub>2</sub> ,IR <sub>1</sub>										6.0 NOP



**Legend:**  
R = 8-bit address  
r = 4-bit address  
R<sub>1</sub> or r<sub>1</sub> = Dst address  
R<sub>2</sub> or r<sub>2</sub> = Src address

**Sequence:**  
Opcode, First Operand, Second Operand

NOTE: The blank areas are not defined.

\*2-byte instruction; fetch cycle appears as a 3-byte instruction



## ABSOLUTE MAXIMUM RATINGS

Voltages on all pins except RESET  
with respect to GND . . . . . -0.3V to +7.0V  
Operating Ambient  
Temperature . . . . . See Ordering Information  
Storage Temperature . . . . . -65°C to +150°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## STANDARD TEST CONDITIONS

The DC characteristics listed below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin.

- $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$  for S (Standard temperature)
- $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$  for E (Extended temperature)

Standard conditions are as follows:

- $+4.75\text{V} \leq V_{CC} \leq +5.25\text{V}$
- $\text{GND} = 0\text{V}$

The Ordering Information section lists package temperature ranges and product numbers. Refer to the Literature List for additional documentation. Package drawings are in the Package Information section.

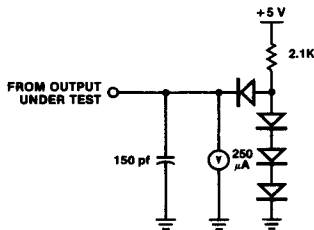


Figure 19. Test Load 1

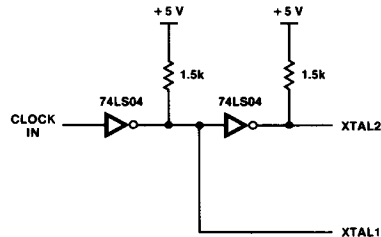


Figure 20. External Clock Interface Circuit

## DC CHARACTERISTICS

Symbol	Parameter	Min	Max	Unit	Condition
$V_{CH}$	Clock Input High Voltage	3.8	$V_{CC}$	V	Driven by External Clock Generator
$V_{CL}$	Clock Input Low Voltage	-0.3	0.8	V	Driven by External Clock Generator
$V_{IH}$	Input High Voltage	2.0	$V_{CC}$	V	
$V_{IL}$	Input Low Voltage	-0.3	0.8	V	
$V_{RH}$	Reset Input High Voltage	3.8	$V_{CC}$	V	See Note
$V_{RL}$	Reset Input Low Voltage	-0.3	0.8	V	
$V_{OH}$	Output High Voltage	2.4		V	$I_{OH} = -250 \mu\text{A}$
$V_{OL}$	Output Low Voltage		0.4	V	$I_{OL} = +2.0 \text{ mA}$
$I_{IL}$	Input Leakage	-10	10	$\mu\text{A}$	$0\text{V} \leq V_{IN} \leq +5.25\text{V}$
$I_{OL}$	Output Leakage	-10	10	$\mu\text{A}$	$0\text{V} \leq V_{IN} \leq +5.25\text{V}$
$I_{IR}$	Reset Input Current		-50	$\mu\text{A}$	$V_{CC} = +5.25\text{V}, V_{RL} = 0\text{V}$
$I_{CC}$	$V_{CC}$ Supply Current		180	mA	

\*The Reset line (pin 6) is used to place the Z8682 in external memory mode. This is accomplished as shown in Figure 13.

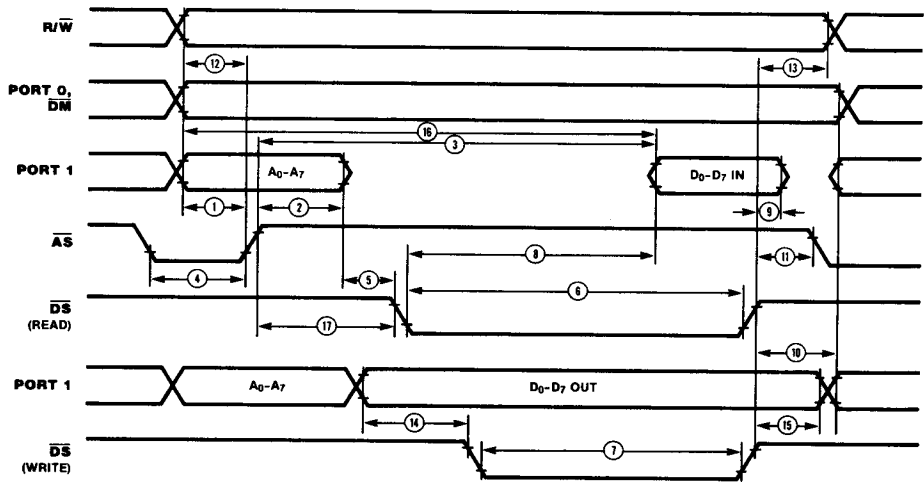


Figure 21. External I/O or Memory Read/Write Timing

## AC CHARACTERISTICS

External I/O or Memory Read and Write Timing

Number	Symbol	Parameter	Z8681/82 8 MHz		Z8681 12 MHz		Notes *†°
			Min	Max	Min	Max	
1	TdA(AS)	Address Valid to $\overline{AS}$ ↑ Delay	50		35		2,3
2	TdAS(A)	$\overline{AS}$ ↑ to Address Float Delay	70		45		2,3
3	TdAS(DR)	$\overline{AS}$ ↑ to Read Data Required Valid		360		220	1,2,3
4	TwAS	$\overline{AS}$ Low Width	80		55		2,3
5	TdAz(DS)	Address Float to $\overline{DS}$ ↓	0		0		
6	TwDSR	$\overline{DS}$ (Read) Low Width	250		185		1,2,3
7	TwDSW	$\overline{DS}$ (Write) Low Width	160		110		1,2,3
8	TdDSR(DR)	$\overline{DS}$ ↓ to Read Data Required Valid		200		130	1,2,3
9	ThDR(DS)	Read Data to $\overline{DS}$ ↑ Hold Time	0		0		
10	TdDS(A)	$\overline{DS}$ ↑ to Address Active Delay	70		45		2,3
11	TdDS(AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay	70		55		2,3
12	TdR/W(AS)	R/ $\overline{W}$ Valid to $\overline{AS}$ ↑ Delay	50		30		2,3
13	TdDS(R/W)	$\overline{DS}$ ↑ to R/ $\overline{W}$ Not Valid	60		35		2,3
14	TdDW(DSW)	Write Data Valid to $\overline{DS}$ (Write) ↓ Delay	50		35		2,3
15	TdDS(DW)	$\overline{DS}$ ↑ to Write Data Not Valid Delay	70		45		2,3
16	TdA(DR)	Address Valid to Read Data Required Valid		410		255	1,2,3
17	TdAS(DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ Delay	80		55		2,3

NOTES:

1. When using extended memory timing add 2 TpC.
2. Timing numbers given are for minimum TpC.
3. See clock cycle time dependent characteristics table.

\* All units in nanoseconds (ns).

† Test Load 1

° All timing references use 2.0V for a logic "1" and 0.8V for a logic "0".

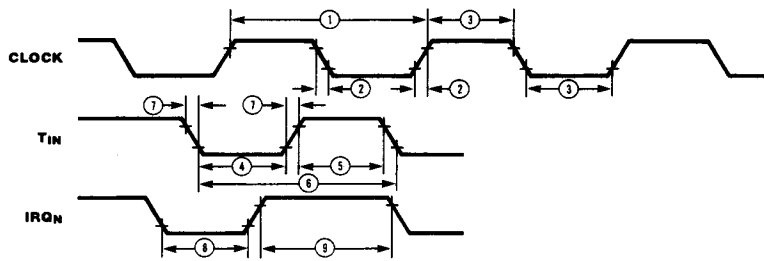


Figure 22. Additional Timing

## AC CHARACTERISTICS

### Additional Timing Table

Number	Symbol	Parameter	Z8681/82 8 MHz		Z8681 12 MHz		Notes*
			Min	Max	Min	Max	
1	TpC	Input Clock Period	125	1000	83	1000	1
2	TrC, TfC	Clock Input Rise and Fall Times		25		15	1
3	TwC	Input Clock Width	37		70		1
4	TwTinL	Timer Input Low Width	100		70		2
5	TwTinH	Timer Input High Width	3TpC		3TpC		2
6	TpTin	Timer Input Period	8TpC		8TpC		2
7	TrTin, TfTin	Timer Input Rise and Fall Times		100		100	2
8	TwIL	Interrupt Request Input Low Time	100		70		2,3
9	TwIH	Interrupt Request Input High Time	3TpC		3TpC		2,3

NOTES:

1. Clock timing references use 3.8V for a logic "1" and 0.8V for a logic "0".

2. Timing references use 2.0V for a logic "1" and 0.8V for a logic "0".

3. Interrupt request via Port 3.

\* Units in nanoseconds (ns).

Z8681/82 MCTD

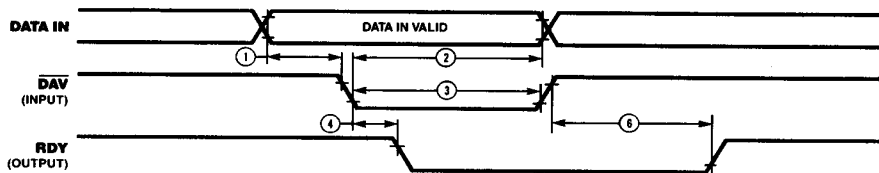


Figure 23a. Input Handshake Timing

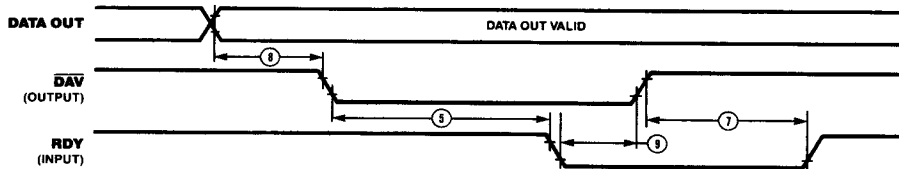


Figure 23b. Output Handshake Timing

## AC CHARACTERISTICS

### Handshake Timing

Number	Symbol	Parameter	Z8681/82		Z8681		Notes†*
			Min	Max	Min	Max	
1	TsDI(DAV)	Data In Setup Time	0		0		
2	ThDI(DAV)	Data In Hold Time	230		160		
3	TwDAV	Data Available Width	175		120		
4	TdDAVlf(RDY)	$\overline{\text{DAV}} \downarrow$ Input to RDY $\downarrow$ Delay		175		120	1,2
5	TdDAVOl(RDY)	$\overline{\text{DAV}} \downarrow$ Output to RDY $\downarrow$ Delay	0		0		1,3
6	TdDAVlr(RDY)	$\overline{\text{DAV}} \uparrow$ Input to RDY $\uparrow$ Delay		175		120	1,2
7	TdDAVOl(RDY)	$\overline{\text{DAV}} \uparrow$ Output to RDY $\uparrow$ Delay	0		0		1,3
8	TdDO(DAV)	Data Out to $\overline{\text{DAV}} \downarrow$ Delay	50		30		1
9	TdRDY(DAV)	Rdy $\downarrow$ Input to $\overline{\text{DAV}} \uparrow$ Delay	0	200	0	140	1

NOTES:

1. Test load 1

2. Input handshake

3. Output handshake

† All timing references use 2.0V for a logic "1" and 0.8V for a logic "0".

\* Units in nanoseconds (ns).

## CLOCK CYCLE TIME-DEPENDENT CHARACTERISTICS

Number	Symbol	Z8681/82	Z8681
		8 MHz Equation	12 MHz Equation
1	TdA(AS)	TpC-75	TpC-50
2	TdAS(A)	TpC-55	TpC-40
3	TdAS(DR)	4TpC-140 *	4TpC-110 *
4	TwAS	TpC-45	TpC-30
6	TwDSR	3TpC-125 *	3TpC-65 *
7	TwDSW	2TpC-90 *	2TpC-55 *
8	TdDSR(DR)	3TpC-175 *	3TpC-120 *
10	Td(DS)A	TpC-55	TpC-40
11	TdDS(AS)	TpC-55	TpC-30
12	TdR/W(AS)	TpC-75	TpC-55
13	TdDS(R/W)	TpC-65	TpC-50
14	TdDW(DSW)	TpC-75	TpC-50
15	TdDS(DW)	TpC-55	TpC-40
16	TdA(DR)	5TpC-215 *	5TpC-160 *
17	TdAS(DS)	TpC-45	TpC-30

\* Add 2TpC when using extended memory timing

Z8681/82 MCTU

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## ORDERING INFORMATION

### Z8 ROMless MCU, 8.0 MHz

**40-pin DIP**

Z8681 PS

Z8681 CS

Z8681 PE

Z8681 CE

Z8681 CM\*

**44-pin PCC**

Z8681 VS†

### Z8 ROMless MCU, 12.0 MHz

**40-pin DIP**

Z8681-12 PS

Z8681-12 CS

**44-pin PCC**

Z8681-12 VS†

### Z8 ROMless MCU, 8.0 MHz

**40-pin DIP**

Z8682 PS

Z8682 CS

Z8682 PE

Z8682 CE

## Codes

First letter is for package; second letter is for temperature.

C = Ceramic DIP  
P = Plastic DIP  
L = Ceramic LCC  
V = Plastic PCC

R = Protopack  
T = Low Profile Protopack  
DIP = Dual-In-Line Package  
LCC = Leadless Chip Carrier  
PCC = Plastic Chip Carrier (Leaded)

## TEMPERATURE

S = 0°C to +70°C  
E = -40°C to +85°C  
M\* = -55°C to +125°C

FLOW  
B = 883 Class B

Example: PS is a plastic DIP, 0°C to +70°C.

†Available soon.

\*For Military Orders, contact your local Zilog Sales Office for Military Electrical Specifications.